UNIVERSITÀ DELLA CALABRIA

UNIVERSITA' DELLA CALABRIA

Dipartimento di Fisica

Scuola di Dottorato

di Scienza e Tecnica BERNARDINO TELESIO

Con il contributo del CERN

CICLO

XXVIII

TITOLO TESI

High-Repeatable Data Acquisition Systems for Pulsed Power Converters in Particle Accelerator Structures

Settore Scientifico Disciplinare ICAR/08

Direttore: Ch.mo Prof. Roberto Bartolino

Supervisore: Ch.mo Prof. Raffaele Zinno

Ch.mo Prof. Pasquale Arpaia

Tutor: Ph.D. Michele Martino

Dottorando: Dott. Carlo Baccigalupi

Summary

In this Ph.D. thesis, the issues related to the metrological characterization of high-performance pulsed power converters are addressed.

Initially, a background and a state of the art on the measurement systems needed to correctly operate a high-performance power converter are presented. As a matter of fact, power converters usually exploits digital control loops to enhance their performance. In this context the final performance of a power converter has to be validated by a reference instrument with higher metrological characteristics. In addition, an on-line measurement system is also needed to digitize the quantity to be controlled with high accuracy.

Then, in industrial applications of power converters metrology, specifications are given in terms of Worst-Case Uncertainty (WCU). Therefore, an analytical model for predicting the Worst-Case Uncertainty (WCU) of a measurement system is discussed and detailed for an instrument affected by Gaussian noise. Furthermore, the study and the design of a *Reference Acquisition System* for characterizing the high-power pulses of the klystron modulators of the Compact LInear Collider ($CLIC$), a new linear accelerator under study at CERN, is presented. Finally, the design of an *On-line Acquisition System* for controlling the CLIC power converter, is presented.

The Thesis continues with the numerical results obtained in simulation for the three main topics (Worst-Case Uncertainty, Reference Acquisition System, On-line Acquisition System) to demonstrate the effectiveness of the proposals.

Finally, the experimental results of a case study in the framework of the above-mentioned CLIC accelerator are reported and compared with the simulations in order to obtain the final validation of the proposals. In particular, CLIC main requirements for the measurement systems mostly concern their level of repeatability which was proven to be only affected by the instrumental noise under certain assumptions. Thus, the two systems were designed to be ultra-low noise solutions and, in turn, they are demonstrated to be repeatable in the order of few tens of parts per million (ppm).

Acknowledgements

I would like to express my sincere gratitude to my university supervisors.
Professor Pasquale Arpaia for sharing his experience and fundamental knowledge with me.
Professors Raffaele Zinno and Domenico Grimaldi for their patience and support.

I am deeply grateful to my CERN supervisor, Ph.D. Michele Martino for his excellent guidance. His constant presence was a fundamental incitement to improve my professional competencies.

My sincere thanks also go to Ph.D. Miguel Cerqueira Bastos and the Electrical Power Converters group at CERN for offering me the opportunity to work in such an interesting and challenging project. Being surrounded by exceptional and helpful colleagues represented an incredible mine to draw upon.

I would like to thank Francesca for standing by me every time I need. Sharing with you this bitter sweet life is my biggest success.

I would also like to thank my family. They were always supporting me and encouraging me with unconditional love.

Finally, I thank all my friends. One of the greatest gifts of life is friendship, and I have received it.

Geneva, November 25^{th} *2015* C. B.

Contents

List of Figures

List of Tables

Symbols and Acronyms

ADC = Analogue-to-Digital Converter
$AWGN$ = Additive White Gaussian Noise
CDF = Cumulative Density Function
$CLIC$ = Compact LInear Collider
$CMRR$ = Common-Mode Rejection Ratio
DSC = Differential Sensing Circuit
$ENOB$ = Effective Number of Bits
EVT = Extreme Value Theory
FTD = Flat-Top Duration
GUM = Guide to the expression of Uncertainty in Measurement
iid = independent and identically distributed
LHC = Large Hadron Collider
LSB = Least Significant Bit
LSE = Least Squares Errors
N_o = Number of Observations
N_p = Number of pulses
N_s = Number of Samples
PDF = Probability Density Function
ppm = parts per million (referred to $10V$ so $1\,ppm = 10\,\mu V$)
PPR = Pulse-to-Pulse Repeatability
RMS = Root Mean Square
RTI = Referred to Input
$SINAD$ = SIgnal-to-Noise And Distortion ratio
VIM = International Vocabulary of Metrology
WCU = Worst-Case Uncertainty
WCR = Worst-Case Repeatability

Introduction

A power converter is a device able to process and control the flow of electric energy by supplying voltages and currents in a form that is optimally suited for the user loads. In power engineering, a converter has to transform electric energy from one form to another (e.g. from AC to DC) [1]. High-performance power converters are becoming more and more used in applications in which a big amount of energy is demanded by the load and, thus, the power consumption from the electrical grid should be kept as low as possible (e.g. reducing losses). This is the case, for instance, of smart power flow management among separate energy storage units [2] or high-performance electric vehicles [3]. In many applications in which power consumption is relevant, pulsed power converters are used [4]. In Fig.1, the typical topology of a pulsed power converter is sketched. The energy coming from the electrical grid is stored into a charging system. A pulse forming system allows the stored energy to be released to the load over a short period, by obtaining a train of high peak-power pulses.

An adequate control for power supply quality is provided through a comprehensive characterization of power pulses (node *B* in Fig.1), both in time and frequency domains. Of course, to characterize the power pulses, a reference measurement system is needed [5]. However, the main evolution efforts were dedicated to pushing the technology toward to the sub-nanosecond regime overlooking the aspects related to the accurate and precise digitization of the pulses themselves. Thus, the metrological problem of a full characterization of the

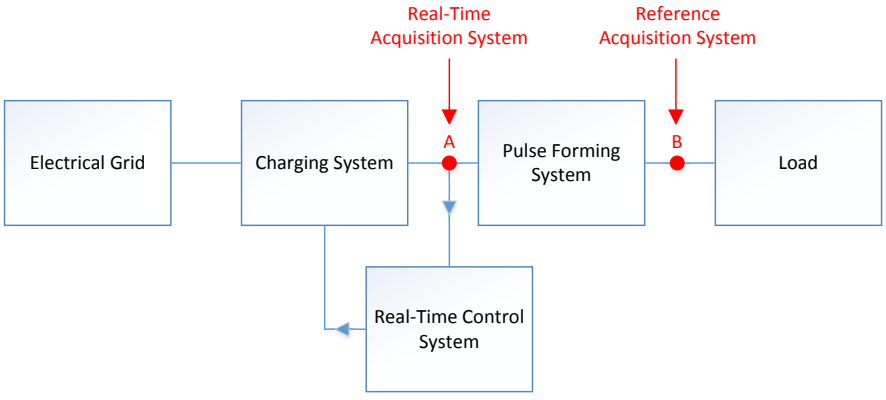

Figure 1 – Typical Topology of a Pulsed Power Converter.

pulsed power converter becomes challenging because of the lack of reference instruments [6]. Furthermore, even if the reference standards concerning pulse measurements [7] give both definitions and procedures to evaluate the pulse parameters, a full characterization procedure in time-domain is not provided; thus, custom methods have to be identified along the specific applications.

Due to all the uncertainty sources inside the measurement chain (e.g. noise super-posed to the measurand, intrinsic uncertainty of the measurement system, and so on), a statistical approach should be used to define the pulses characteristics. In many industrial applications, a worst-case approach is desired in order to determine an uncertainty interval in which any measurement will lie (under given conditions) [8].

In addition, applying digital methods to the control of power converters allows different enhancements as (i) creating new features, (ii) improving performance, and (iii) increasing flexibility while keeping low the cost [9]. Indeed, high-performance pulsed power converters usually exploit a digital control loop for regulating the voltage out of the charging system [9]. To do that, a high-performance real-time acquisition system is needed to digitize the output of the charging system (node *A* in Fig.1) and provide the samples to the controller of the loop in order to adjust the voltage [10]. In this PhD thesis, all these aspects are discussed and addressed.

In particular, in *PART 1*, a background and a state of the art on the measurement systems needed to correctly operate a high-performance power converter are presented.

In *PART 2*, the analytical model for predicting the Worst-Case Uncertainty (WCU) of a measurement system is discussed and detailed for an instrument affected by gaussian noise. Furthermore, the study and design of a *Reference Acquisition System* for characterizing the high-power pulses of the klystron modulators of the CLIC , is presented. Finally, the design of the *Real-Time Acquisition System* for controlling the CLIC power converter, is presented.

In *PART 3*, the numerical results obtained in simulation of the three main topics (Worst-Case Uncertainty, Reference Acquisition System, Real-Time Acquisition System) are discussed to demonstrate the effectiveness of the proposals.

Finally, in *PART 4*, the experimental results of a case study in the framework of the new linear electron-positron particle accelerator currently under study at *CERN*, the Compact LInear Collider ($CLIC$) [11], are reported and compared with the simulations in order to obtain the final validation of the proposals.

PART 1 - BACKGROUND AND STATE OF THE ART

Background

At CERN, a new particle accelerator is currently under study, the Compact LInear Collider (*CLIC*) [11]. The CLIC project is focused on the design of a linear electron-positron collider with a center-of-mass collision energy of 3 TeV and a luminosity of $2 \times 10^{34}\, cm^{-2} s^{-1}$.

In Fig.2, the latest layout of CLIC is reported. The top part of the figure shows the Drive Beam generation in two Main Linacs and the successive time compression of the Drive Beam pulses in the Delay Loops and Combiner Rings (CR1 and CR2). The time-compressed Drive Beam reaches a current of about 100 A at a beam energy of about 2.4 GeV. This compressed Drive Beam is transported through the Main Linac tunnel to 24 individual turnarounds. Each Drive Beam segment is directed by pulsed extraction elements, for the final RF power generation, into the accelerating structures of the Main Beams. Hence in the Main Linac tunnel we find four beam transport lines: the transport lines of the Main Beam and Drive Beam plus the acceleration line for the Main Beam and the deceleration line for the Drive Beam. The beams collide after a long Beam Delivery Section (BDS) (collimation, final focus) in one interaction point (IP) in the center of the complex [12].

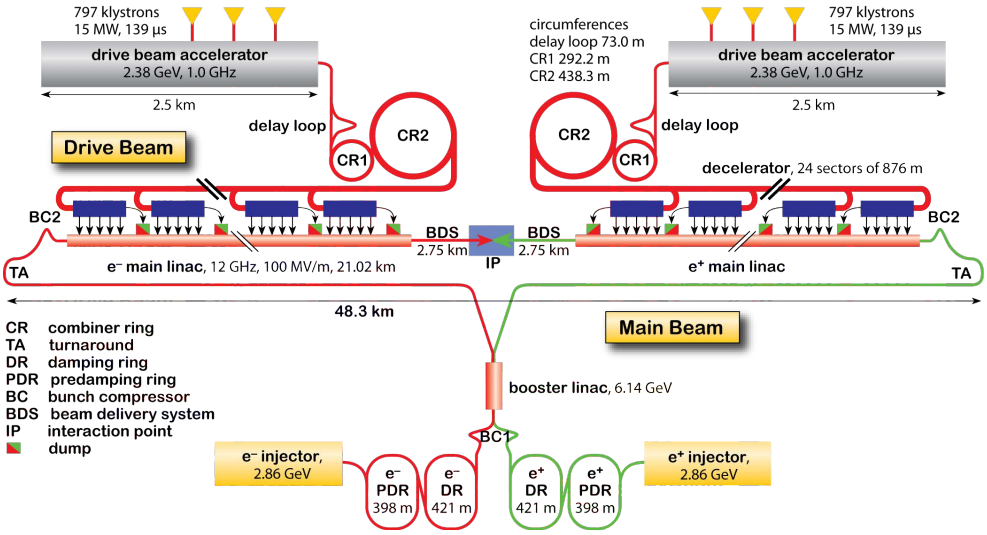

Figure 2 – CLIC Layout at 3 TeV

Fig.3, shows a possible implementation of this accelerator in the Geneva area. The proportions become more clear. The generation of the Main Beams, the Drive Beams, and the central collision point would fall into existing CERN territory, whereas the two 24 m long acceleration tunnels would extend into the local area as underground installations. The blue dots show the tunnel length needed for a collision energy of 3 TeV, whereas the pink dots indicate the size of the installation for 500 GeV.

To operate such a high-performance particle accelerator a huge amount of energy needs to be provided by its power converters. In fact, the *mass-energy* equivalence formulated by Einstein,

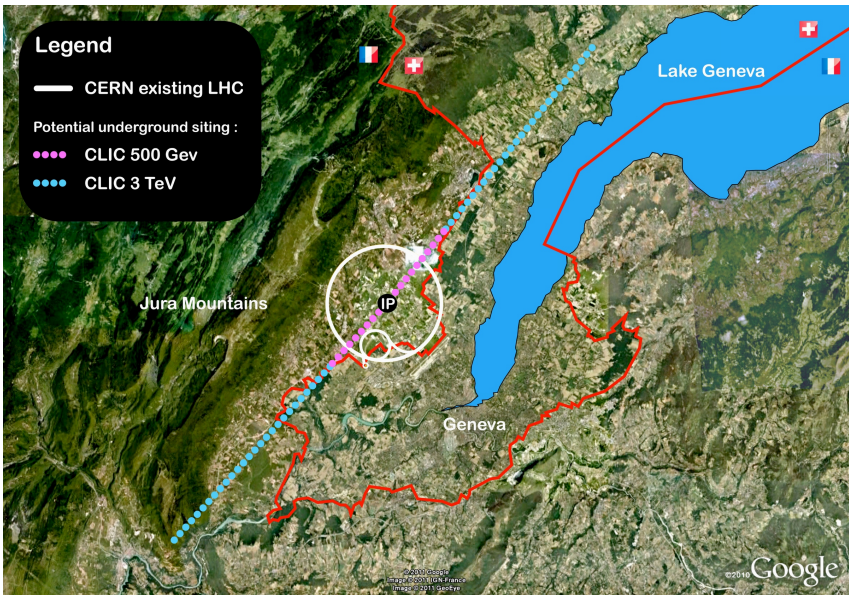

Figure 3 – Map showing a potential location for the CLIC accelerator complex

reported in equation (1), states that the more particles are accelerated, the more mass they gain and thus, the more high-energy collisions can be observed.

$$E = mc^2 \tag{1}$$

In order to accelerate and guide a beam of charged particles (q), forces shall be applied according to equation (2):

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B}) \tag{2}$$

The first part of equation (2), $q\vec{E}$, indicates that particles are accelerated by means of an electrical field. To reach an adequate level of acceleration, high-voltage power converters are needed to generate strong electrical fields. In addition, the second part of equation (2), states that as the energy of particles increases, the magnetic field controlling their trajectory must also increase. Therefore, strong magnetic fields are demanded to the electro-magnets. Once again, to do that, power converters are needed.

In order to reach the desired energy level, together with reasonable power consumption from the electrical grid, *CLIC* power converters [13] are demanded to deliver a pulsed power repeatable to better than ±100 parts per million (ppm) [14]. Its klystron modulators [15] will therefore be operated in pulsed mode with a pulse length of 140 μs [14],[11]. In Tab.1, the typical specifications of the *CLIC* power pulses are reported.

Table 1 – Typical Pulse Characteristics.

Pulse Specification		
Parameter	**Acronym**	**Value**
Nominal Pulse Amplitude Level	V_{kn}	$180\,kV$
Nominal Pulse Current Level	I_{kn}	$150\,A$
Pulse Peak Power	$P_{mod-out}$	$\approx 27\,MW$
Positive Going Transition Duration	t_{rise}	$3\,\mu s$
Negative Going Transition Duration	t_{fall}	$3\,\mu s$
Transition Settling Duration	t_{set}	$5\,\mu s$
Flat-Top Duration	t_{flat}	$140\,\mu s$
Repetition Rate	$REPR$	$50\,Hz$
Voltage Overshoot	V_{ovs}	$1\,\%$
Precisions		
Flat-Top Tolerance	FTT	$0.85\,\%$
Pulse-to-Pulse Repeatability	PPR	$\pm 100\ ppm$
Frequency Range of Interest	FRI	$1\,kHz - 5\,MHz$

Two different topologies of the *CLIC* klystron modulator are currently under study at *ETH Zurich (CH)* [16] and the *LEEPCI Laval (CA)* [17]. In Fig.4, the latest topology of the modulator under study at *ETH Zurich* is sketched. As shown in Fig.4, to meet the requirements for the RF power quality, derived directly from the accelerator performance specifications, two high-performance measurement system are needed.

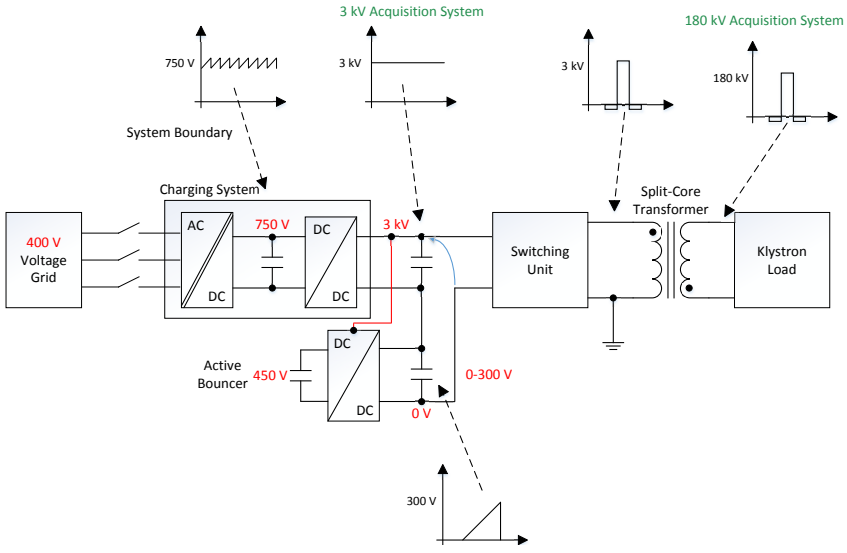

Figure 4 – Topology of the CLIC Klystron Modulator.

The first one (*3 kV Acquisition System* in Fig.4) will be used for a real-time control of the output voltage of the charging system. The second one (*180 kV Acquisition System* in Fig.4) will be used for an offline verification of the modulator performance, in particular with respect to its Pulse-to-Pulse Repeatability (PPR).

State of the Art

Pulsed power supplies are widely used in many applications as radars, pulsed lasers, electromagnetic pulse generators and particle accelerators. In this framework, the full characterization of power pulses is needed, both in time and frequency domains, in order to guarantee an adequate control for power supply quality.

The market interest and the research on pulse measurements are significantly dedicated to improving the immunity to interference demanded by the transmission protocols in Ultra Wide-Band (UWB) applications [18]. This trend was highlighted in the state of the art for time-domain pulse waveform measurements in the nanosecond regime, produced by the National Institute of Standards and Technology (NIST) [6]. The main evolution efforts were dedicated to pushing the technology toward to the sub-nanosecond regime overlooking the aspects related to the accurate and precise digitization of the pulses themselves. Thus, the metrological problem of a full characterization of the pulsed power converter becomes challenging because of the lack of reference instruments. Furthermore, even if the reference standards concerning pulse measurements [7] give both definitions and procedures to evaluate the pulse parameters, a full characterization procedure in time-domain is not provided; thus, custom methods have to be identified along the specific applications.

In this context, the crucial specification of Worst-Case Uncertainty (WCU) [19] is required as in many other engineering fields, such as nuclear or aero-space applications. However, WCU is not included into the Guide to the Expression of Uncertainty in Measurements (GUM) [20], which mainly focuses on providing the standard uncertainty associated with a best estimate of a measurand. More recently, the focus of the *GUM* working group has shifted towards the probability density function (*pdf*) as a comprehensive way to express the experimenter's knowledge of a measurand [21]. Moreover, in the measurement practice, the WCU is usually determined as a Type-B uncertainty [22], e.g. on the basis of manufacturer's production specification of the particular instrument. In many cases of research, when custom-designed instruments have to be characterized, manufacturer's specifications are not available, thus Type-A methods have to be defined for determining WCU. In fact, this turns into the problem of characterizing the extreme values (e.g. the peaks) considered as the worst cases of a measurement system working in its nominal conditions [23]. The Uni-variate Extreme Value Theory, or simply Extreme Value Theory, is widely used for predicting the peak values of a given phenomenon in different fields (e.g., risk management [24],[25], finance, economics, or even for estimating the fastest human time on the $100\,m$ sprint [26]), and specifically in engineering, e.g., studies ranging from tides [27] to accelerator technology [28]. As an example, in telecommunications, an accurate expression for the peak distribution of the Orthogonal Frequency Division Multiplexing (OFDM) envelope was determined by the University of Massachusetts [29]. In fact, the main problem about the applicability of OFDM systems in low-power wireless applications is the highly-variable amplitude of transmitted signals. The above study defined a rigorous method for predicting the upcoming peak values of the envelope by the previous peak observations.

However, this means that each prediction needs to be supported by an adequate data collection which, in some cases, requires very-long observations of the phenomena, resulting in unfeasible test duration. Therefore, an analytical model was identified to overcome this problem by predicting the WCU statistical distribution of a given instrument by only characterizing its internal noise.

If on one side one has to guarantee the final performance of a power converter by means of a reference acquisition system, on the other side the introduction of a digital control loop allows different enhancements while keeping low the cost of the converter [9]. Indeed, high-performance pulsed power converters usually exploit a digital control loop for regulating the voltage out of the charging system [9]. To do that, a high-performance real-time acquisition system is needed to digitize the output of the charging system (node A in Fig.1) and provide the samples to the controller of the loop in order to adjust the voltage. In designing an effective digital control system, the main challenge is to meet simultaneously both the metrological requirements and the time constraints imposed by the specific application. As a matter of fact, the stability of a regulator is heavily affected by the speed of the control loop. Researchers working in fields ranging from military [30] to electronic controls in automotive [31], found great interest in this research line. However new and more demanding applications arise from particle accelerator structures in which the repeatability of the power converters is a key parameter for guaranteeing the performance of the machine.

PART 2 - PROPOSAL

1 The Worst-Case Uncertainty Analytical Model

In this chapter, the exact Cumulative Distribution Function (*CDF*) of the uncertainty of several measurements, modelled as independent and identically distributed (iid) normal random variables, is presented, together with an approximated *pdf* of the Worst Case Uncertainty.

1.1 Overview

In a set of replicated measurements of the same measurand, the upcoming peaks can be forecast without any knowledge about preliminary observations or data collections, thus overcoming the main issue related to the Extreme Value Theory. In section 1.2, the metrological problem is formalized and an analytical WCU model is proposed. In section 4.1, a case study at CERN on a reference acquisition system for assessing the performance of a high-voltage pulsed power supply for the klystron modulators of the Compact LInear Collider ($CLIC$) is introduced. In particular, in section 4.2, the numerical results of performance analysis of the proposed model, aimed at confirming the validity of the underlying approximations, are reported. Finally, in section 7, the distribution approximated through the model is validated by comparison with experimental results obtained with the reference acquisition system for the $CLIC$ klystron modulators.

1.2 Worst-Case Uncertainty Theoretical Model

In this section, an approximated *pdf* of the type-A WCU is defined for Gaussian-noise measurement systems by deriving the exact *CDF* of replicated measurements, modelled as independent and identically distributed (iid) normal random variables. In particular, after stating the metrological problem, the WCU definition is given, by analysing the three random variables corresponding to its three main operations of difference, absolute value and maximum. Finally, the analytical model is derived, by leaving to the Appendix A the rigorous proofs of both its equation and the Gaussian noise approximation.

1.2.1 Worst-Cacse Uncertainty Definition

In many situations, a periodic signal is to be acquired in a given time window, and measurements have to be taken in different periods. Among these periods, the measured instantaneous values at the *same* (in equivalent time) sampling instant can vary significantly owing to several uncertainty sources. In many research cases when custom-designed instruments have to be characterized, manufacturer's specifications are not available, thus Type-A methods have to be defined for determining WCU. In fact, this turns into the problem of characterizing the extreme values (e.g. the peaks) considered as the worst cases of a measurement system working under its nominal conditions [23].

If the measurand is assumed to be *ideal* and the measurement system has negligible instability within the signal period, then the measurement is affected only by the instrumental *noise*, defined according to the Standard IEEE 1057-07 [32] as: "Any deviation between the output signal (converted to input units) and the input signal except deviations caused by linear time invariant system response (gain and phase shift), a dc level shift, total harmonic distortion (THD), or an error in the sample rate".

Hereafter, all the samples of the measurement system noise (and their random effect) are modelled as independent and identically distributed (iid) random variables. By acquiring N_s samples per period and a total number N_p of periods, the WCU can be defined as in equation 1.1, where three operations are carried out on each of the N_o pairs of acquired periods ($N_o = N_p - 1$), (i) the difference, (ii) the absolute value, and (iii) the maximum:

$$WCU = max_i |V_{i,j} - V_{i,j+1}| \tag{1.1}$$

where $V_{i,j}$ and $V_{i,j+1}$ are the values of the i^{th} samples of the j^{th} and $(j+1)^{th}$ acquired periods, respectively (Fig.1.1), with:

$$\begin{cases} 1 \le i \le N_s \\ 1 \le j \le N_o \end{cases} \tag{1.2}$$

In the following subsections, the three random variables, corresponding to the above operations, are analysed for deriving the WCU model equation.

The Difference Random Variable

For a given index j, N_s random variables $Y_i = V_{i,j} - V_{i,j+1}$ with $1 \le i \le N_s$ are defined. Actually, Y_i coincides with $Y_{i,j}$, therefore,in the following, the latter full notation will be used only when

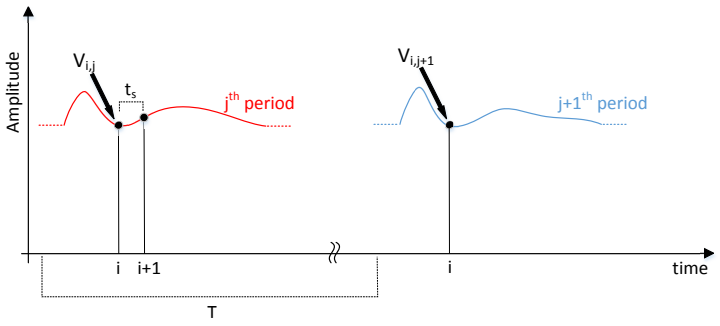

Figure 1.1 – Worst-Case Uncertainty Definition (t_s: sampling period, T: signal period).

necessary for the sake of clarity. The generic $V_{q,k} = \hat{V}_{q,k} + n_{q,k}$ is the sum of the deterministic sample of the ideal measurand $\hat{V}_{q,k}$ and the random variable $n_{q,k}$ which is a sample of the stationary stochastic process $n(t)$ that represents the time-domain noise of the measurement system.

$$\hat{V}_{i,j} = \hat{V}_{i,k} \quad \forall \begin{cases} 1 \leq i \leq N_s \\ j,k \in N \end{cases} \tag{1.3}$$

The Absolute Value Random Variable

Under the assumption of statistical independence upon the index j (the issue of statistic dependence will be discussed in detail in the subsequent sections), the Cumulative Distribution Function (CDF) $F_{|Y_i|}(x)$ is computed:

$$\begin{aligned} &F_{|Y_i|}(x) = Pr(|Y_i| \leq x) = Pr(-x \leq Y_i \leq x) = \\ &= Pr(Y_i \leq x) - Pr(Y_i \leq -x) = \\ &= F_{Y_i}(x) - F_{Y_i}(-x) \end{aligned} \tag{1.4}$$

By assuming that each $V_{i,j}$ is symmetrically distributed around its mean value, each Y_i is symmetrically distributed around zero:

$$\begin{aligned} &F_{Y_i}(x) - F_{Y_i}(-x) = F_{Y_i}(x) - [1 - F_{Y_i}(x)] = \\ &= 2F_{Y_i}(x) - 1 \end{aligned} \tag{1.5}$$

Finally, the absolute value is only defined for positive values of x:

$$F_{|Y_i|}(x) = \begin{cases} 2F_{Y_i}(x) - 1 & , x \geq 0 \\ 0 & , x < 0 \end{cases} \tag{1.6}$$

The pdf is given by the derivative of the CDF:

$$f_{|Y_i|}(x) = \begin{cases} 2f_{Y_i}(x) & , x \geq 0 \\ 0 & , x < 0 \end{cases} \tag{1.7}$$

The Maximum Random Variable

Let us consider now the maximum M_j between the N_s independent and identically distributed ($i.i.d.$) random variables $|Y_1|, |Y_2|, ..., |Y_{N_s}|$ (taken from the j^{th} and $j+1^{th}$ periods). The dependence upon j has been already neglected, therefore $M_j = M = max\{|Y_1|, |Y_2|, ..., |Y_{N_s}|\}$. Given the $i.i.d.$ assumptions, the CDF of M is expressed as [33]:

$$F_M(x) = Pr(M \leq x) = Pr(|Y_1| \leq x, |Y_2| \leq x, ..., |Y_{N_s}| \leq x) = \prod_{i=1}^{N_s} Pr(|Y_i| \leq x) = F_{|Y_i|}^{N_s}(x) \tag{1.8}$$

The CDF of M can be now expressed as a function of the CDF of the underlying distribution Y_i.

$$F_{M_j}(x) = \begin{cases} \left[2F_{Y_i}(x) - 1\right]^{N_s} & , x \geq 0 \\ 0 & , x < 0 \end{cases} \tag{1.9}$$

The pdf is simply given by the derivative of the CDF:

$$f_{M_j}(x) = \begin{cases} 2N_s f_{Y_i}(x) \left[2F_{Y_i}(x) - 1\right]^{N_s - 1} & , x \geq 0 \\ 0 & , x < 0 \end{cases} \tag{1.10}$$

Equation (1.10) describes the distribution of WCU_j, as the maximum of the absolute value of the difference of all the samples between two consecutive periods (the index j is fixed).

1.2.2 Analytical Model

Once the WCU was estimated for a given sample size N_o, the variability of M over the N_s periods is considered:

$$\begin{cases} WCU_j = M_j = max_i|V_{i,j} - V_{i,j+1}| & , 1 \le i \le N_s \\ WCU(N_o) = Z = max_j\{M_j\} & , 1 \le j \le N_o \end{cases} \tag{1.11}$$

Having assumed the independence on j, the CDF of $Z = Z^{ind}$ can be computed straightforwardly by simply raising (1.9) to the N_o^{th} power:

$$F_{Z^{ind}}(x) = F_{M_j}^{N_o}(x) = \begin{cases} [2F_{Y_i}(x) - 1]^{N_s \cdot N_o} & , x \ge 0 \\ 0 & , x < 0 \end{cases} \tag{1.12}$$

In the particular case of independent random variables, the analytical equation of the PDF of the WCU distribution is finally assessed by computing the derivative of the equation (1.12):

$$\begin{cases} f_{Z^{ind}}(x) = 2N_sN_of_{Y_i}(x)[2F_{Y_i}(x) - 1]^{N_sN_o-1} & , x \ge 0 \\ 0 & , x < 0 \end{cases} \tag{1.13}$$

So far, the validity of all the equations is guaranteed by assuming that: (i) all the variables $V_{i,j}$ are symmetrically distributed around their mean value (or equivalently, each $Y_{i,j}$ is symmetrically distributed around zero), and (ii) the dependence on j of $Y_{i,j}$ can be neglected. Whereas the first assumption is very weak and fully realistic, the independence on j is very strong and not credible, therefore it must be dealt with properly. In Appendix A, the actual WCU distribution will be presented and discussed. In addition, it will be also proved that the distribution (1.13) is a worst case approximation of the actual distribution in the case of white and Gaussian noise $n(t)$ of the measurement system. In section 4.2, it will be shown that the worst-case approximation accurately models simulation data, whereas in section 7, also the hypothesis of white Gaussian noise will be tested against experimental data of the case study.

2 The Reference Acquisition System

As already said, pulse measurement literature is mainly focused on fast systems with relaxed metrological requirements. In this chapter a new research trend on slower signals with stringent metrological requirements is explored. In particular, an acquisition system to characterize the flat-top of $3\,\mu s$ rise-time trapezoidal voltage pulses, with bandwidth of $5\,MHz$, repeatability of $\pm 25\,ppm$, and noise RMS level in the order of $3\,ppm$, is proposed.

2.1 Overview

In section 2.2, the requirements for the proposed acquisition system as well as the definition of the main target parameter, the Pulse-to-Pulse Repeatability (PPR), are defined. Afterwards, in section 2.3, the proposal of an analogue front-end for improving the measurement conditions is presented together with its design choices. It's important to clarify that the circuit presented in this section is just a proof demonstrator able to validate the feasibility and effectiveness of the proposed architecture. In section 5 and 8 respectively, the Pspice simulations and the experimental results of the proof demonstrator are presented in order to demonstrate a good match between the simulated demonstrator and the actual prototype. An important point is discussed in section 8.0.5 where a Differential Sensing Circuit (DSC) is presented. This circuit represents the interface to the upstream voltage divider (discussed afterward); therefore it will ensure a good decoupling between the voltage divider and its load, the presented acquisition system.

2.2 Requirements for CLIC

The complete measurement system consists of a high-precision high-voltage divider, able to convert $150\,kV$ pulses into $10\,V$ pulses [34], and a high-speed high-repeatability acquisition system. However, the interest of this work is limited only to the acquisition system; as a matter of fact, all the contribution of the upstream voltage divider are neglected so far, focusing only on the custom analogue front-end and the digitizer.

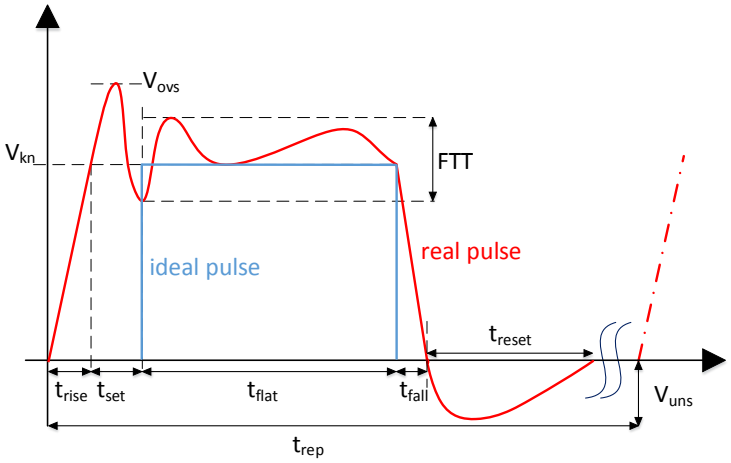

Figure 2.1 – Pulse Parameters Definition.

2.2.1 Pulse-to-Pulse Repeatability

The *Pulse-to-Pulse Repeatability* (PPR) is defined as (Fig.2.2):

$$PPR = max|V_{i,j} - V_{i,j+1}| \tag{2.1}$$

By considering two consecutive pulses flat-tops and their instantaneous voltage values in the $same$ (in equivalent time) sampling instant i within the waveform flat-top (Fig.2.2), $V_{i,j}$ and $V_{i,j+1}$, the main goal of the measuring system is to verify that:

$$PPR \leq PPR_{max} \tag{2.2}$$

ANSI/NCSL Z540-1-1994 states: (i) "*The laboratory shall ensure that calibration uncertainties are sufficiently small so that the adequacy of the measurement is not affected*" and (ii) "*Collective uncertainty of the measurement standards shall not exceed 25% of the acceptable tolerance*" [35], defining the Test Uncertainty Ratio (TUR) as 1 : 4. As a consequence, in order to adequately characterize the pulses with repeatability tolerance (PPR_{max}) e.g. of $\pm 100\,ppm$, the target repeatability of the measurement system should be better than $\pm 25\,ppm$.

2.2.2 The Acquisition System

The project CLIC of CERN requires the repeatability specification to be respected only during the pulse flat-top, for the range of frequencies ($1\,kHz, 5\,MHz$) [14]. To prove pulse-to-pulse

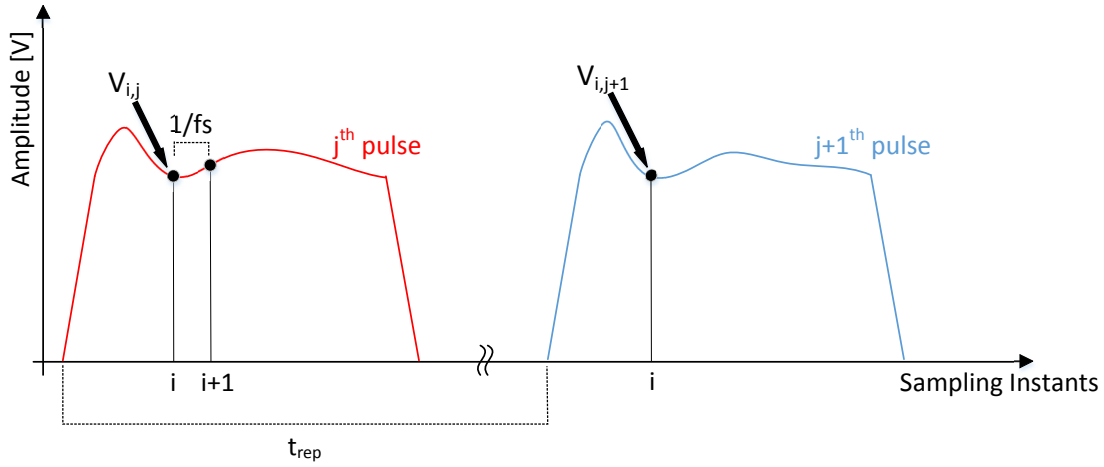

Figure 2.2 – Pulse-to-Pulse Repeatability Definition.

repeatability up to 5 MHz, the acquisition system has to sample at least at a rate of 10 MS/s according to the Nyquist criterion. In addition, if the acquisition system has a suitable stability within the repetition period of the pulses train (20 ms), the only factor that could affect PPR is noise (including quantization noise). By assuming a known distribution for the system's noise, a statistical relation between RMS noise and peak-based PPR exploits the concept of confidence interval (such as usual for type-A uncertainty in the ISO Guide of Uncertainty [20]). Furthermore, the resolution is often used as the first-approach index for evaluating the suitability of an instrument for a measurement. In this case, an instrument with an LSB greater than 25 ppm cannot ensure a PPR better than 25 ppm.For taking into account the actual non-ideality of the acquisition board, the $effective\ resolution$ in terms of $ENOB$ is considered (as usual in experimental physics under suitable assumptions about the actual quantizer model underlying the $ENOB$ definition). Under these hypotheses, the specification on repeatability can be translated into a corresponding constraint on noise. In this case, for a direct sampling of the pulse with an input range of $(0,10)\,V$, a necessary (but not sufficient) condition to assess signal variations in the order of 25 ppm is:

$$LSB = \frac{InputRange}{2^{ENOB}} = \frac{10V}{2^{ENOB}} < 25\,ppm = 250\,\mu V \iff \tag{2.3}$$
$$\iff ENOB > 15.3$$

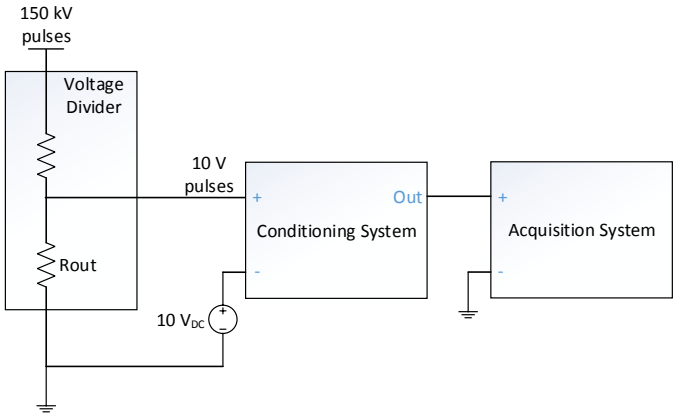

Figure 2.3 – Reference Measurement System - Common *Ground* Is Represented In Order To Simplify The Diagram.

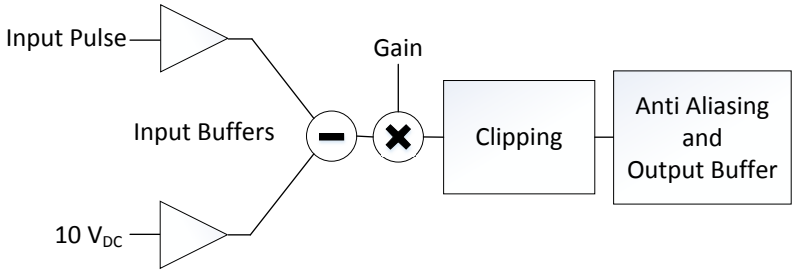

Figure 2.4 – Analogue Front-End Block Diagram.

2.3 Analogue Front-End

2.3.1 Basic Ideas

Nowadays, state-of-the-art acquisition systems on the market, operating at sampling rates equal or higher than 10 MS/s with a full scale of at least 10 V, do not exceed 14 nominal bits. Conversely, acquisition boards (such as NI-PXI-5922 from National Instruments) reach also 15 MS/s with a nominal resolution of 16 bits, but with a maximum input range of $\pm 5\,V$. This does not allow direct measurements of the 10 V pulses, therefore an analogue pre-conditioning front-end is needed. The basic idea is to conceive a front-end that subtracts the nominal value of the flat-top from the pulse and amplifies the resulting signal (Fig. 2.3). This allows the requirements of the digitization to be relaxed, by amplifying the most significant part of the input signal, the pulse flat-top. As a matter of fact, the repeatability specification (PPR) has to be verified only during the flat-top of the pulse; by placing the flat-top around zero, the analogue front-end improves the dynamic range of the digitization system. However, this conditioning circuit introduces a certain amount of noise, much higher than the quantization noise of the acquisition board which needs to be carefully minimized in the design.

2.3.2 Concept Design

The architecture of the front-end is outlined in Fig.2.4. The upper input buffer provides very-high input resistance to the preceding high-voltage divider, while the lower buffer centers the 10 V pulse flat-top around zero, in order to improve the dynamic range of the digitization. The subsequent gain stage amplifies the pulse flat-top, in order to best fit the acquisition board range $\pm 5\,V$. The clipping stage avoids saturation of the subsequent acquisition board input circuitry. This ensures all the devices of the circuit work in their linear region of operation, in order to assure their long-term performance. The range $\pm 5\,V$ is used because the $\pm 1\,V$ is not compatible with the adopted clipping strategy. In fact, clipping with levels as low as $\pm 1.25\,V$ is unfeasible owing to the over-voltage handling of the NI PXI-5922, that shows an unexpectedly long recovery time. Lower clipping rails would reduce the useful range and give rise to high non-linearity arising from the diodes behavior in the clipping region. With a $\pm 5\,V$ full-scale, the clipping levels are set to about $\pm 4.7\,V$ dedicating a useful range of $\pm 2.5\,V$ for the flat-top. The flat-top tolerance of about $85\,mV_{pp}$ is fit into the $\pm 2.5\,V$ range by means of a total amplification of about $50\,V/V$.

2.3.3 Physical Design

A circuit performing the above mentioned tasks is depicted in Fig.2.5. The overall gain of about $50\,V/V$, chosen for the above mentioned reason, is realized by two separated stages since no adequately low-noise operational amplifiers have a bandwidth of at least $5\,MHz$ for such gain. In the proof demonstrator the two input signals are firstly filtered through two simple RC low-pass filters in order to reduce the input noise (indeed the final version of the system will be equipped by the mentioned interface to the voltage divider discussed in 8.0.5); the $10\,V_{DC}$ channel is heavily filtered ($16\,Hz$) whereas the input pulse channel needs to be wide-band ($20\,MHz$). The two buffers (model OPA627 of Texas Instruments) have the following characteristics:

- Supply voltage range up to $\pm 18\,V$ ($\pm 15\,V$ rails were used in order to have an input voltage range of at least $\pm 10\,V$)
- High input resistance, in order to minimize input bias current ($10\,pA$ is the maximum input bias current specified on the datasheet);
- Low input capacitance ($7\,pF$ specified on the datasheet), in order to not affect the compensation of the voltage divider (taking into accout also the capacitance of the long connection cables in the order of hundreds of pF).
- A current noise spectral density of $2.5\,fA/\sqrt{Hz}$ and a voltage noise of $4.5nV/\sqrt{Hz}$. At to date, the high-voltage divider has not been designed yet at CERN by the CLIC Team. Thus, the actual value of its lower-arm equivalent resistance is not available. In any case, even if an equivalent resistance of 100 $k\Omega$ is assumed, a voltage noise of $0.25nV/\sqrt{Hz}$ is achieved on the buffer, still negligible with respect to its voltage noise.

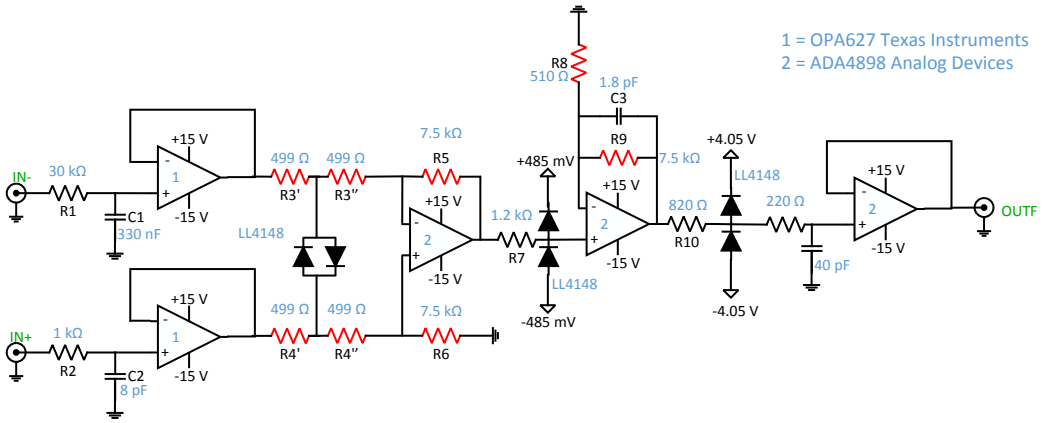

Figure 2.5 – Analogue Front-End Schematic.

- Very good dynamic performance, in order to have a bandwidth of at least 5 MHz, in particular for the positive input buffer (16 MHz at gain of 1 is declared).

Two fast diodes (model LL4148) in anti-parallel clip the input differential signal in order to not saturate the difference amplifier (nominal gain of 7.5) when the signal on the inverting input is zero (i.e., without pulse). In this stage, the input resistors (R3 and R4) are split in order to limit the current flowing through the diodes when they are active; in particular, $R3^{'}$ and $R4^{'}$ limit the current before and after the flat-top of the pulse. $R3 = R3^{'} + R3^{''}$ together with $R5$, as well as $R4 = R4^{'} + R4^{''}$ together with $R6$, set the gain during the flat-top (when the diodes are OFF). The voltage drop across the diodes, when they are ON, is conversely amplified by the ratio $R5/R3^{''} = R6/R4^{''}$. Therefore, by choosing $R3^{'} = R3^{''}$ and $R4^{'} = R4^{''}$, the flat-top gain is half of the gain seen by the voltage drop across the diodes when they are active. Obviously, the same clipping operation has to be repeated at the output of the same stage. Also for this stage, the same fast diodes were chosen (model LL4148). The clipping voltage is conveniently set by means of two opposite rails in this stage. A non-inverting stage (nominal gain of 6.9) was chosen owing to its high input impedance, making resistor R7 ininfluent for the gain setting. Two identical amplifiers (model ADA4898 of Analog Devices) were chosen for the two amplifying stages owing to their excellent performance in terms of:

- Input noise (0.9 $nV/\sqrt{Hz}$ declared);
- Bandwidth (65 MHz at gain of 1 allows the 7.5 amplification assuring more than 8 MHz bandwidth);
- Supply voltage range of $\pm 15\,V$ allowed in order to have an input voltage higher than 10 V.

Finally, after the second amplification stage, a last pair of clipping diodes (same model LL4148) are needed to avoid over-range in the input stage of the subsequent acquisition board (the

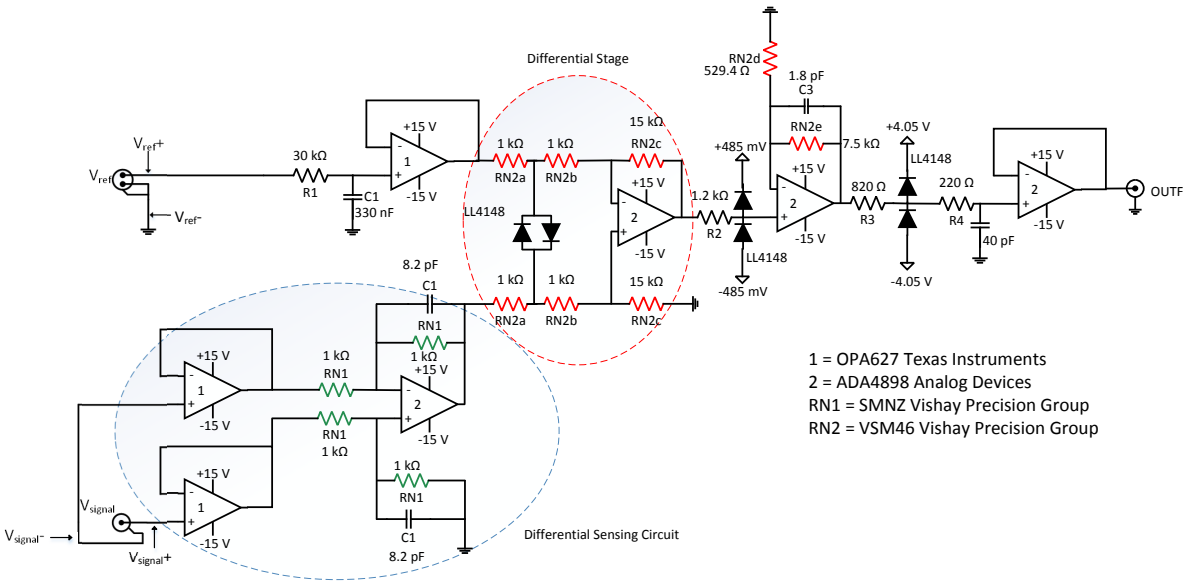

Figure 2.6 – The Enhanced Analogue Front-End

two rail voltages can be set according to the input stage limits). The last consideration is about the requirements on resistor quality; in Fig.2.5, all the resistors in red affect the overall gain stability and $CMRR$ [36]. An array of 8 matched precision resistors can guarantee at the same time high gain stability (low temperature coefficient can easily be achieved) and high $CMRR$ (low relative tolerances down to 0.01% can be specified). However, more stringent performance requirements arose from deeper investigations on the actual working conditions of the system and from $CLIC$ requirements evolution. In particular, if an adequate $CMRR$ value is not achieved, the differential stage (red dotted circle in Fig.2.6) would not perform an effective subtraction. Furthermore, given the harsh work environment, the dependency of system performance on environmental changes and conditions must also be investigated.

The final version of the reference acquisition system is composed of an improved analogue front-end (Fig.2.6), and the state-of-the-art acquisition board $NIPXI-5922$.[5]

2.4 Design Enhancement

The new performance requirements were satisfied mainly by using the two circuits highlighted by dotted circles in Fig.2.6. The first circuit, highlighted in red, exploits an array ($RN2$) of matched resistors with 0.01% of relative tolerance with the following advantages:

- considerably enhance $CMRR$ [36] by reducing the possible unbalance of the two branches of the differential stage (red dotted circle in Fig.2.6).
- stabilize gain by integrating all the temperature-sensitive gain-setting resistors into the same chip.

The second circuit, highlighted in blue, uses a differential sensing circuit on the input stage, with the following twofold advantages:

- rejection of the common-mode voltage between the analogue front-end and the upstream voltage divider, [5] which could arise from the ground loop between the two different grounds, by means of another high-precision resistors network $RN1$ with 0.01% of relative tolerances.
- complete decoupling of the voltage divider from the analogue front-end by means of two input buffers.

3 The On-line Acquisition System

3.1 Overview

In this chapter, the design of a $\pm 18\,ppm$ repeatable digitizer, with real-time delay less than $1.2\,\mu s$ and $0-11\,V$ full-scale range, is presented.

In particular, in section 3.2, the system requirements are defined, whereas in section 3.3, the working principle is discussed. In section 3.4, the design choices are detailed and the circuital realization of the prototype produced at *CERN* is presented. Then, in Chapter 6 (section 6), simulation tests aimed at verifying the design choices are presented. Finally, in Chapter 9 (section 10), the experimental results of an experimental proof of principle are reported and discussed.

3.2 Requirements for CLIC

In a real-time control of power converters for the last generation of particle accelerators, a digital control loop is exploited to guarantee the requested performance of the power system. In this section, the requirements of the real-time measurement sub-system for digital control loop are discussed with the specific case study of the new linear electron-positron particle accelerator currently under study at *CERN*, the Compact LInear Collider ($CLIC$) [11].

$CLIC$ will allow collisions up to several TeV, exploring energy regions never reached before, thanks to its unprecedented combination of high energy and experiment precision. In order to reach the desired energy level, together with reasonable power consumption from the electrical grid, $CLIC$ power converters [13] are demanded to deliver a pulsed power repeatable in the order of few tens of ppm [14]. To do that, a high-voltage modulator is currently under design by the laboratory for high-power electronics at *ETH Zurich (CH)* [16] and the *LEEPCI* Laval (CA) [17]. The latest topology of the ETH design is depicted in Fig.3.1. The modulator is composed by a charging system which, after a pre-charge phase, accumulates energy from the grid obtaining a nominal 3 kV output voltage. The switching unit allows the stored energy to be

released during 140 μs, obtaining a pulse train on the primary side of a split-core transformer at a repetition rate of 50 Hz. The charging system output voltage is also regulated by an active bouncer for mitigating the effect of discharge of the capacitors bank during the pulses. Finally, on the secondary side, the pulses are amplified up to 180 kV directly feeding the klystrons. A high-voltage divider [34] is used to convert the 3 kV voltage into 10 V in order to be handled by a suitable real-time digitizing system. In this context, the system measures and provides a suitable adjustment value for the switching unit input voltage sketched in Fig.3.2.

3.2.1 Measurand

The measurand signal is characterized by different phases: (i) an *initial ramp up*, in which the charging system reaches the nominal voltage, (ii) a $pulse$, during which the modulator generates the pulse ideally keeping the voltage constant, and (iii) a $recharge$, in which the nominal voltage out of the charging system is restored. The full performance specification concerns only the *Pulse* phase, though the measurement of the complete signal is required. This poses a crucial challenge on how to guarantee the required performance on the high-state, during the *Pulse*, while measuring a wide-range signal in real time. Furthermore, the switched-mode power converter generates a switching noise superposed on the measurand which must not jeopardize the final performance of the measurement system.

3.2.2 Repeatability

The real-time measurement system will be used to guarantee a modulator repeatability in the order of ± 50 ppm of full-scale during the pulse. The particular application, discussed in [5], defines a Pulse-to-Pulse Repeatability (PPR) as:

$$PPR = max|V_{i,j} - V_{i,j+1}| \tag{3.1}$$

where $V_{i,j}$ and $V_{i,j+1}$, sketched in Fig.3.3, are the instantaneous voltage values in the *same* (in equivalent time) sampling instant i between two consecutive pulses on the secondary side of the modulator, namely j^{th} and $j^{th}+1$. For the charging system this definition applies to the *Pulse* phase. In addition, to be able to properly measure and correct variations of 50 ppm, the

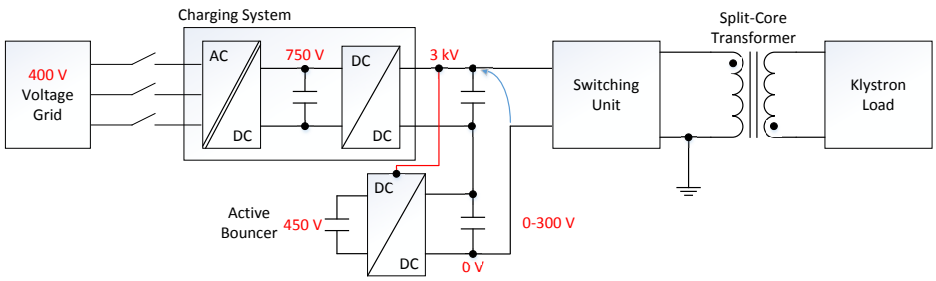

Figure 3.1 – Topology of the High-Voltage Modulator under design at ETH Zurich

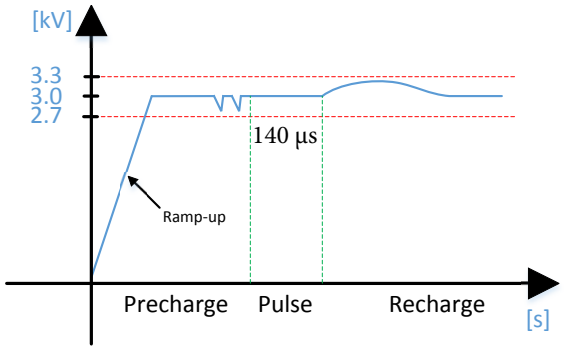

Figure 3.2 – Switching Unit Input Voltage

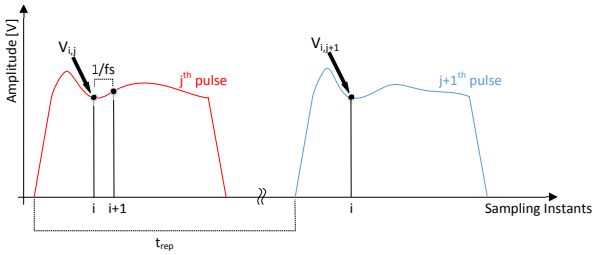

Figure 3.3 – Pulse-to-Pulse Repeatability Definition.

system should have better repeatability performance. Thus, target instrument PPR was set to better than 50 ppm. It has been studied in [5] that if the instrument has a suitable stability within the pulses period, (20 ms), noise is the only factor affecting repeatability, thus all long term effects can be neglected (e.g. temperature drift).

3.2.3 Throughput and Bandwidth

The digital control loop will run at a rate $f_{loop} = 600\ kS/s$ and the instrument must deliver one sample at each control loop period ($throughput = f_{loop}$).

3.2.4 Delay

Delay is one of the most important parameters of a digital control loop. For this system, a total group delay $d < 1.2\ \mu s$ is specified for the whole measurement chain sketched in Fig.3.4 (high-voltage divider, analogue front-end, ADC, and digital filtering). In the following, for the sake of simplicity, the group delay at $f = 0\ Hz$ is called delay. This is a challenging specification when combined with an overall bandwidth of less than 300 kHz, as required by $CLIC$ application.

In Table 3.1, the main requirements for the real-time measurement system are summarized.

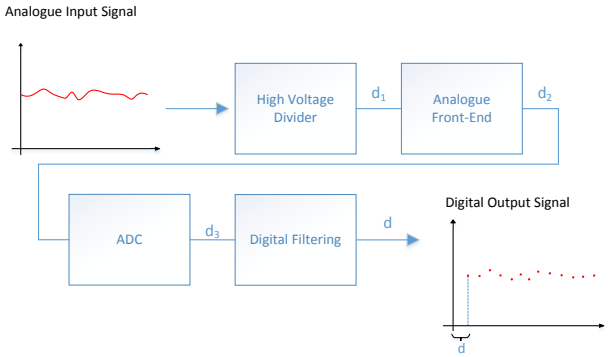

Figure 3.4 – Definition of Delay in a Power Converter Real-time Data Acquisition

Table 3.1 – Main Requirements

Parameter	Symbol	Value
Repeatability during Pulse	Rep_p	50 ppm
Repeatability elsewhere	Rep	$< 1\,\%$
Throughput	T	600 kS/s
Bandwidth	BW	$> 200\ kHz$
Delay	d	$< 1.2\ \mu s$

3.3 Design

In this section, the design choices of the proposed instrument (Fig.3.5) are discussed with respect to the defined requirements.

3.3.1 Basic Principle

The 3 kV voltage is converted into 10 V by means of a high-voltage divider [34]. During the pre-charge phase, where no particular precision is required ($< \pm 1\,\%$), the switch S_2 allows subtracting the input signal from itself in order to obtain a *zero-signal* (ideally) on the upper branch of Fig.3.5. At the same time, a wide-range ADC, (ADC_2) digitizes the input signal

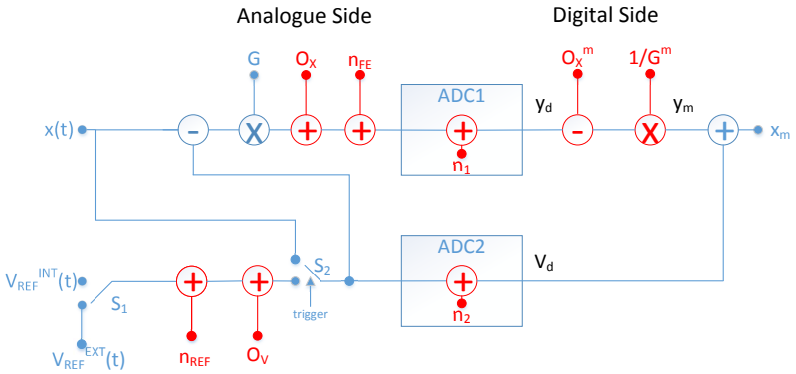

Figure 3.5 – Measurement System Block Diagram

obtaining a coarse measurement of the initial ramp. When the ramp is over (this event will be identified by an external trigger provided by ETHz modulator), the switch commutates toward an internal reference 10 V_{DC} voltage. This is subtracted from the signal in order to center its high-state around zero and then amplify only the part where high-precision is required by a factor G to best fit ADC_1 range. Down-stream of these two operations, unwanted offset (O_x in Fig.3.5) and gain errors will arise from all the possible analogue components. All the nonideality effects will be processed digitally in order to properly reconstruct the original signal. A switch allows an external 10 V_{DC} reference ($Vref_{EXT}$) to be connected, for a direct calibration of the internal generated reference $Vref_{INT}$.

3.3.2 Full-Signal Reconstruction

During normal working conditions, both the conditioned signal and the internal reference DC voltage are digitized (y_d and V_d, respectively, in Fig.3.5). These two signals are affected by the noise of (i) the front-end (n_{FE}), (ii) the 10 V_{DC} reference (n_{REF}), and (iii) the two $ADCs$ quantization, respectively n_1 and n_2. In order to reconstruct the original input signal, offset and gain introduced into the analogue path as a whole have to be measured and digitally compensated. At this point, the resulting signals y_m and V_d are the digitized product of the original signal x:

$$\begin{aligned} x_m = \frac{[x-(V_{REF}^{INT}+n_{REF}+Ov)]\cdot G+Ox+n_{FE}+n_1-Ox^m}{G^m} + \\ +V_{REF}^{INT}+n_{REF}+Ov+n_2 \end{aligned} \tag{3.2}$$

Gain and offset can be accurately measured so that $Ox^m = Ox$, $G^m = G$ (full uncertainty estimation not discussed here) and:

$$\begin{aligned} x_m = x - V_{REF}^{INT} - n_{REF} - Ov + \frac{n_{FE}+n_1}{G^m} + \\ +V_{REF}^{INT} + Ov + n_2 = x + \left(\frac{n_{FE}+n_1}{G^m}\right) + (n_{REF}+n_2) \end{aligned} \tag{3.3}$$

where all the deterministic errors have been already compensated.
In conclusion, particular attention should be paid to (i) accurately measure gain and offset for proper compensation, (ii) realize a low-noise front-end in order to keep n_{FE} as low as possible, (iii) heavily filter n_{REF}, and (iv) use high-resolution $ADCs$ such that $\frac{n_1}{G}$ and n_2 meet the specs.

3.3.3 Sampling and Filtering Strategy

The digital control loop will run at 600 kS/s. To mitigate the ripple produced by power switching, an oversampling [37], filtering, and decimation strategy was adopted in this design. The sampling rate is defined as $f_s = N \cdot 600\ kS/s$, where N is the oversampling ratio. In order to not produce significant aliasing, the instrument must be equipped with anti-aliasing

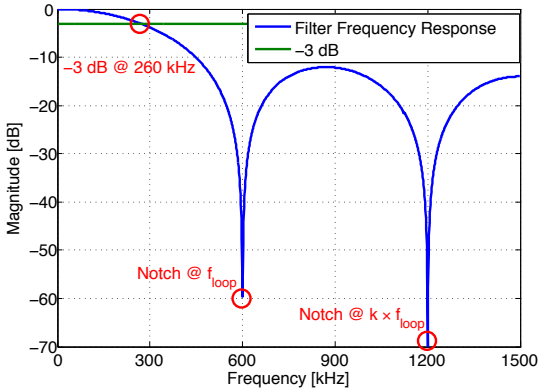

Figure 3.6 – Frequency Response of the Average 4^{th} FIR filter

analogue and digital filters. Analogue filtering have to mitigate the effect of noise in the range of frequencies folding in base-band (above Nyquist frequency). In the current application, no relevant noise components are expected at high frequency (except from swithcing harmonics), thus an attenuation in the order of 10 dB at $f_N = N \cdot f_{loop} - \frac{f_{loop}}{2}$ was considered for the design of the analogue front-end. It is worth noting that the upstream high-voltage divider, assumed as a first order filter at 1 MHz, already plays a role in the analogue anti-aliasing filtering strategy, accordingly introducing additional attenuation at f_N. For digital filtering, a simple average filter, belonging to the class of linear-phase *FIRs*, is foreseen. The frequency response of a 4^{th} order filter, depicted in Fig.3.6 ($N = 5$ => sampling rate $f_s = 3\ MS/s$, and $f_N = 2.7\ MHz$) shows a notch at 600 kHz (and harmonics), with the important advantage of heavily mitigating the switching ripple of the power stage at those frequencies. The group delay introduced by this filter can be estimated as:

$$d_{digital} = \frac{N-1}{2N f_{loop}} \approx 670\,ns \tag{3.4}$$

where N is the number of coefficients. In this case, a group delay in the order of 670 ns is calculated.

3.3.4 ADC Noise vs Analogue Noise

Equation (3.3) states the dependence of the reconstruction quality of x on both the analogue (n_{FE} and n_{REF}) and the digital noise (n_1 and n_2). In [8], an analytical model for describing the statistical distribution of the worst-case PPR, namely the Worst-Case Repeatability (WCR), of an instrument affected by an Additive White Gaussian Noise ($AWGN$) was found. This happens typically when the analogue noise $AWGN$ is adequately dominant with respect to the quantization noise of the ADC, assumed to be uniformly distributed between $\frac{-\Delta}{2}$ and $\frac{\Delta}{2}$, where Δ is the *ADC LSB*. On the contrary, if the quantization noise is dominant with respect to analogue noise, the WCR cannot be higher than Δ itself.
In the following, the dominating noise contributions (analogue and digital) are discussed.

n_1

Quantization noise of ADC_1, which has to digitize the *high-state* signal. The high-speed ADC $AD7625$, declares a $SINAD$ of 92 dB. The Effective Number Of Bits ($ENOB$) is calculated as:

$$ENOB = \frac{SINAD - 1.76}{6.02} \approx 14.9 \tag{3.5}$$

The signal voltage swing $V.S.$ is $\pm 4\ V$, thus the LSB of ADC_1, denoted by Δ_1, can be obtained as:

$$\Delta_1 = \frac{V.S.}{2^{ENOB}\, G \times 10\ \mu V} \approx \frac{246\ \mu V}{40\ \mu V} \approx 6.2\ ppm \tag{3.6}$$

n_2

Quantization noise of ADC_2 which has to digitize a 10 V_{DC} voltage. As an example, the 18-bits $AD7634$ can be triggered to sample at 600 kS/s over an input voltage range of $10\,V$. In this conditions, $AD7634$ has a $SINAD$ of 100 dB, thus its $ENOB$ specification turns out to be ≈ 16.3 from (3.5) and, consequently, the LSB is about $\Delta_2 \approx 12.4\ ppm$.

Analogue Noise

n_{REF} is the noise arising from the DC reference voltage to be subtracted from the original signal. Since no bandwidth is required for this branch of the front-end, this voltage can be heavily filtered in order to reduce n_{REF}. Finally, n_{FE} is the noise of the analogue front-end. A low-noise solution for the front-end was indeed one of the main design constraints.

Worst-Case Repeatability

At the required bandwidth, the front-end's noise is expected to be lower than the quantization noises of the two ADCs. Under the assumption of uniformly-distributed quantization noises for the two ADCs, a deterministic superior bound for the WCR can be estimated. In fact, from (3.1), the worst-case condition is verified when the j^{th} acquisition is affected by the quantization noise $\left(\frac{\Delta_1}{2} + \frac{\Delta_2}{2}\right)$ and the $(j+1)^{th}$ by $-\left(\frac{\Delta_1}{2} + \frac{\Delta_2}{2}\right)$. Thus, the superior bound can be assessed as:

$$WCR = \Delta_1 + \Delta_2 \approx 18.6\ ppm, \tag{3.7}$$

which is comfortably lower than the 50 ppm requirement. It is worth noting that, even if the low-noise feature of the analogue front-end is not critical in this application, by modifying the analogue filters parameters, the instrument can be adapted to applications where wider bandwidth is required, by accordingly taking advantage of the low-noise front-end.

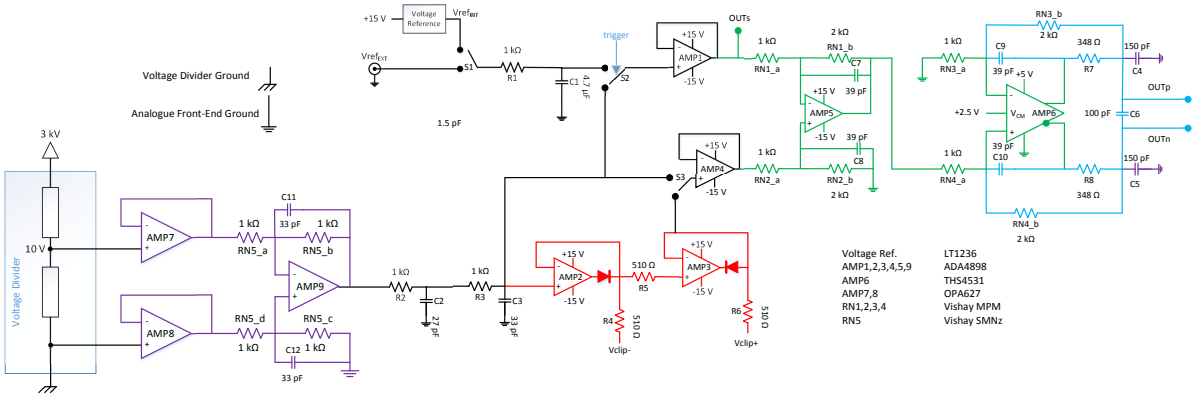

Figure 3.7 – Analogue Front-End Schematics

3.4 Physical Design of the Analogue Front-End

In Fig.3.7, the schematics of the proposed analogue front-end is depicted. Each stage described in the following is highlighted with different colors.

3.4.1 Input Stage

Reference Voltage Input

On the upper branch (in black in Fig. 3.7), the switch $S1$ allows either the external or internal 10 V reference voltage to be selected. The internal reference voltage ($Vref_{INT}$) is realized by means of the Linear Technologies voltage reference $LT1236$. The low-pass filter R_1C_1 has a cut-off of about 30 Hz. The switch $S2$, depending on the particular phase of the input signal (pre-charge or pulse) selects the corresponding line to be subtracted from the signal. The input signal is then buffered by $AMP1$. On the lower branch, a 2^{nd} order low-pass filter ($R_2C_2R_3C_3$) represents the first stage of the anti-aliasing filter described in 3.3.3 (the stage "zero" of the anti-aliasing being the Voltage Divider itself).

Signal Input

A differential sensing circuit is used on the signal input. The circuit, already discussed in [5] and used in [38], is depicted in Fig.3.7 in violet and aims at solving twofold issues:

- Reject the Common Mode Voltage between acquisition system and voltage divider arising from the ground loop related to separated grounds, by means of a suitable difference amplifier (ADA4898). Indeed voltage divider and measurement system will be installed into two separate racks, therefore the relative ground voltages might be

significantly different;

- Decouple the voltage divider from the analogue front-end by means of two input buffers (again ADA4898).

3.4.2 Clipping Stage

The cascade of two $ADA4898$ in super-diode configuration realizes a fast clipping circuit to protect the input stage of ADC_1 [39](in red in Fig.3.7). During the pre-charge phase the low-side clipping is deactivated by setting the voltage $Vclip-$ to ground. Switch $S3$ allows disabling the clipping circuit.

3.4.3 Differential Stage

Another *ADA4898* in difference configuration is used to translate the input signal (lower branch in Fig.3.7) around zero by subtracting the reference voltage (upper branch in green in Fig.3.7), and to apply a gain $G_1 = 2\ V/V$. Finally, a Fully Differential Amplifier (model $THS4532$) performs single-ended to differential conversion and amplifies the signal by a factor $G_2 = 2\ V/V$. It is worth noting that two separate differential stages are needed since the *FDA* only allows a unipolar supply voltage of, at most, 5 V. This means that it cannot handle 10 V input signals. The resistor networks $RN_{1,2,3,4}$ are the Vishay MPM series, which guarantee a good gain accuracy, given the low-tolerance resistors of 0.01 %. In the final engineered version of the analogue front-end the Vishay resistor network $VSM46$ will be used to guarantee both high-CMRR [36] and temperature stability [38]. $VSM46$ is composed by 8 matched resistors with (i) low relative tolerances (0.01 %) and (ii) low temperature coefficient (0.1 $ppm/°C$). These characteristics are very important in this design, in fact:

- Their ratio keeps constant while temperature changes (they are matched), allowing the gain and offset drift to be heavily reduced.
- They avoid degradation of $CMRR$ due to unbalances of the two branches of the two amplifiers [36].

3.4.4 Output Stage

The last stage (light blue in Fig.3.7) completes the analogue anti-aliasing filter described in 3.3.3. In Fig.3.7, the reported values for all the resistors and capacitors involved in the filter are chosen in order to have at least 10 dB of attenuation at $f_N = 2.7\ MHz$.

PART 3 - NUMERICAL RESULTS

4 The Worst-Case Uncertainty Analytical Model

4.1 Repeatability Case Study at CERN

At CERN, a new particle accelerator is currently under study, the Compact LInear Collider ($CLIC$). This new electron-positron collider would provide significant fundamental physics information even beyond that available from the Large Hadron Collider (LHC) as a result of its unique combination of experimental precision and high energy [11]. The accelerating principle relies on energy transfer from a drive beam, which is generated in a classic linear accelerator using more than 1600 klystrons [40] in synchronized pulsed mode for RF power production, to a main beam. The nominal drive beam energy can only be reached with more than 1,000 klystron modulators, thus, the overall efficiency of the klystron and the modulator has to be maximized in order to confine the overall power consumption within an acceptable range [11],[14].
In Table 1, the CLIC klystron modulators pulses specifications were reported. The very challenging requirements for the RF power quality, derived directly from the accelerator performance specifications, are met by imposing a flat-top repeatability (according to the related standard [41] the flat-top is the pulse level), down-stream of the modulators, better than $\pm 100 ppm$. A specifically designed reference acquisition system [5] (Fig.4.1) was proven experimentally capable of assessing this performance. In this context, the focus is mostly dedicated to the Worst-Case Repeatability (WCR) which is defined as:

$$WCR = max_i |V_{i,j} - V_{i,j+1}|. \tag{4.1}$$

$V_{i,j}$ and $V_{i,j+1}$ (Fig.1.1) are the instantaneous voltage values at the *same* (in equivalent time) sampling instant i within two consecutive pulses flat-tops (j and $j+1$). The difference between WCU and WCR is analogous to the difference between *precision* and *repeatability* as defined in the International Vocabulary of Metrology (VIM) [42]. In particular, according to the approach of the VIM, the repeatability can be seen as the most restrictive case of the uncertainty, namely when the operating conditions are not varying during the measurement. In addition, within this case study, the general WCU definition, discussed in 1.2.1, is applied

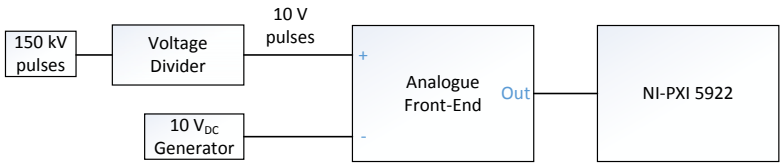

Figure 4.1 – Reference Acquisition System Block Diagram.

Table 4.1 – Reference Acquisition System Specification

Reference Acquisition System Specification		
Parameter	**Symbol**	**Value**
Worst-Case Repeatability	WCR	$< 25\,ppm$
Worst-Case Repeatability Mode	M	$\approx 15\,ppm$
RMS Noise	σ	$\approx 3\,ppm$
Bandwidth	BW	$\approx 5\,MHz$
Maximum Sampling Frequency	f_s	$15\,MS/s$
Linearity Error	ϵ_L	$< 2\,ppm$
Common Mode Rejection Ratio	$CMRR$	$> 86\,dB$

to the particular case of a train of pulses.

By assuming the measurand pulses as perfectly repeatable, the differences defined in (4.1) should be exactly equal to zero. However, even under this assumption, the WCR measurement is affected by the instrument noise. In fact, the reference acquisition system developed at CERN has suitable stability within the repetition period of the train of pulses ($20\,ms$) [5], thus its noise is the only factor affecting WCR, because all the *long-term* effects (e.g. temperature drift) can be neglected. In particular, its analogue front-end exploits a very low-noise difference amplifier to implement the difference between the input pulse and a DC voltage reference set at the nominal amplitude of the pulse itself (it also introduces an amplification down-stream of the difference operation). This allows the acquisition board to acquire only the interesting part of the pulse, the flat-top, by accordingly taking advantage of its high-resolution. In Table 4.1, the full specifications of the reference acquisition system [5] are reported.

The theory reported in the last section can be applied to this experimental case study; in fact, the definitions of WCU in (1.1) and WCR in (4.1) (symbols are the same on purpose), are exactly equivalent: the only difference is that in the $CLIC$ context, the measurements are taken under repeatability conditions [42].

4.1.1 Noise Standard Deviation

From the WCR definition (4.1), the differences of two flat-tops samples are distributed as Y_i. In addition, under the ideal hypothesis of perfectly repeatable flat-tops, two counterparts samples will have exactly the same value. However, the acquisition system will introduce some additive noise on the flat-tops (mostly due to the analogue front-end [5]).

4.1.2 Number of Samples

Each pulse has a Flat-Top Duration (FTD) of 150 μs (Table 1) and it is acquired at a Sampling Rate (SR) of 15 MS/s. By considering the flat-top samples as iid random variables, the *numerosity* N_s should be therefore chosen as:

$$N_s = FTD \cdot SR = 2250 \tag{4.2}$$

4.1.3 Number of Observations

In the context of the case study, a pulse has a repetition period of 20 ms; the number of observations N_o (sample size) is therefore strictly related to the time duration of the acquisition (observation time). As an example, if the WCR has to be verified over 1 s, 50 pulses have to be acquired. This parameter should be chosen according to the WCR (or, in general, WCU) specification requested by the specific application.

4.2 Numerical Results

In this section, a simulation analysis for (i) validating the assumptions underlying the model, and (ii) characterizing the model at varying its main parameters is reported.

4.2.1 Model Goodness

In the following, two simulation trials in MATLAB proving the effectiveness of the approximated equation (1.13) are reported. Two sets of samples, each of them composed by N_s Normal random numbers, are generated N_o times by the MATLAB's *randn* function for emulating the acquisition of N_o consecutive pulse flat-tops. *randn* is not guaranteed to generate a zero mean sample, or a negligible mean value, therefore this effect is always compensated before further processing. The WCR definition (1.11) is applied to calculate $WCR(N_o)$. The statistical sample as a whole is generated by reiterating the simulation N_{test} times. A χ^2 test [43] is then carried out in order to verify that the data in the sample under study are distributed according to the proposed distribution. The χ^2 test is carried out at a significance level $\alpha = 0.1\%$, in order to control the nonreproducibility rate to usual levels of scientific evidence, as recently suggested in [43]. Compatible results between simulation and experimental tests with the *CLIC* reference acquisition system are obtained by assuming an additive white Gaussian noise with $\sigma = 3.12\,ppm$ of Full Scale as the *underlying* distribution with CDF equal to $F_{Y_i}(z)$ (in [5], the acquisition system's RMS noise was assessed to be equal to 3.12 ppm). In Table 4.2, the model parameters for the simulations are reported.

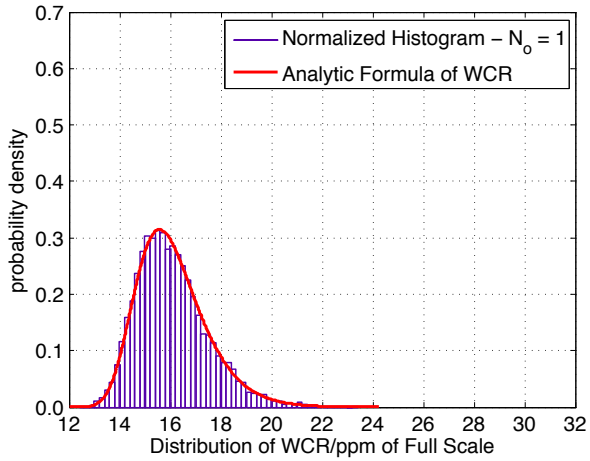

Figure 4.2 – Distribution of WCR for $N_o = 1$ and $N_{test} = 10,000$.

WCR over 2 pulses

For the first simulation trial, the distribution of WCR, estimated with a sample size $N_o = 1$ (corresponding to $N_p = 2$ pulses), is depicted in Fig.4.2, where both the normalized histogram obtained in simulation and the analytical formula (1.13) are shown. A χ^2 test gave not reason to doubt about the validity of the proposed analytical formula, at a significance level $\alpha = 0.1\%$ (the goodness of the fit can be evaluated also visually).

WCR over 180,000 pulses

For the second simulation trial, the distribution of WCR over a sample size $N_o = 180,000$ ($1\,h$ of acquisition) is estimated (Fig.4.3). The comparison with the diagram of Fig.4.2 highlights the dependency of the mode of the distribution on the sample size. In fact, in the first simulation (Fig.4.2), the maximum value among only one pair of pulses was considered, whereas in Fig. 4.3, the maximum value among 180,000 pairs of pulses is represented as a single count in the normalized histogram. This results in a higher mode of the distribution. Also in this case, the proposed model fits the simulated distribution, as confirmed by a χ^2 test at the above significance level $\alpha = 0.1\%$.

Table 4.2 – Model Parameters used in Simulation

Model Parameters		
Parameter	**Symbol**	**Value**
Number of Samples	N_s	2250
Noise standard deviation	σ	3.12 ppm of FS
Test iterations	N_{test}	10,000
$\chi^2 test$ Significance Level	α	0.1 %

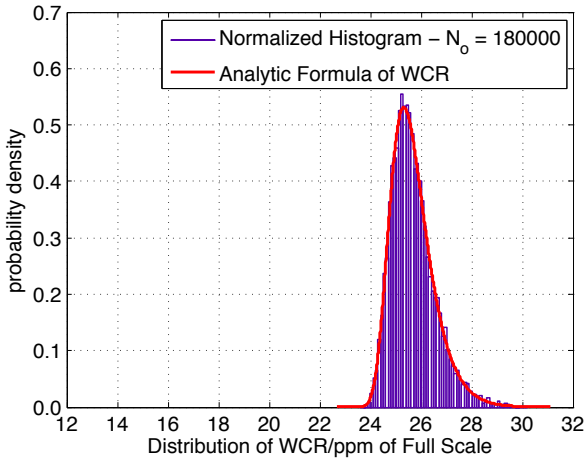

Figure 4.3 – Distribution of WCR for $N_o = 180,000$ and $N_{test} = 10,000$.

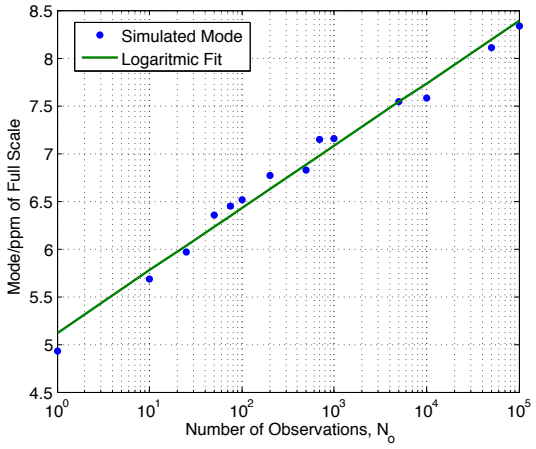

Figure 4.4 – Mode of WCR versus N_o, $\sigma = 1$ ppm of Full Scale

4.2.2 Model Characterization

Once the Once the assumptions underlying the proposed model were validated by simulation, the mode of the WCR distribution can be predicted at varying (i) the sample size, and (ii) the RMS noise.

Mode of WCR versus sample size

In Fig.4.4, the trend of the mode is depicted for N_o ranging from 1 to 10^5 (with $\sigma = 1\,ppm$). However, the model can be generalized for higher σ, for systems with higher noise. A logarithmic dependency of the WCR versus the sample size N_o is also highlighted.

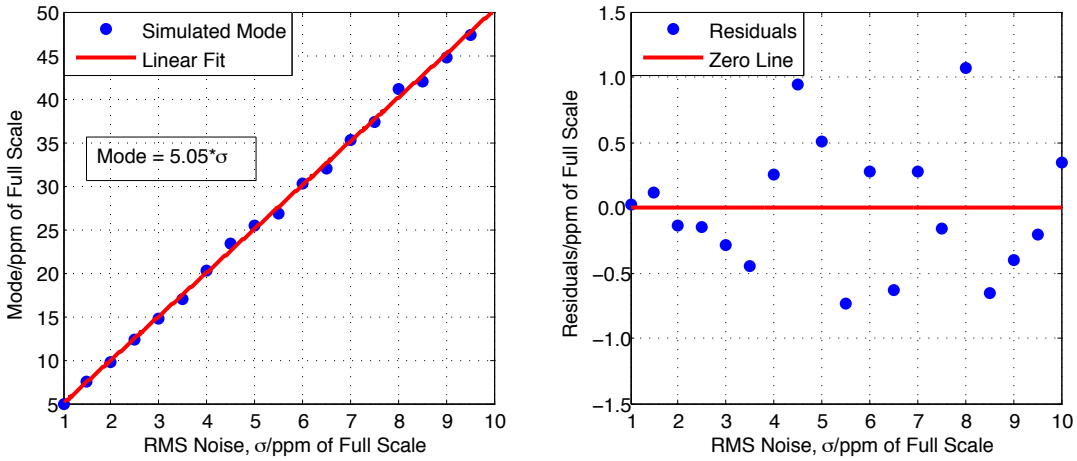

Figure 4.5 – Mode of WCR versus σ (left), Residuals of Linear Fit (right). $N_o = 1$.

Mode of WCR versus RMS noise

The trend of the mode of the WCR distribution versus σ was estimated for $N_o = 1$ (Fig.4.5, left). The linear relation between the two variables is highlighted by the goodness of linear fitting based on Least Squares Errors (LSE), as well as by its residuals (Fig. 4.5, right). In this case, a model without known term was used to consider the limit (ideal) condition $\sigma = 0$ which has to return a mode exactly equal to zero.

5 The Reference Acquisition System

The performance of the analogue front-end was assessed in simulation, by analyzing:

- Amplitude frequency response, in order to verify the required $5\,MHz$ bandwidth (the phase delay was not assessed because not relevant for repeatability measurements);
- Noise, in order to estimate the RMS noise introduced by the conditioning system, directly affecting PPR (according to what already mentioned in 2.2.2);
- Static linearity, in order to verify its impact on the PPR. Conceptually, repeatability is not directly affected by linearity such as statistically defined in the International Vocabulary of Metrology [42]. However, according to the definition of PPR in (2.1, in two consecutive samples the circuit is called to work on close points of its input/output characteristic. A significant differential non-linearity could give rise to a corresponding significant difference in the circuit response to two consecutive samples.
- Settling time, in order to verify that the step response settles within the required time (Tab.1 and Fig.2.1)

5.1 Amplitude Frequency Response

In Fig.5.1, the result of the frequency response simulation is shown. The $-3\,dB$ point is located around $5\,MHz$, therefore the first specification is proved to be achievable.

5.2 Noise Analysis

As already mentioned in section 2.2.2, under the hypotheses of a good system stability within the repetition period of the train of pulses, the system noise is the only factor affecting PPR and its assessment is essential for achieving the required PPR. A behavioral model-based analysis of the analogue front-end allows the RMS value of the noise power spectral density

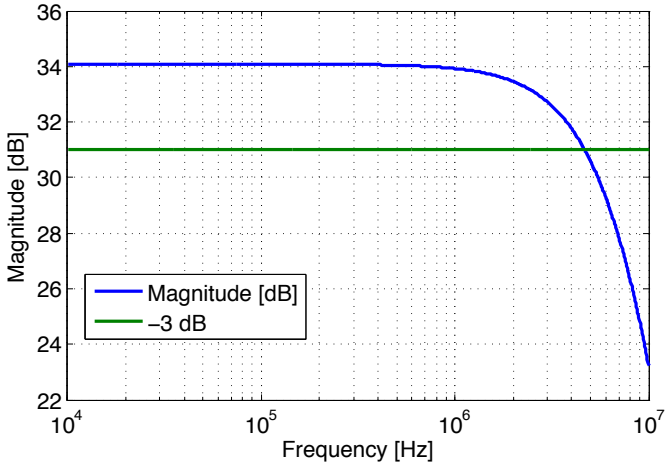

Figure 5.1 – Simulated Amplitude Frquency Response.

(PSD) to be assessed as:

$$N_{rms} = \sqrt{\int_{f_L}^{f_H} PSD(f)df} \tag{5.1}$$

where the integration boundaries f_L and f_H used in simulation are $1\,kHz$ and $100\,MHz$, respectively. Initially, the accuracy of the amplifiers noise model was verified by comparing the results of the noise simulation of each device and the datasheet specification. In Fig.5.2, a RMS noise of about $4.7\,ppm$ Referred To Input (RTI), obtained by PSpice, is shown. This is the amount of noise expected at the input of the acquisition board. The final value of noise of the acquisition as a whole can be assessed by considering the filtering effect of the limited bandwidth of the downstream acquisition board. As an example, the NI-PXI-5922 has a nominal bandwidth of $6\,MHz$ when sampling at its maximum speed of $15\,MS/s$. As a first approximation, the filtering effect of the board can be taken into account by considering the simulation results up to $6\,MHz$ (instead of $100\,MHz$): a RMS value of about $3.1\,ppm\,RTI$ is estimated in this case.

5.3 Linearity

This test allowed the linearity error Referred To Input (RTI), shown in Fig.5.3, to be calculated. By statically varying the differential input, the input-output characteristic can be evaluated and the linearity error calculated as:

$$E_{ppm} = \frac{V_{out} - G \cdot V_{in} - Offset}{G \cdot 10\,\mu V} \tag{5.2}$$

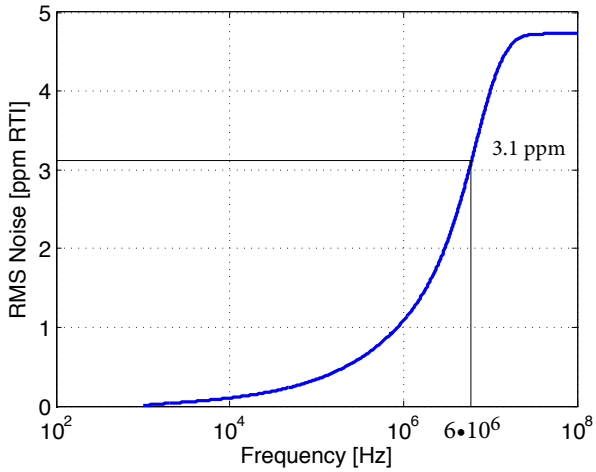

Figure 5.2 – Simulated RMS Noise.

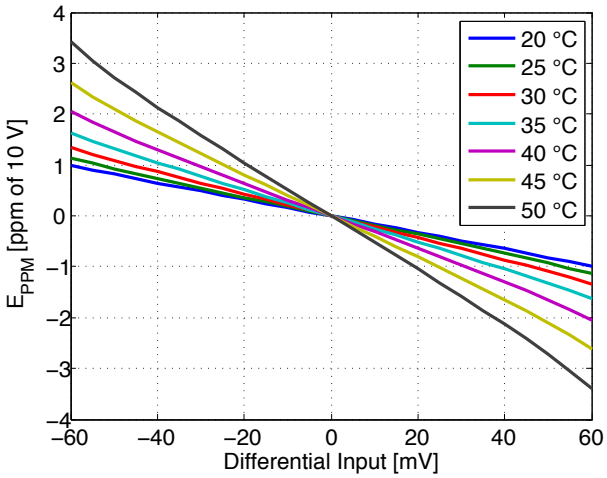

Figure 5.3 – Non-Linearity Curves At Different Temperatures.

The simulation was obtained in Pspice by performing (i) a DC primary sweep from $-FTT/2$ to $FTT/2$ (rigorously from $-42.5\,mV$ to $+42.5\,mV$ but, in order to include some additional margins the input sweep was performed from $-60\,mV$ to $+60\,mV$), and a (ii) temperature secondary sweep from 20 °C to 50 °C in order to obtain the variation of the linearity error with temperature. The maximum error occurs at 50 °C and is less than $4\,ppm$.

5.4 Settling Time

An input step from 0 to 10 V with rise time of 10 ns is applied at the positive input of the analogue front-end (the negative input is connected to a 10 V_{DC} source) by measuring the output transition. Figs.5.4,5.5 show a settling time comfortably shorter than the required $5\,\mu s$ (Tab.1); in particular, in Fig.5.4, the whole transition is shown for both input and output

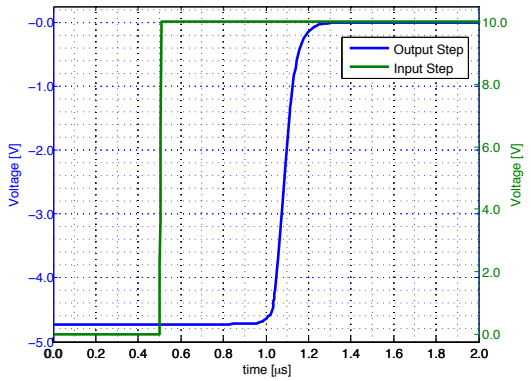

Figure 5.4 – Response to 10 V – 10 ns step (Input Step in Green, Output Step in Blue)

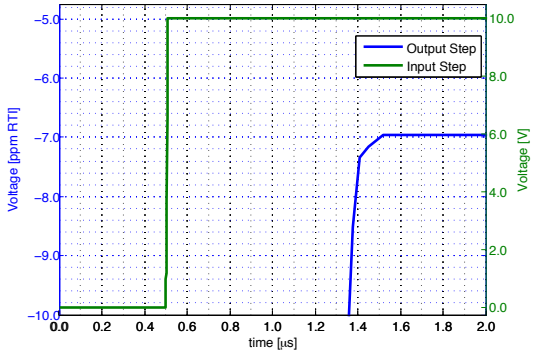

Figure 5.5 – Response to 10 V – 10 ns step (Input Step in Green, Output Step in Blue) - Zoom

signals, while in Fig.5.5, a zoom on the settling point is depicted (in this case the output signal is Referred To Input, RTI, and translated in ppm of Full Scale.) However, in nominal working conditions, a step signal with a rise time shorter than 3 μs is not expected, thus the settling time is expected not to be a critical issue for this application.

6 The On-line Acquisition System

In this section, the performance of the proposed instrument are simulated in Pspice and compared with the requirements stated in section 2.2.

6.1 Noise and Bandwidth

Two Pspice simulations have been performed to verify bandwidth and noise performance.

In the first simulation, the noise introduced by the analogue front-end was assessed. The contributions of all the components sketched in Fig.2.5 are taken into account. The results, depicted in Fig.6.1 (green curve), show an RMS noise value of about 3.2 ppm referred to input (RTI).

In the second Pspice simulation, the $-3\ dB$ bandwidth of the proposed real-time digitizer was verified. In Fig.6.1, the simulation result is depicted showing that the $-3\ dB$ bandwidth is higher than 1 MHz, while an attenuation of more than 10 dB is obtained at $B_{AF} = 2.7\ MHz$ as stated in section 3.4.

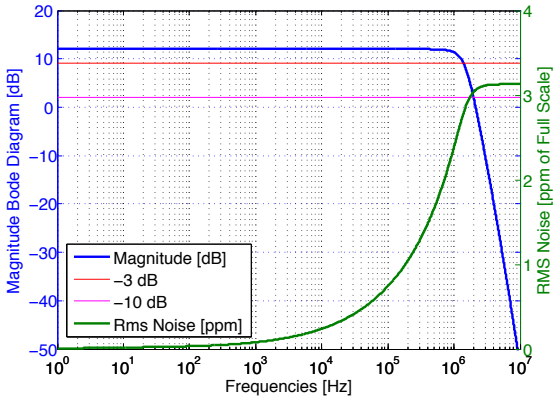

Figure 6.1 – Magnitude Bode Diagram and RMS Noise

Table 6.1 – Expected Delay

Source	Value [ns]
High-voltage divider	160
Analogue front-end	340
ADC	40
Digital filtering	670
Total	**1210**

6.2 Delay

The group delay of the analogue front-end was also assessed in simulation. A delay of about 340 ns was observed from low frequency up to about 300 kHz. However, also the contributions of (i) the upstream high-voltage divider, (ii) the ADC, and (iii) digital filtering should be taken into account. In Tab.6.1, all these contributions are summarized.

If the bandwidth of the high-voltage divider is less than 1 MHz, the analogue anti-aliasing filter will be re-tuned to increase the bandwidth of the analogue front-end. In fact, as mentioned in section 3.3.3, a high-voltage divider is typically the first stage of the considered anti-aliasing filter, thus its trade-off delay/attenuation has to be included into the design. In this case, the RMS noise of the analogue front-end is not expected to increase drastically, owing to the very low-noise design.

6.3 Worst-Case Repeatability

In the last simulation trials, the expected *WCR* was assessed. The quantization noise of both ADC_1 and ADC_2 was simulated according to their *SINAD* specification (section 2.2) by means of the Pspice function *RND*, which generates random numbers with uniform distribution. A 10 V_{DC} stimulus is given as input to the analogue front-end and the output is measured $N = 30$ times. Each pair of consecutive acquisitions is then used to calculate the *WCR* as the maximum observed value of PPR. In Fig.6.2, a statistical sample of WCR ($N-1 = 29$ observations) is depicted and visually compared with the superior bound discussed in section 3.3.4. In conclusion, the *WCR* assessed in simulation is comfortably lower than the required 50 ppm.

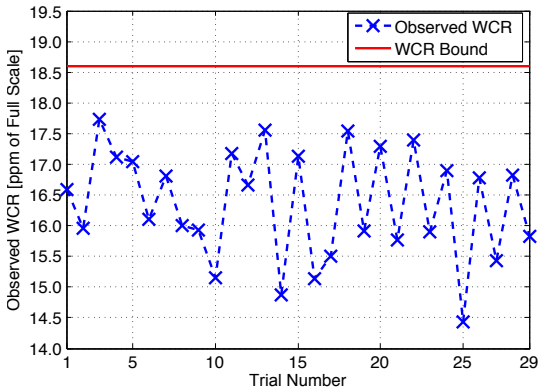

Figure 6.2 – Observed Worst-Case Repeatability

PART 4 - EXPERIMENTAL RESULTS

7 The Worst-Case Uncertainty Analytical Model

An experimental proof demonstration was carried out for the above mentioned case study at CERN. The reference acquisition system for the $CLIC$ klystron modulators is composed by a custom ultra low-noise analogue front-end [5], and a high-speed high-resolution acquisition board, the $NI-PXI$ 5922. The acquisition system has suitable stability within the period of the pulse's train (20 ms), thus all the *long-terms* effects (e.g. temperature drift) can be neglected and the only factor affecting WCR is the instrumental noise.

In the following, the model is characterized by verifying (i) the assumption of additive white Gaussian noise, and (ii) the behaviour for the required sample size (short-term prediction) and an 1-year long time window (long-term).

7.0.1 Additive White Gaussian Noise

The reference acquisition system was carefully characterized in terms of its internal noise by means of the test set-up sketched in Fig.7.1 with shorted and grounded inputs. In this section, the hypotheses of additive Gaussian and white noise are verified by means of a χ^2 test (Gaussianity), and an auto-correlation test (whiteness).

Gaussian Noise Model

Under the hypotheses that (i) the acquisition board $NI-PXI$ 5922 does not saturate during the sampling, and (ii) the internal noise of the analogue front-end (Fig.7.1) has a standard

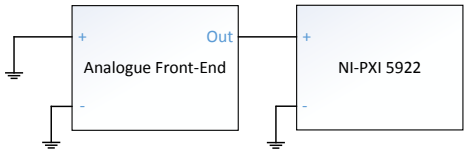

Figure 7.1 – Worst-Case Repeatability Measurement Setup.

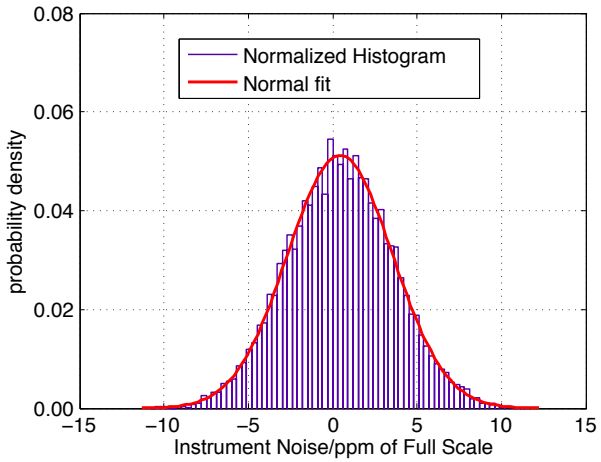

Figure 7.2 – Noise of the *CLIC* Reference Acquisition System with Normal Fit (10,000 samples).

deviation greater than 0.4Δ, with Δ the quantization step, it has been reported in [44] and demonstrated in [45] that its internal noise can be accurately modeled as Gaussian noise. In [5], the noise standard deviation was assessed to be $3.12\,ppm$ of Full Scale, much greater than $0.4\Delta_{5922} \approx 0.4\,ppm$ of Full Scale (all values reported are Referred To Input, RTI), according to the specification of effective number of bits in the data-sheet. The goodness of the Gaussian model with $\sigma = 3.12\ ppm$ of Full Scale for the system's noise was also verified by means of a χ^2 test ($\alpha = 0.1\%$). The test results are depicted in Fig.7.2, where the normalized noise histogram built by a 10,000 sample size is compared with the Normal fitting.

White Noise Model

The other assumption to be verified is the whiteness of the instrumental noise. By definition, a white noise has a normalized impulsive auto-correlation ideally equal to 1 at zero-lags and 0 elsewhere. In the practice, noise whiteness is tested by verifying that, for every $lag \neq 0$, the absolute value of its auto-correlation function is below a given threshold corresponding to the confidence interval.
Thus, the noise was acquired within the flat-band of the instrument, namely $5\,MHz$ [5]. The results of Fig.7.3 highlight clearly the impulsive shape of the auto-correlation function, confirming the initial assumption of white instrument noise.

7.0.2 WCR Prediction

In the following, the model is verified for the required sample size (short-term prediction) and an 1-year long time window (long-term).

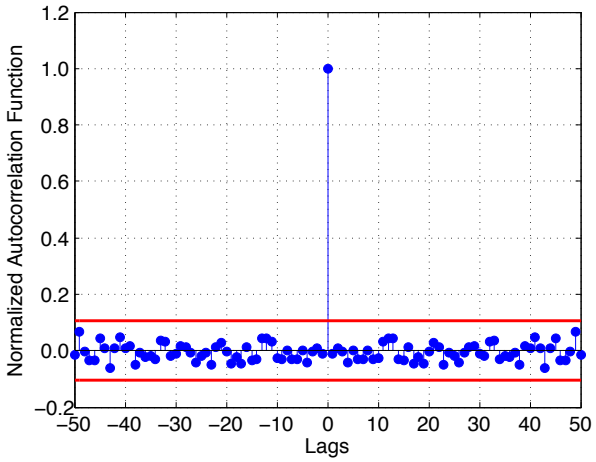

Figure 7.3 – Normalized Auto-Correlation Function with 99.9 % of Confidence Interval.

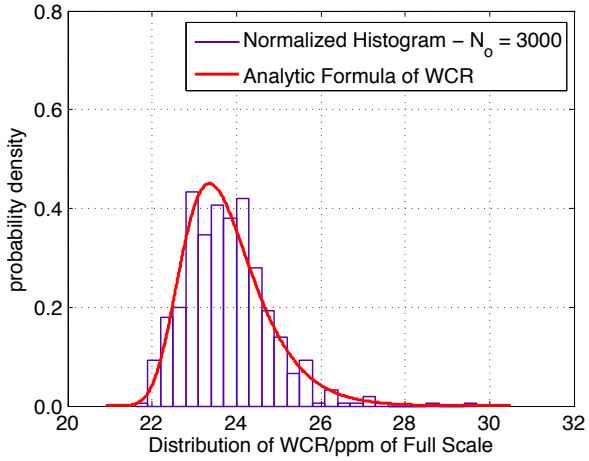

Figure 7.4 – WCR of the CLIC Reference Acquisition System for $N_o = 3{,}000$ and $N_{test} = 500$.

Short Term

By means of the same test set-up of Fig.7.1, the intrinsic WCR of the system was characterized according to equation (1.11) over the desired sample size $N_o = 3000 - 1$ (1 minute of acquisition). The statistical sample is generated by reiterating the whole measurement $N_{test} = 500$ times (note that such a measurement has a duration of about 500 minutes).
In Fig.7.4, the measured WCR is compared with the proposed model. Also in this case, the χ^2 test did not reject the hypothesis that the acquisition system's WCR is actually distributed according to the proposed distribution at a significance level $\alpha = 0.1\%$.

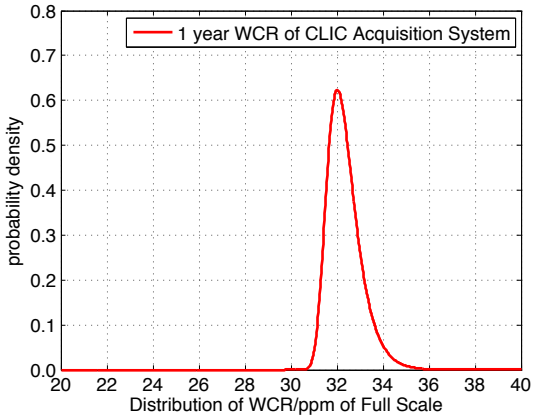

Figure 7.5 – Estimated WCR of the CLIC Reference Acquisition System for $N_o = 1.5768 \times 10^9$.

Long Term

The agreement shown during these tests allows the WCR of the system to be predicted for larger N_o, when the actual measurement would be infeasible due to the extremely long test duration. Assuming the total RMS noise of the reference acquisition system to be not greater than $3.12\,ppm$ of Full Scale, the estimated WCR distribution is depicted in Fig.7.5 for $N_o = 1.5768 \times 10^9$, corresponding to 1 year of acquisition considering the $CLIC$ case study ($1.5768 \times 10^9 \cdot RP = 365\,days$).

8 The Reference Acquisition System: Proof of Principle

The design of the proposed circuit was validated experimentally within a case study for the CLIC project at CERN, summarized in Tab.1.

8.0.1 Amplitude Frequency Response

The measurement setup, shown in Fig.8.1, consists of an arbitrary waveform generator (Agilent 33220A) and two digital multimeters (HP 3458A). The two multimeters were firstly characterized up to 10 MHz and, in the worst case, their difference was smaller than 0.6 dB. A set of sine vaves of small amplitude (20 mV_{pp}) was generated by the arbitrary waveform generator with frequency ranging from 10 kHz to 100 MHz and sent both to a multimeter and the analogue front-end. At each step, the rms values of the two signals (input and output of the analogue front-end) were measured by the two multimeters in AC voltage mode in order to obtain the corresponding point on the Bode diagram. The experimental results, shown in Fig.8.2, are compatible with the simulation ones. Moreover, a good flatness is observed up to 5 MHz, where the $-3\,dB$ point is located.

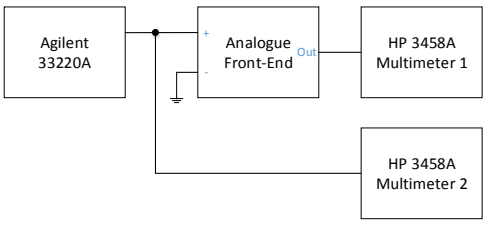

Figure 8.1 – System Frequency Response Setup

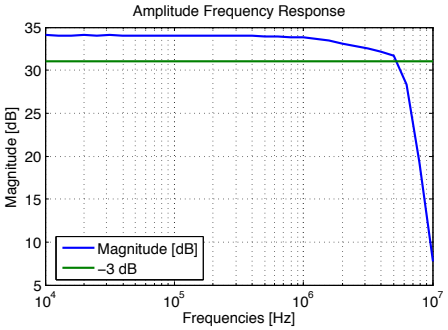

Figure 8.2 – Amplitude Bode Diagram

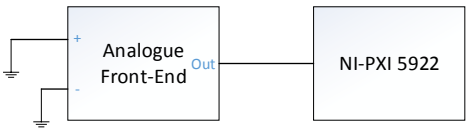

Figure 8.3 – Noise Evaluation Setup Block Diagram

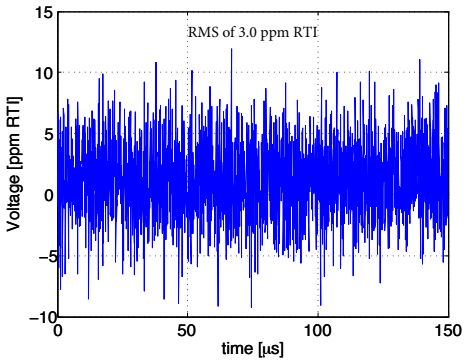

Figure 8.4 – Typical Acquired Noise Sample

8.0.2 Noise Analysis

The measurement setup shown in Fig.8.3) allows the noise affecting the system composed by the analogue front-end and the acquisition board NI PXI 5922 to be assessed. Preliminarily, the NI PXI 5922 internal noise with its inputs shorted to ground was proved to be negligible with respect to the analogue front-end's one. The noise of the analog front-end was tested with the measuring channel in unbalanced differential configuration measuring a RMS noise of about 3.0 $ppm\ RTI$ as depicted in Fig.8.4. The results proved that the experimental and simulated noise levels of the circuit, respectively 3.0 ppm and 3.1 ppm at 6 MHz, are compatible. However, this proof demonstrator is not optimized in terms of noise immunity (e.g. it is not shielded), therefore, a lower noise can be achieved in an engineered version of the circuit.

8.0.3 Linearity

This test allows the linearity error to be assessed in the same conditions as the analogous simulation analysis. The measurement setup of Fig.8.5 consists of a 10 V_{DC} reference named PBC [46] and a DAC (AN 3200) with a resolution of 10 μV. At each step, the DAC generates a DC voltage ranging from $(10\,V - 60\,mV)$ to $(10\,V + 60\,mV)$ in order to obtain the same differential input sweep used in simulations. Both multimeters are set for DC voltage measurements with an aperture of 50 power line cycles. For each input value, $N = 5$ samples are acquired in order to evaluate the measurement repeatability ($\sigma/\sqrt{N}$). The test results, calculated according to equation (5.2) and depicted in Fig.8.6, match the simulation ones, with a non-linearity error of less than 2 ppm of 10 V at a temperature of 21 °C.

8.0.4 Repeatability Results

Once the main performance forecast by simulation has been experimentally confirmed on the prototype, two fold tests of repeatability aimed at validating the design as a whole were carried out: (i) in $short\ circuit$, for assessing the intrinsic repeatability of the circuit without any input signal, and (ii) in operation, for assessing the $Common\ Mode\ Rejection$, because,

during the pulse flat-top, both input voltages are around 10 V.

Short-circuit Test

For this test, a laboratory setup analogous as for noise characterization with both the inputs at ground (Fig.8.3) was used. The Pulse-to-Pulse Repeatability was computed according to eq. 2.1 by means of two noise acquisitions lasting 150 μs each (2250 samples at 15 MS/s) and spaced by an idle time of 20 ms in order to emulate the acquisition of two consecutive pulses. The procedure was repeated 300 times (emulating 300 pulses) to obtain the histogram of PPR in Fig.8.7. The mode of the distribution is about 15 ppm while the maximum, obtained as the maximum amongst 675000 samples (2250·300), is below 25 ppm. This confirms the suitability of the design for the reference acquisition system.

Common Mode Rejection Test

The test setup depicted in Fig.8.8 allows the $CMRR$ of the system to be tested when a DC common voltage of 10 V is connected to both the analogue front-end inputs. Two different reference DC generators were used, the PBC [46] and the Fluke 732A, in order to evluate the generator contribution. The results, of Figs.8.9,8.10 show that the repeatability as assessed by the generator Fluke732A (Fig.8.10) is significantly worse than by the PBC (Fig.8.9), by considering both the mode and the tails of the distribution. This difference is caused both by a higher instrumental noise of the 732A (producing a higher common mode noise because the 732A is applied to both the inputs) and by the Common Mode Rejection Ratio (CMRR) of the circuit. As stated in 2.3.3, $CMRR$ is heavily affected by the quality of the resistors used in the prototype [36]. In fact, the $CMRR$ of a difference amplifier is given by:

$$CMRR \approx \frac{\frac{1}{2}(G_{DIFF}+1)}{\left[\frac{1}{2}(G_{DIFF}+1)\left(\frac{1}{CMRR_{AMP}}\right)\right]+\frac{\Delta R}{R}} \tag{8.1}$$

where:

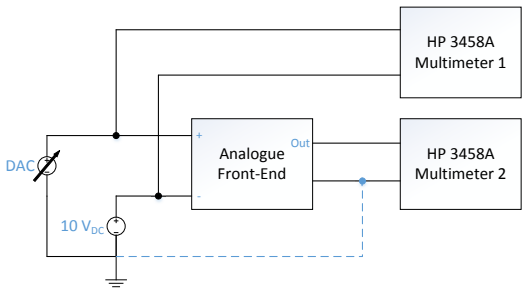

Figure 8.5 – Linearity Setup

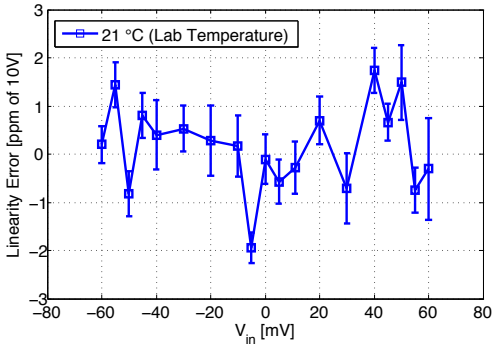

Figure 8.6 – Measured Linearity

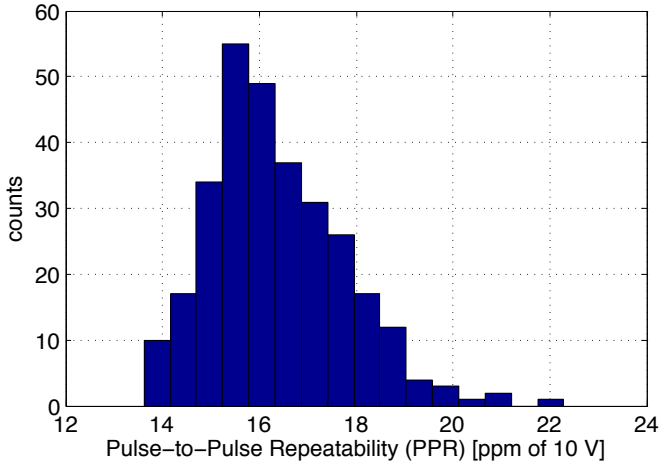

Figure 8.7 – Repeatability Measured in Short Circuits.

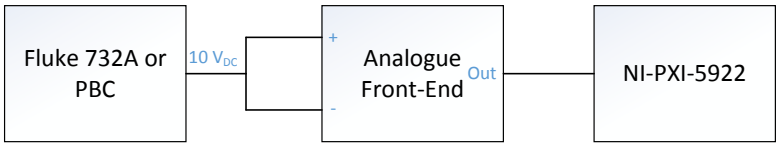

Figure 8.8 – Setup For Repeatability Measurement With 10 V_{DC} At Both Inputs.

- G_{DIFF} is the differential gain of the amplifier (≈ 7.5);
- $CMRR_{AMP}$ is the $CMRR$ declared on the datasheet of the amplifier ($\approx 120\,dB$);
- and $\frac{\Delta R}{R}$ is the tolerance of the resistors involved in differential gain setting (0.1 % are used in the prototype).

This highlights a $CMRR$ of about 66 dB by considering the worst case of resistors with combined maximum relative uncertainty of 0.2 %. $CMRR$ can be improved by replacing the

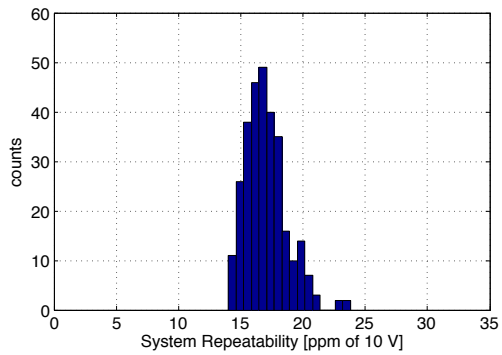

Figure 8.9 – PBC

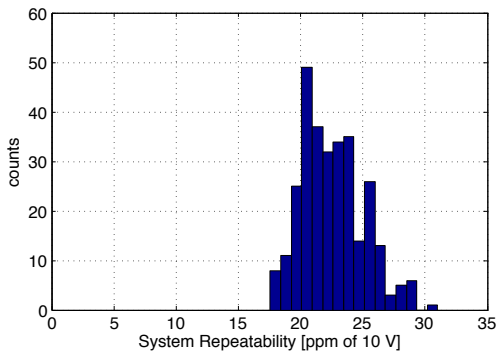

Figure 8.10 – Fluke 732A

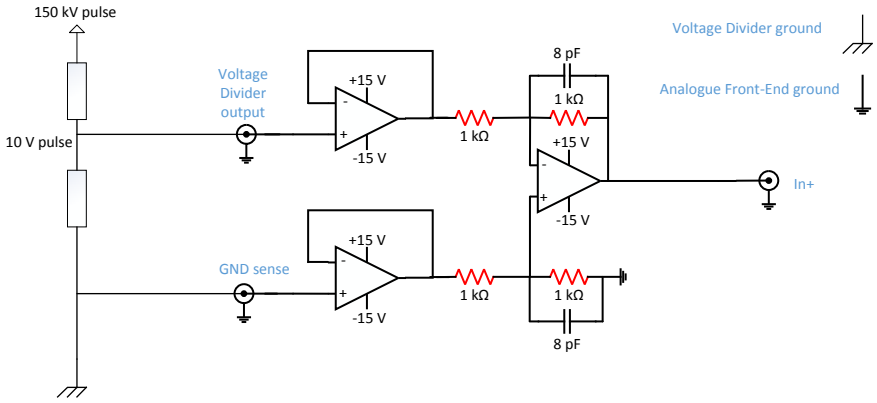

Figure 8.11 – Differential Sensing Circuit.

presently used 0.1 % resistors by a set of matched 0.01 % resistors. In this circumstance, a worst-case $CMRR$ of about 86 dB is estimated. The higher common mode noise of the generator Fluke732A is expected to be rejected by the circuit, and the PPR improved accordingly. However, this test allows measuring the repeatability performance of a generator plus the acquisition system; since the real interest of this work is limited to the characterization of the acquisition system repeatability, the short circuit test should be considered as the reference.

8.0.5 Differential Sensing Circuit

In the final version of the analogue front-end, a Differential Sensing Circuit (DSC) is needed for the positive input (replacing the R_2/C_2 filter and the buffer in Fig.2.5). The circuit aims at solving twofold issues (Fig.8.11):

- Reject the Common Mode Voltage between acquisition system and voltage divider arising from the ground loop related to separated and far grounds, by means of a suitable difference amplifier (again based on the ADA4898);
- Decouple the voltage divider from the analogue front-end by means of two input buffers (model OPA627).

In Fig.8.12, the amplitude frequency response of the analogue front-end with the DSC assessed in simulation is shown. The cut-off bandwidth is still localized around 5 MHz demonstrating that the DSC does not affect the amplitude frequency response of the analogue front-end. Furthermore, Fig.8.13 shows that the new RMS noise of the front-end is approximately 3.4 ppm RTI.

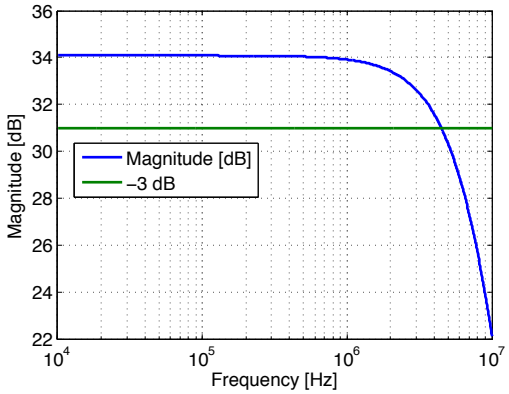

Figure 8.12 – Simulated Amplitude Frequency Response with Differential Sensing on Positive Input.

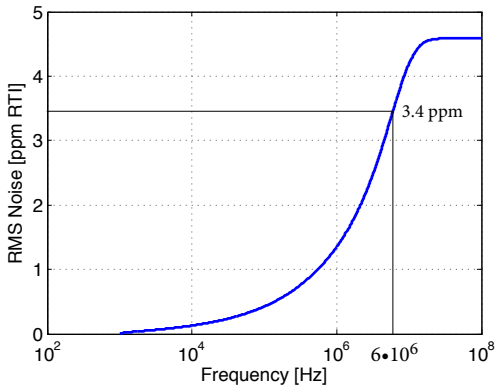

Figure 8.13 – Simulated *RMS* Noise with Differential Sensing on Positive Input.

9 The Reference Acquisition System: Metrological Characterization

9.1 CMRR Measurement

During the design of the front-end, particular attention was paid to the design of a high-CMRR differential stage. [5] In particular, the *DC CMRR* turned out to be an important feature to properly shift the high state of the pulse to around zero. In the following, the *CMRR* measurements aimed at experimentally proving the achievement of the above-mentioned design goal are reported.

9.1.1 Common-Mode Input Voltage Rejection

A *CMRR* higher than 86 *dB* was expected in [5] because of the 0.01% tolerance resistors. Such a design expectation was proven by means of the setups in Fig.9.1. The test was carried out in two phases:

- The first phase (Fig.9.1a), consisted of measuring the output offset of the front-end when both inputs are shorted to ground with the high-resolution (up to 24 bits) high-speed (up to 15 MS/s) acquisition board NI-PXI 5922. In Fig.9.2, the results of repeated

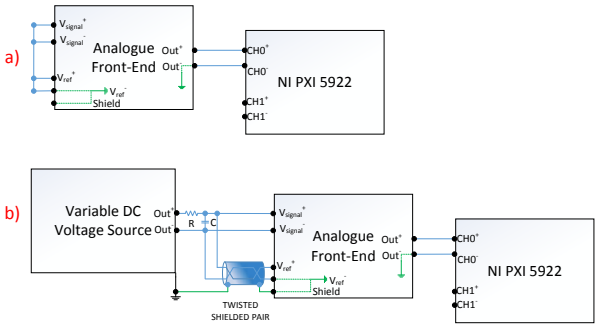

Figure 9.1 – Setup for measuring $CMRR_{diff}$, with inputs: a) Shorted to Ground, and b) Supplied by *DC* Voltage

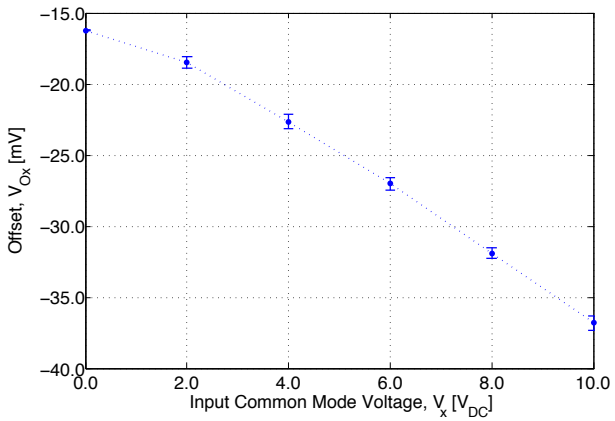

Figure 9.2 – Measured Output Offset (V_{Ox}) vs Common-Mode Input Voltage (V_x). Error bars show the standard deviation for the 68 % confidence interval (1-σ)

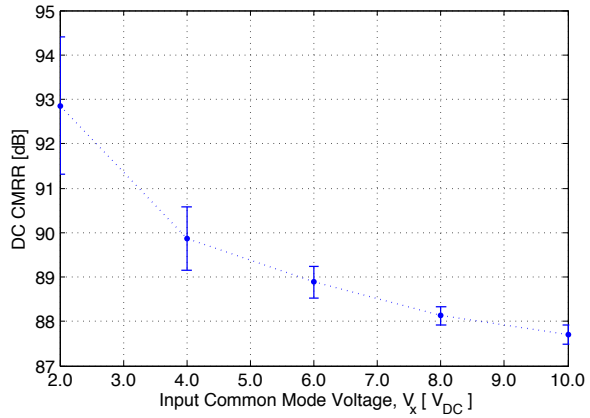

Figure 9.3 – $CMRR$ vs Common-Mode Input Voltage (1-σ Uncertainty Band)

measurements are depicted where the errors bars represent the standard deviation (30 measurements for each point). An offset of about $V_{Osc} \approx -16\,mV$ is shown for an input common mode voltage of $V_0 = 0\,V$ (shorted and grounded inputs).

- The second phase (setup in Fig.9.1b) consisted of measuring the output offset ($V_{Ox} = V_{O2}...V_{O10}$) corresponding to a particular input common mode voltage. A variable DC voltage source was used to generate a DC voltage $V_x = 2.0 \cdots 10.0$V (2.0V steps) that was simultaneously applied to both inputs of the analogue front-end. At this stage of the measurement, the focus of interest was on the $DC\ CMRR$ of the differential stage (red dotted circle in Fig.2.6), namely $CMRR_{diff}$. Therefore, an RC low-pass filter ($R = 820\,k\Omega$, $C = 10\,nF$) was used to remove disturbances with frequency content above $20\,Hz$. At each step, a common-mode voltage equal to the voltage generated by the calibrator was applied to the circuit. In Fig.9.2, the results are illustrated.

The acquisition board NI PXI 5922 acquires 30 records of the front-end's offset with a trigger at 50 Hz (20 ms period). Each record is composed by 2250 samples (150 μs at 15 MS/s, namely the nominal working conditions). The Common-Mode Input Voltage Rejection $CMRR_{diff}$ can be computed using:

$$CMRR_{diff} = 20Log_{10}\left(\frac{G \cdot V_x}{|V_{Ox} - V_{Osc}|}\right) \tag{9.1}$$

where G is the gain of the front-end ($G = 50\,V/V$), V_x the corresponding common-mode input, V_{Ox} and V_{Osc} the offset measured when $x\,V$ are applied to the inputs, and when both the inputs are shorted to ground (first phase), respectively.
In Fig.9.3, the $CMRR$ is reported by highlighting the 1-σ dispersion over 30 samples. The worst case was observed with a common mode input of 10V, which is the nominal working condition of the measurement system. As explained in,[47] the offset voltage of an operational amplifier is affected by the bias point of its input differential pair, which in turn is affected by the imposed common-mode input voltage. This results in a *CMRR* variation with respect to the particular working point. At 10 V, a $DC\ CMRR_{diff}$ of about 87.7 dB was measured, confirming the theoretical prediction in. [5] Nevertheless, the test setup measured the $CMRR_{diff}$ of the circuit as a whole (not only the difference amplifier as in [5]); thus, if the worst-case condition is met by the whole $CMRR$, $a\,fortiori$ it will be met by the difference amplifier.

9.1.2 Common Mode Ground Voltage Rejection

In metrological applications, all the measurements have to be referred to the same reference voltage (e.g. GND voltage) otherwise ground loops could affect the measurement quality (Fig.9.4).

The input stage of the analogue front-end is composed of a differential sensing circuit (in blue in Fig.2.6),[5] which rejects the common-mode voltage between the two grounds. This common mode voltage is $CMRR_{ref}$. The test setup of Fig.9.5 allows $CMRR_{ref}$ to be assessed

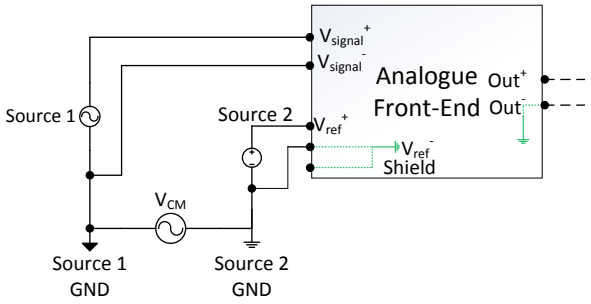

Figure 9.4 – Ground Loop Between Two Far Grounds

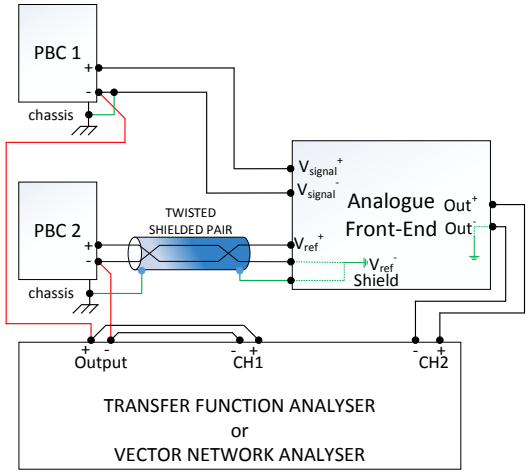

Figure 9.5 – Test Setup for Measuring $CMRR_{ref}$ Between the Two Voltage Reference

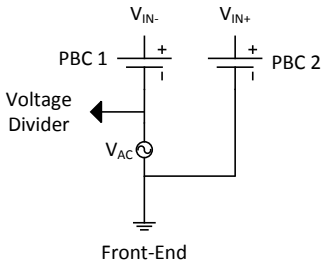

Figure 9.6 – CM_{ref} definition

Figure 9.7 – $CMRR_{ref}$ Measurement Setup and CM_{ref} Definition

over a frequency range of 1 MHz. Case in comparison with the previous measurement, where $CMRR_{diff}$ was evaluated by imposing a common-mode voltage between each input and GND, in this test the common mode voltage was imposed between the references of the two DC generators. A Transfer Function Analyzer, TFA (also known as Frequency Response Analyzer or Gain Phase Analyzer), Powertek GP 102 was used to generate a set of sine waves ranging in frequency from 10 mHz to 1 MHz. The sine waves were applied between the chassis references of two fully floating DC 10 V portable generators ($PBCs$).[46] The two PBCs, in turn, fed the two inputs of the front-end fixing the static working point at 10 V. Amplitude and phase (difference) of the input sine waves (connected to CH1 by means of a tee connection) and the output of the front-end were then measured by the TFA in order to determine the Bode diagram.

In this test, PBC 1 was used to emulate the signal coming from the Voltage Divider and PBC 2 the local 10 V reference voltage. In the test setup of Fig.9.5, it is shown that the chassis of PBC 1 is connected to the terminal minus of V_{signal} on the front-end, which is a differential

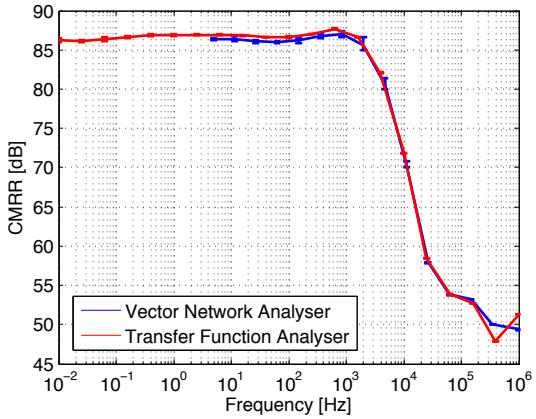

Figure 9.8 – $CMRR$ of the Circuit for Rejecting Common Mode Voltage Between the Voltage Divider and the Local Ground

input. On the contrary, the chassis of PBC 2 is connected to the front-end's ground through the shield of the twisted shielded pair. Fig.9.6, shows how V_{AC} was combined at the input stage and highlights the common mode voltage (V_{CM}) which was actually experienced by the front-end:

$$V_{CM} = \frac{V_{IN+}+V_{IN-}}{2} = \frac{(V_{PBC1}+V_{AC})+V_{PBC2}}{2} = 10\,V + \frac{V_{AC}}{2} \tag{9.2}$$

The DC part of equation (9.2) (10 V) was rejected according to section 9.1.1 while the rejection of $V_{AC}/2$ was the actual purpose of this test. In a way similar to the $CMRR_{diff}$ in 9.1, $CMRR_{ref}$ can be defined as:

$$CMRR_{ref} = 20 \cdot Log_{10}\left(\frac{G_D}{G_{CM}}\right) = 20 \cdot Log_{10}\left(\frac{G_D V_{CM}}{V_{out}}\right) = = 20 \cdot Log_{10}\left(\frac{G_D V_{AC}}{2 \cdot V_{out}}\right) = 20 \cdot Log_{10}\left(\frac{G_D V_{AC}}{V_{out}}\right) - 20 \cdot Log_{10}(2) \tag{9.3}$$

where G_D and G_{CM} are the differential and common-mode gains respectively. This shows that a correction factor of $-20 \cdot Log_{10}(2)$ should be applied to the instrument reading.

Given the importance of $CMRR$ for this particular work, the measurement reproducibility was tested using different test instruments and test conditions:

- two different input sine waves amplitude were applied (1 V_p and 100 mV_p);
- two *TFAs* were used (same model, different serial numbers);

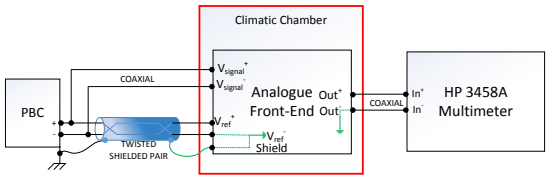

Figure 9.9 – Test Setup for Offset Drift Measurement

- a Vector Network Analyser (*VNA*), was used thanks to its gain-phase features (model Keysight E5061B).

The results obtained were always within ±0.4 % of each other's nominal values. In the last case, due to the *VNA* frequency limitation, the lowest analyzed frequency was 5 Hz.

The results obtained over 10 repetitions with both the TFA and VNA are depicted in Fig.9.8, where the average value together with the minimum and maximum bars are shown. They show a $CMRR_{ref}$ of about 87 dB up to 1 kHz, decreasing at higher frequencies down to 48 dB at 1 MHz, which is still a considerable result.

9.2 Offset Drift

The output drift of the analogue front-end, with an applied common mode voltage of 10 V, was characterized by means of the test setup in Fig.9.9. The analogue front-end was placed inside a climate-controlled chamber, and the output voltage, corresponding to a 10 V_{DC} common mode input (PBC), was measured by a digital multimeter HP 3458A thanks to its DC accuracy of 0.6 ppm. The multimeter was set with a measurement time of 1 s, corresponding to a Number of Power-Line-Cycles (*NPLC*) of 50. In this way, the effect of both the normal-mode and the high-frequency noise is mitigated by averaging the measurand over 1 s, and only the slow-trend stability is assessed. In this section, the output voltage when both analogue front-end inputs are set to 10 V is referred to as offset. The following test results for (i) *offset in nominal conditions*, (ii) *temperature slow variation*, (iii) *temperature fast variation*, and (iv) *humidity response* are illustrated.

9.2.1 Offset in Nominal Conditions

The first test aimed at assessing the offset of the instrument during its nominal working conditions when normal operations (as power-up) or unwanted power-supply drops occur at a fixed and controlled temperature of 23 °C and relative humidity of 30 %. The test was carried out in four phases, corresponding to four different sources of offset variations: (1) not powered, (2) *powered*, (3) *constant power supply*, and (4) *power supply drop*. In Fig.9.10, the result of the test as a whole is reported by highlighting the four steps.

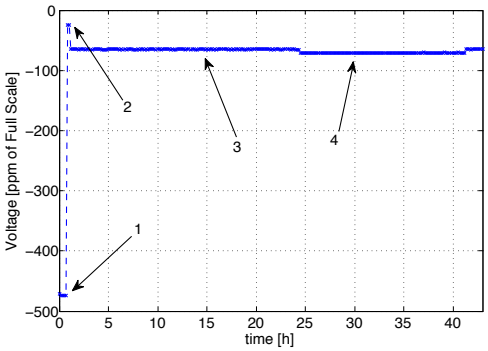

Figure 9.10 – Overall Measurement

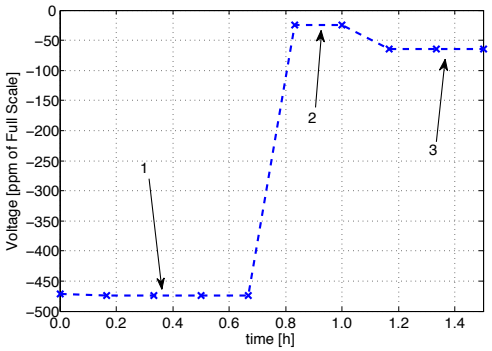

Figure 9.11 – Power-up

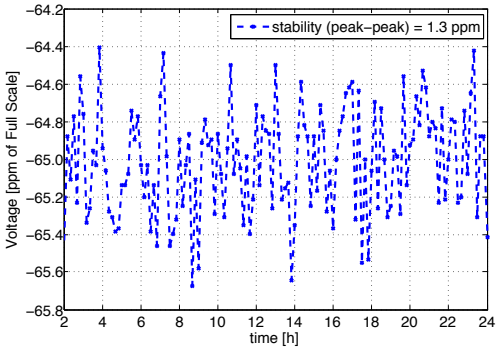

Figure 9.12 – Stability

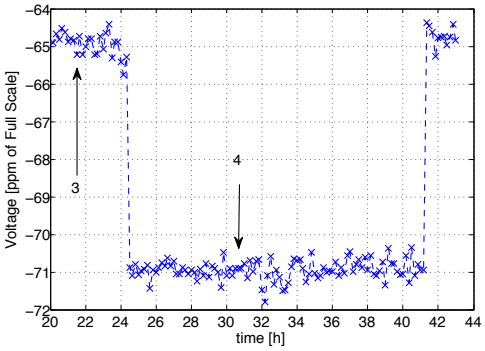

Figure 9.13 – Power Supply Drop

- *Step 1* The test started with the analogue front-end not powered which is resulted in an offset voltage of about −470 ppm of the full-scale (all the reported values are referred to the input). See Fig.9.11.

- *Step 2* When the power supply was turned on, the offset rapidly increased from the initial value up to about −24 ppm with floating inputs. See Fig.9.11.

- *Step 3* When the *PBC* was connected to both the inputs the offset moved to its nominal value of about −65 ppm (see Fig.9.12) showing a very good peak-to-peak stability of about 1.3 ppm for more than 20 hours.

- *Step 4* A voltage drop was emulated in the power supply; in particular, the nominal $\pm 15\,V$ were symmetrically decreased to $\pm 14\,V$. In this case, the offset level suffered a drop of about 6 ppm for a supply variation of $1\,V$ highlighting a good Power Supply Rejection Ratio (*PSRR*) of about 84 dB. Finally, the supply voltage was increased again to $\pm 15\,V$ and the offset returned to its nominal value of about −65 ppm. See Fig.9.13.

9.2.2 Slow Temperature Variation

The slow temperature variation test consisted in imposing a temperature profile with slow variations (30 °C in 6 hours), at a constant relative humidity of 30 %, while measuring the offset

by a digital multimeter *HP 3458A* (Fig.9.9). In this case, an output variation of about 1.5 ppm was measured over the total temperature variation of 32 °C (Fig.9.14). Correspondingly, even if there was not an instantaneous correlation between temperature and offset voltage (e.g. there is a delay), a temperature coefficient better than about 0.05 ppm/°C with a temperature variation rate of 5°C/h could be derived.

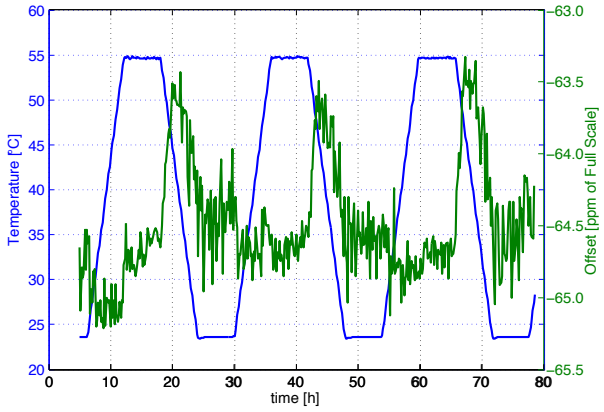

Figure 9.14 – Offset Variations (right-hand scale in green) Due to a 5 °C/h Temperature Profile (left-hand scale in blue)

9.2.3 Fast Temperature Variation

The dependence of the offset on the temperature rate is demonstrated by the fast temperature variation test. Starting from 23 °C, the temperature was increased at a rate of 10 °C/h (double the rate of the previous test) up to about 43 °C at a constant relative humidity of 30 %. In this case, an offset variation of about 2.0 ppm was measured (see Fig.9.15), higher than 1.5 ppm obtained in the previous test over 30°C of variation. In conclusion, a temperature coefficient better than 0.1 ppm/°C was derived from the measurement with a temperature variation rate of 10°C/h.

9.2.4 Humidity Response

The analysis of the offset dependence on the environmental conditions was completed by assessing the relative humidity response (*RH*) of the instrument. In particular, the test consisted of producing a humidity step from 30 % to 70 % while keeping temperature stable at 23 °C . A maximum drift of only 0.4 ppm was observed (Fig.9.16), even over such an important humidity change. The acquired offset values shown in Fig.9.16 were digitally filtered highlight the low-frequency trend due to humidity variations. In conclusion, the sensitivity of the analog front-end to humidity is less than 0.4 ppm/% RH, which is considered negligible for the CERN application.

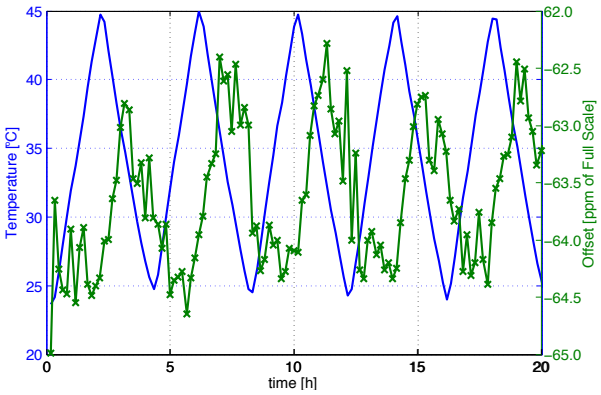

Figure 9.15 – Offset Variations (right-hand scale in green) Due to a 10 °C/h Temperature Profile (left-hand scale in blue)

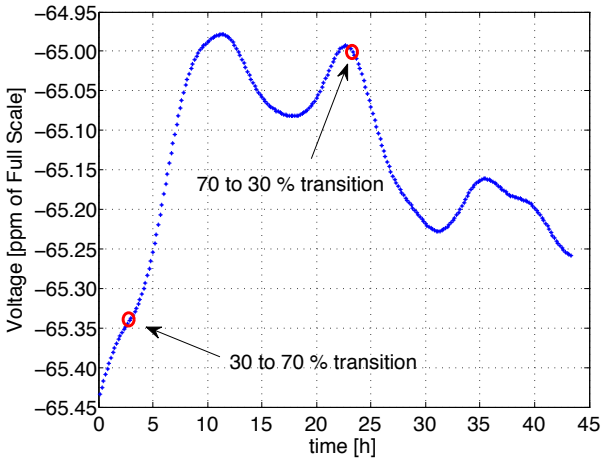

Figure 9.16 – Offset Variations Due to a Humidity Change from 30% to 70%

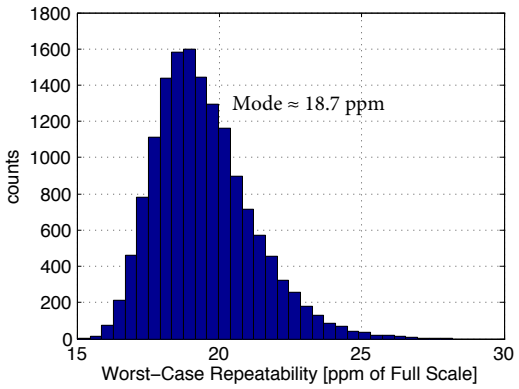

Figure 9.17 – Worst-Case Repeatability histogram with both input shorted to GND

9.3 Worst-Case Repeatability

The test setup of Fig.9.1, already used for $CMRR_{diff}$ measurement in 9.1, was used for assessing the Worst-Case Repeatability (WCR) defined as:

$$WCR(j) = max_i \left| V_{i,j} - V_{i,j+1} \right| \tag{9.4}$$

where $V_{i,j}$ is the i^{th} sample of the j^{th} pulse whereas $V_{i,j+1}$ is the homologous sample belonging to the following pulse.[8] The measurement was carried out by acquiring 15,000 records of the analogue front-end output, each of them composed by 2,250 samples. For each of the 15000 acquisitions, the maximum observed value was recorded. All these values were used to build a histogram of the WCR in order to highlight its sample mode.
In the following, the test results for: (i) *short circuit*, (ii) 10 V_{DC} *common mode*, and (iii) *distribution mode vs common-mode input* are illustrated.

9.3.1 Short Circuit

The test setup of Fig.9.1(a) was used for this first test. The two inputs were shorted together to ground in order to measure only the contribution of the analogue front-end and the acquisition board to the WCR figure. Fig.9.17 shows the histogram of the worst-case values of 15000 acquisitions, which has a mode of about 18.7 ppm of full-scale and a highest value worst-case value well below 30 ppm.

9.3.2 10 V_{DC} Common Mode

This test, whose setup is depicted in Fig.9.1(b), allowed the WCR of the measurement system to be assessed in its nominal working conditions, with a common-mode voltage of 10 V imposed at the input. The input voltage was generated by the PBC and the RC filter, connected to its output, attenuated the noise frequency content greater than about 20 Hz, thus only

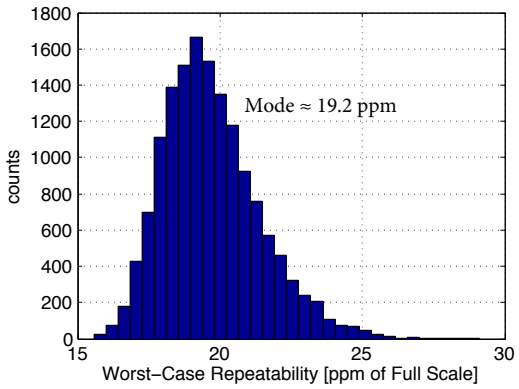

Figure 9.18 – Worst-Case Repeatability histogram with both input connected to a PBC

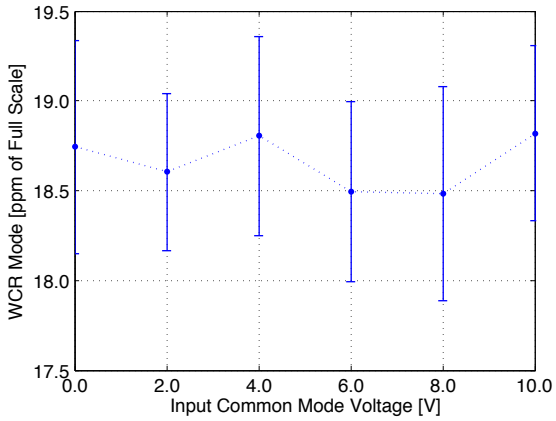

Figure 9.19 – Mode of WCR for Different Common Mode Input Voltages with 1-σ error bars

the DC was assumed as input of the front-end. The histogram for this WCR measurement is shown in Fig.9.18 and was compatible to the one obtained with shorted and grounded inputs. This was also confirmed by a χ^2 Kolmogorov-Smirnov test at the significance level $\alpha = 5\,\%$ and aimed at verifying that the two independent statistical samples have the same underlying distribution, thus confirming the expected $CMRR$ performance of the circuit.

9.3.3 Distribution Mode vs Common Mode Input Voltage

The WCR test was also carried out for inputs ranging from 0 V_{DC} to 10 V_{DC} (steps of 2 V) in order to verify the improved repeatability immunity to common mode input. A variable DC voltage source provided an input voltage, filtered to remove noise spectral content greater than 20 Hz, and connected as common-mode voltage to the front-end. For each common mode input value, 50 histograms were built and 50 values of mode were determined. In Fig.9.19, the average of 50 sample modes with the experimental standard deviations are depicted for each value of common mode input.

10 The On-line Acquisition System

In this section, several experimental tests are discussed in order to assess the performance of the first prototype of the new instrument. It is worth noting that, in this section, both the custom analogue front-end and the two ADCs are tested. In particular, in order to test the two ADCs, their commercially available evaluation boards were used. In the following, the results of the following tests carried out on the prototype are illustrated:

- *Noise test*: the analogue noise is assessed together with the quantization noise of ADC_2;
- *Bandwidth test*: the amplitude bode diagram is measured thanks to a custom test setup in order to verify that no significant resonances are present;
- *Delay test*: the group delay evaluated in simulation is compared with the experimental step response;
- *DC CMRR test*: given the working principle of the analogue front-end (zero-translation), DC CMRR is assessed by means of a custom setup;
- *AC CMRR test*: the differential sensing circuit, described in section 3.4, allows rejecting the common-mode voltage between the high-voltage divider ground and the analogue front-end ground accordingly defining an AC CMRR;
- *Full signal acquisition and Pulse-to-Pulse repeatability test*: the Pulse-to-Pulse Repeatability (PPR) of the whole measurement system is measured and compared with the design expectations.

10.1 Noise Test

This experimental test aims at assessing the *rms* noise level of the analogue front-end. In section 3.3.4, a *WCR* of 18.6 ppm was demonstrated to be achievable, if the analogue noise is lower than the quantization noise of the two *ADCs*.

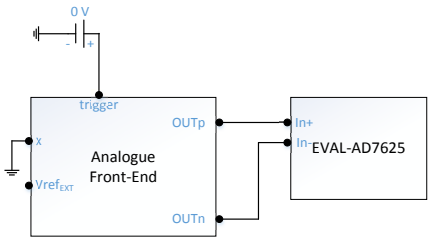

Figure 10.1 – Test Setup for Noise Measurement

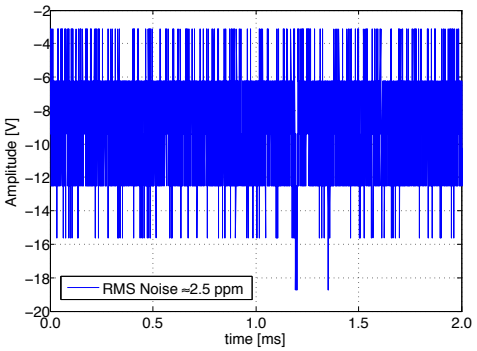

Figure 10.2 – Analogue Front-End's Noise

Figure 10.3 – Test Setup (a) and Experimental Results (b) of Analogue Front-End's Noise

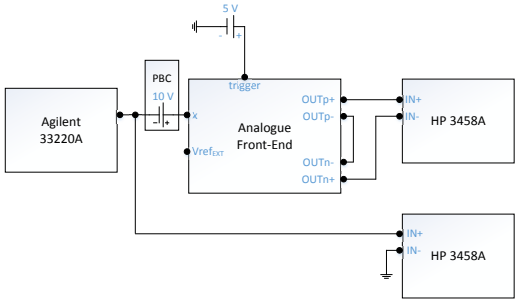

Figure 10.4 – Test Setup for Bandwidth Measurement

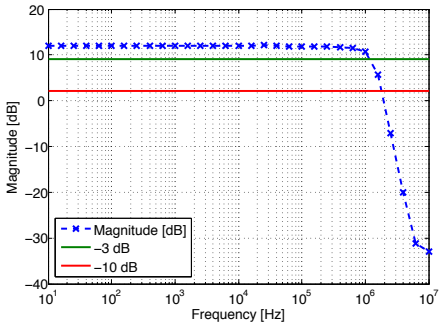

Figure 10.5 – Amplitude Frequency Response

Figure 10.6 – Test Setup (a) and Experimental Results (b) of Analogue Front-End Amplitude Bode Diagram

In Fig.10.1, the setup used for this test is depicted.

The trigger signal is set to 0 and the switch S_2 is positioned such that the difference stage (green in Fig.3.7) subtracts the signal on the terminal "x" (shorted to ground in this test) from itself in order to achieve *ideally* an output of 0. In this case, on the differential output ($OUTp - OUTn$), only the intrinsic noise of the analogue front-end is measured. The state-of the art acquisition board *NI PXI 5922* allows a differential acquisition of the two input channels. By acquiring 6.000 samples at 3 MS/s, a noise record of 2 ms is obtained. The *rms* value is about 2.5 ppm.

10.2 Bandwidth Test

In this test, the amplitude of the Bode diagram of the analogue front-end is measured in order to verify the absence of resonances and the nominal working of the analogue anti-aliasing filter as expected from design and simulation.

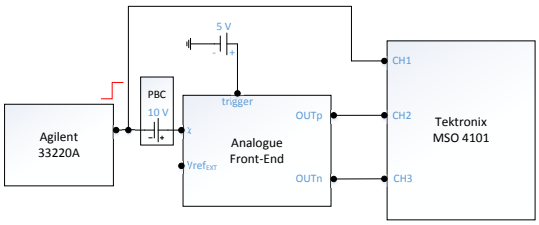

Figure 10.7 – Test Setup for Delay Measurement

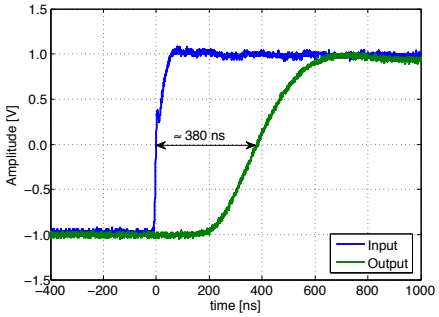

Figure 10.8 – Step Response

Figure 10.9 – Test Setup (a) and Experimental Results (b) of Step Response

The experimental test setup is sketched in Fig.10.4. An arbitrary waveform generator (Agilent/Keysight 33220A) generates a set of sine waves of $2\,V_{pp}$, with frequency ranging from $10\,Hz$ to $10\,MHz$. The sine waves are sent both to a digital multimeter (HP 3458A) and to the negative terminal of a reference *DC* voltage and current generator [46] (PBC). The positive terminal of the *PBC* sends the sine waves, shifted-up of $10\,V_{DC}$, to the signal input of the analogue front-end. The *DC* voltage shift is needed to center the $\pm 1\,V$ sine waves around $10\,V$ in order to not activate the clipping circuitry (which clips voltages below $V_{clip-} \approx 9\,V$ and above $V_{clip+} \approx 11\,V$). At this point, given the working principle of the front-end, the $Vref_{INT} = 10\,V_{DC}$ is subtracted from the input signal and the difference is amplified by a total gain of about $4\,V/V$. The sine waves out of the analogue front-end are finally measured by another digital multimeter. At each step, the *rms* values of the two signals (input and output of the analogue front-end) are measured by the two multimeters in *AC* voltage mode in order to obtain the corresponding point of the Bode diagram. The experimental results (Fig.10.6) are compatible with the simulation outcomes.

10.3 Delay Test

In this test, the step response of the analogue front-end is measured and compared with the group delay assessed in simulation.

The test setup is presented in Fig. 10.7. The arbitrary waveform generator provides a $\pm 1\,V$ step, with $5\,ns$ of rise time, to the channel 1 (*CH1*) of a digital oscilloscope. In nominal working conditions, such dynamic signals are not expected. Thus, this test evaluates a worst-case delay with respect to the simulation. Also in this case, a *PBC* shifts-up the step around $10\,V$ in order to center it in the "non-clipping" range of the analogue front-end. The Oscilloscope digitizes also the positive and negative outputs of the front-end on channels 2 and 3, respectively. In this way, by subtracting the *CH3* from *CH2*, the results in Fig.10.9 are obtained. A delay at 50 % of the transition of about $380\,ns$, compatible with the simulated group delay, is assessed.

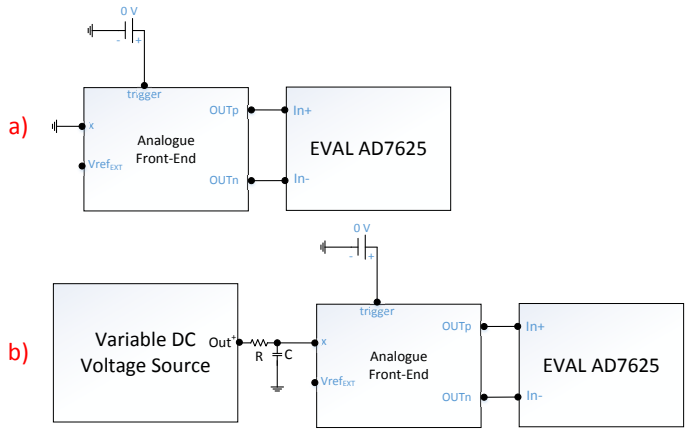

Figure 10.10 – Test Setups for DC CMRR Measurement: first (a) and second (b) test phase.

10.4 DC CMRR Test

Given the working principle of the analogue front-end (V_{ref} subtraction and amplification), the Common-Mode Rejection Ratio ($CMRR$) in DC is a critical parameter. As a matter of fact, a poor $DC\ CMRR$ would have the effect of not properly center the nominal $10\,V_{DC}$ around zero. As detailed in [36], the tolerances of the gain-setting resistors of a difference stage as in section 2.3.3 affect directly $DC\,CMRR$ performance of the stage itself. In this design, the resistor networks Vishay MPM with 0.1 % of absolute tolerance were used.

$DC\ CMRR$ was measured in two test phases by means of the corresponding twofold setups in Figs.10.10. The ADC $AD7625$, controlled by its evaluation board, acquires 50 records of the front-end's offset. Each record is composed by 450 samples acquired at $3\,MS/s$ ($150\,\mu s$), emulating the acquisition of a *pulse* phase. The test was carried out in two phases:

- The first phase (setup in Fig.10.10a), consisted of measuring the output offset of the front-end when both the nputs are shorted to ground. An offset of about $V_{Osc} \approx -380\,\mu V$ is shown for an input common mode voltage of $V_0 = 0\,V$ (shorted and grounded inputs).
- The second phase (setup in Fig.10.10b) consisted of measuring the output offset ($V_{Ox} = V_{O2} \cdots V_{O10}$) corresponding to a particular input common-mode voltage. A variable DC voltage source was used for generating a DC voltage $V_x = 2 \cdots 10V$ ($2V$ steps), simultaneously applied to both the inputs of the analogue front-end. The focus of interest was on the $DC\,CMRR$ of the difference stage (green part in Fig.2.5). Therefore, an RC low-pass filter (R = 820 k, C = 10 nF) was used to remove disturbances with frequency content above $20\,Hz$. At each step, a common-mode voltage equal to the output of the variable DC source was applied to the circuit.

In Fig.10.11, the results of the repeated measurements are depicted with 1-sigma uncertainty on 30 measurements for each point.

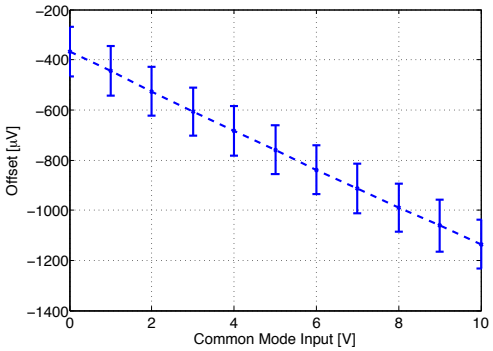

Figure 10.11 – Measured Output Offset V_{Ox} vs Common-Mode Input Voltage V_x ($1-\sigma$ Uncertainty)

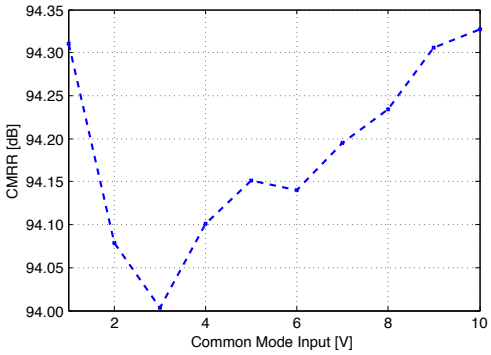

Figure 10.12 – CMRR vs Common-Mode Input Voltage ($1-\sigma$ Uncertainty)

The Common-Mode Rejection Ratio is computed as:

$$CMRR_{diff} = 20Log_{10}\left(\frac{G \cdot V_x}{|V_{Ox} - V_{Osc}|}\right) \tag{10.1}$$

where G is the gain of the front-end ($G = 4\,V/V$), V_x the corresponding common-mode input, V_{Ox} and V_{Osc} the offset measured when $x\,V$ are applied to the inputs and when both the inputs are shorted to ground (first phase), respectively.

In Fig.10.12, the $DC\,CMRR$ is reported with respect to the applied common-mode input voltage. A considerable result of about $94.5\,dB$ in nominal working conditions ($V_x = 10\,V$) is highlighted.

10.5 AC CMRR Test

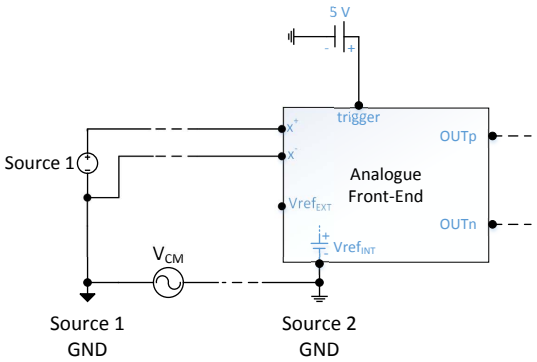

Figure 10.13 – Ground Loop Between Two Far Grounds

The input stage of the analogue front-end is composed of a differential sensing circuit (in violet in Fig.2.5) [5], which rejects the common-mode voltage $CMRR_{ref}$ between the two grounds in order to avoid loops (Fig.10.13).

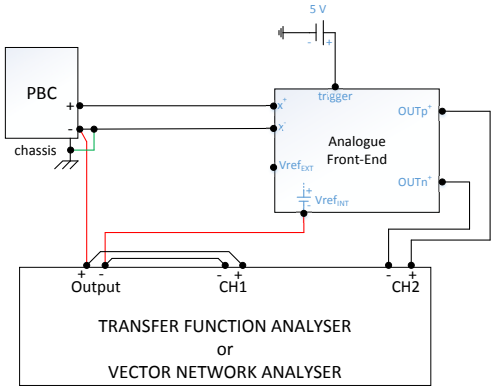

Figure 10.14 – $CMRR_{ref}$ Measurement Setup

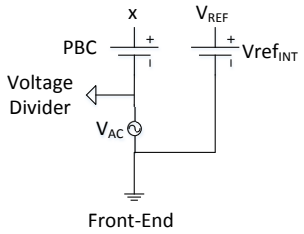

Figure 10.15 – $V_{[}CM]$ Definition

The test setup of Fig.10.14, already used in [38], allows $CMRR_{ref}$ to be assessed over a frequency range of 1 MHz. In this test, the common-mode voltage was imposed between the references of two DC generators. A Transfer Function Analyzer, TFA (also known as Frequency Response Analyzer or Gain Phase Analyzer), Powertek GP 102 was used to generate a set of sine waves (2 V amplitude), ranging in frequency from 10 mHz to 1 MHz. The sine waves were applied between the chassis reference of a fully floating DC 10 V portable generator ($PBCs$) [46], and the local ground of the analogue front-end. The PBC, in turn, fed the signal input of the front-end by fixing the static working point at 10 V. Amplitude and phase (difference) of the input sine waves and the output of the front-end were then measured by the TFA in order to determine the Bode diagram.

In this test, the PBC emulates the signal from the voltage divider, whereas the V_{ref} input is connected to the internal 10 V_{DC} reference voltage (V_{ref}^{INT}) by means of the switch S_1. The test setup in Fig.9.5 highlights how the chassis of the PBC is connected to the negative terminal of the signal input x on the front-end, which is a differential input (not connected to the local ground). On the contrary, the reference voltage of V_{ref}^{INT} is directly connected to the front-end's ground. Fig.10.15 shows how V_{AC} is combined at the input stage and highlights the common mode voltage actually experienced by the front-end:

$$V_{CM} = \frac{x+V_{REF}}{2} = \frac{(V_{PBC1}+V_{AC})+V_{ref}^{INT}}{2} = 10\,V + \frac{V_{AC}}{2} \tag{10.2}$$

The DC part of equation (10.2) (10 V) was rejected as explained in section 10.4, while the rejection of $V_{AC}/2$ is the actual purpose of this test. Analogously as the $CMRR_{diff}$ in (10.1),

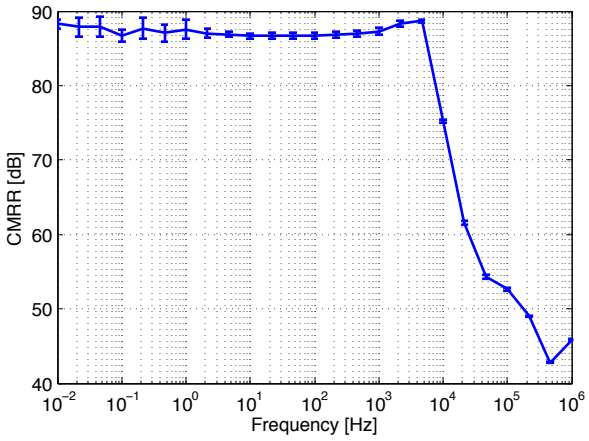

Figure 10.16 – $CMRR$ of the Circuit for Rejecting Common Mode Voltage Between the Voltage Divider and the Local Ground (1-$sigma$ uncertainty)

$CMRR_{ref}$ can be defined as:

$$\begin{aligned} CMRR_{ref} &= 20 \cdot Log_{10}\left(\frac{G_D}{G_{CM}}\right) = 20 \cdot Log_{10}\left(\frac{G_D V_{CM}}{V_{out}}\right) = \\ &= 20 \cdot Log_{10}\left(\frac{G_D V_{AC}}{2 \cdot V_{out}}\right) = \\ &20 \cdot Log_{10}\left(\frac{G_D V_{AC}}{V_{out}}\right) - 20 \cdot Log_{10}(2) \end{aligned} \tag{10.3}$$

where G_D and G_{CM} are the differential and common-mode gains, respectively and V_{out} is the voltage output of the analogue front-end. This shows that a correction factor of $-20 \cdot Log_{10}(2)$ should be applied to the instrument reading. The average results obtained over 10 repetitions with the $1-\sigma$ uncertainty are shown in Fig.10.16. The $CMRR_{ref}$ of about $87\,dB$ up to $5\,kHz$, decreases at higher frequencies down to about $45\,dB$ at $1\,MHz$ which is still a considerable result.

10.6 Full-Signal Acquisition and Pulse-to-Pulse Repeatability Test

The test setup in Fig.10.17 allows the full reconstruction of a $10\,V$ signal to be verified and the experimental Pulse-to-Pulse Repeatability (PPR) to be assessed. The floating generator *PBC* [46] emulates the voltage of the voltage divider by providing a $10\,V$ signal at the input of the analogue front-end. The nominal working conditions are emulated by shorting the negative terminal of the *PBC* to a fixed potential, different from the front-end's ground. The *ADC AD*7625, controlled by its commercial evaluation board, digitizes at $3\,MS/s$ the input signal conditioned according to the working principle of the front-end. At the same time, the *ADC AD*7634, by its evaluation board, acquires at $600\,kS/s$ the internal reference voltage ($Vref_{INT}$), which is subtracted to the input signal in order to be centered around zero. In

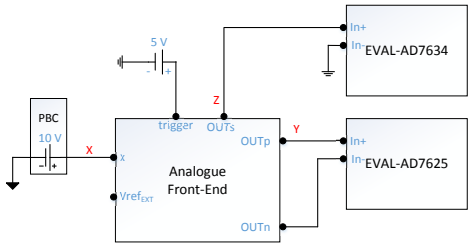

Figure 10.17 – Test Setup for full signal reconstruction and PPR measurement

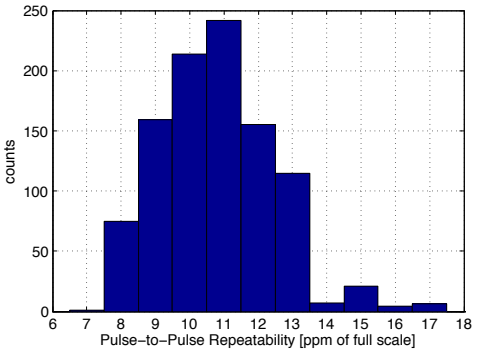

Figure 10.18 – Pulse-to-Pulse Repeatability in nominal working conditions

post-processing, the signal coming from $AD7625$ is filtered and decimated as discussed in section 3.3.3, in order to reduce the final throughput to $600\,kS/s$. Furthermore, offset and gain compensation both for the analogue front-end and the two ADCs was applied according to equation (3.3).

The post-processing operations for reconstructing the original signal are:

$$X_k = Z_k + \frac{1}{N \cdot G^m} \sum_{i=1}^{N} (Y_i - Ox^m) \tag{10.4}$$

The subscript k points out that data are delivered at $600\,kS/s$, whereas the variable Y_i needs to be averaged and decimated by a factor $N = 5$ in order to be combined with Z_k. G^m is the overall gain of the analogue front-end obtained as the average of the first 10 points of Fig.10.12. Ox^m is the offset of the front-end when working in nominal working conditions. For this calibration, the analogue front-end input was connected to a $10\,V$ source (PBC) and the corresponding offset was measured by a digital multimeter (model HP3458A). In this configuration, the measured offset is given by the difference between the input $10\,V$ (PBC) and the internal reference ($LT1236$), amplified by the front-end's gain. Thus, the variable X_k was measured

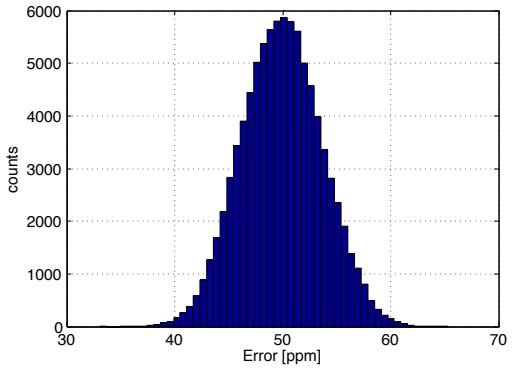

Figure 10.19 – Online Reference System Accuracy

1000 times (each acquisition lasts 150 μs, which are the nominal working conditions) and the PPR definition of equation (3.1) was applied in order to obtain the histogram depicted in Fig.10.18. The PPR is always below the threshold of 18.6 ppm as expected from the calculation of section 3.3.4, by confirming the achievement of the main design parameter of the $CLIC$ application.

Finally, though the $CLIC$ application requirements only concern repeatability (in particular Pulse-to-Pulse Repeatability as defined in equation (3.1)), also the accuracy of the proposed digitizer was assessed by means of the test setup of Fig.10.17. The *PBC* generator was calibrated by the Swiss Federal Institute of Metrology, *METAS*, (2−steps traceability). After gain and offset compensation, the digitizer measured the *PBC* output voltage by showing an accuracy in the order of 50 ppm (mode of the histogram in Fig.10.19).

Conclusions

In this PhD thesis, the challenges related to the characterization and the active control of a pulsed power converter for particle accelerator structures have been addressed.

First, an analytical model, based on a type-A approach for characterizing the Worst-Case Uncertainty of a measurement instrument, has been presented and detailed for an instrument affected by Gaussian noise. Numerical simulations demonstrated its effective capability of fitting the actual distribution and, thus, validated the model. The model was also verified by comparing predicted and experimental distributions measured by means of the reference acquisition system for the CLIC klystron modulators at CERN (where the requirements concern the Worst-Case Repeatability). However, the model can be generalized for any measurement system by simply characterizing its instrumental noise (assumed to be white and Gaussian) in terms of standard deviation, to be provided as input to the model. As a matter of fact, the model allows the WCU of a measurement system to be predicted for any sample size and this analytical tool can be used to formalize the uncertainty requirements of a measurement system.The model can be generalized for any measurement system if the statistical distribution of the instrumental noise is known.

As said, the *WCU* model was also validated by means of the Reference Acquisition System for the CLIC klystron modulators. The design of this custom instrument has been presented and experimental test setups demonstrated unprecedented performance. In particular, a $CMRR$ of more than $87\,dB$ in *DC*, consistent with the design expectations was verified. The system showed also a 3-sigma offset stability of about $\pm 0.65\ ppm$ over about 24 hours. The temperature coefficient was estimated to be less than $0.1\ ppm/°C$ in the worst-case condition of fast temperature variations, while humidity dependency was shown to be negligible even for high variations of humidity (from 30 % up to 70 %). This is an important result, in fact, such a so robust instrument against temperature fluctuations excludes the need for a water cooling system, by significantly improving the instrument usability. Finally, the Worst-Case Repeatability, the main instrument quality figure, was assessed to be less than $\pm 25\ ppm$.

The last topic addressed in this PhD thesis is the proof of principle of a custom analogue front-end of a real-time digitizer for controlling the high-voltage of $CLIC$ power converters has been presented. Starting from the requirements, the concept design and a physical architecture are presented and discussed. Pspice simulations were performed to demonstrate the effectiveness

of the proposed architecture with respect to the defined requirements. Experimental test setups allowed the performance of the prototype developed at CERN to be assessed, by highlighting also compatibility with the design simulation results. In conclusion, while noise, bandwidth, $DCCMRR$ and Pulse-to-Pulse Repeatability (PPR) were demonstrated to be comfortably inside the requirements, delay turned out to be very critical at the required bandwidth, even if still inside the specification.

A APPENDIX: Rigorous Formula for WCU Distribution

In this section, the actual *WCU* distribution is derived analytically, by proving also that the distribution (1.13) is a worst-case approximation of the actual distribution in the case of white and Gaussian noise $n(t)$ of the measurement system.

A.0.1 WCU for a Given Sample Size with Gaussian Noise

In this subsection, the rigorous equation of the *WCU* distribution is presented and discussed. The assumption of whiteness and Gaussianity of the stochastic process $n(t)$ (introduced in section 1.2.1) guarantees both the symmetry and the $i.i.d.$ hypotheses, therefore each $V_{i,j}$ is distributed as $\mathcal{N}(\mu_i, \sigma^2)$. These samples, $1 \leq j \leq N_p$, can be rearranged in a random vector $V_i \sim \mathcal{N}_{N_p}(\boldsymbol{\mu_i}, \boldsymbol{\Sigma})$, with $N_p \times N_p$ co-variance matrix $\boldsymbol{\Sigma}$:

$$\boldsymbol{\Sigma}_{N_p \times N_p} = \begin{pmatrix} \sigma^2 & 0 & 0 & 0 & \cdots \\ 0 & \sigma^2 & 0 & 0 & \cdots \\ 0 & 0 & \sigma^2 & 0 & \cdots \\ 0 & 0 & 0 & \sigma^2 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \end{pmatrix} = \sigma^2 \cdot \boldsymbol{I}_{N_p \times N_p} \tag{A.1}$$

The difference random variables $Y_i = V_{i,j} - V_{i,j+1}$, $1 \leq j \leq N_o = N_p - 1$, can also be arranged as a random vector:

$$Y_i = \mathbf{M} V_i \tag{A.2}$$

where the transformation matrix **M** is described as:

$$\mathbf{M}_{N_o \times N_p} = \begin{pmatrix} 1 & -1 & 0 & 0 & \cdots \\ 0 & 1 & -1 & 0 & \cdots \\ 0 & 0 & 1 & -1 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \end{pmatrix} \tag{A.3}$$

The random vector Y_i is therefore jointly Gaussian and $Y_i \sim \mathcal{N}_{N_o}(\mathbf{M}\boldsymbol{\mu_i}, \mathbf{M}\boldsymbol{\Sigma}\mathbf{M}^T)$ [48].

The N_o-dimensional joint *PDF* has a pretty simple form; indeed $Y_i \sim \mathcal{N}_{N_o}(\mathbf{0}, \sigma^2\mathbf{M}\mathbf{M}^T)$, therefore:

$$f_{Y_i} = f_{Y_i}(Y_1, ..., Y_{N_o}) = \frac{e^{-\frac{1}{2}\mathbf{y}^T(\sigma^2\mathbf{M}\mathbf{M}^T)^{-1}\mathbf{y}}}{\sqrt{(2\pi)^{N_o}\left|\sigma^2\mathbf{M}\mathbf{M}^T\right|}} = \frac{e^{-\frac{1}{2}\mathbf{y}^T(\sigma^2\mathbf{M}\mathbf{M}^T)^{-1}\mathbf{y}}}{\sqrt{(2\pi)^{N_o} \cdot N_p} \cdot \sigma^{N_o}} \tag{A.4}$$

The expression (A.4) exploits the following identities:

$$N_o = rank\left\{\mathbf{M}\mathbf{M}^T\right\} \tag{A.5}$$

$$\left|\sigma^2\mathbf{M}\mathbf{M}^T\right| = N_p \cdot \sigma^{2N_o} \tag{A.6}$$

The covariance matrix of Y_i also has a very simple structure:

$$\left(\sigma^2\mathbf{M}\mathbf{M}^T\right)_{N_o \times N_o} = \sigma^2 \begin{pmatrix} 2 & -1 & 0 & 0 & \cdots \\ -1 & 2 & -1 & 0 & \cdots \\ 0 & -1 & 2 & -1 & \cdots \\ 0 & 0 & -1 & 2 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \end{pmatrix} \tag{A.7}$$

Expression (A.7) clearly shows that adjacent samples, with respect to j, are not independent since the covariance matrix is not diagonal, but statistic dependence is limited to adjacent samples only, therefore the covariance matrix structure is rather simple.

The *PDF* of Y_i is therefore completely known, and the independence on i can be now exploited

fully to obtain the distribution of $WCU(N_o)$. $WCU(N_o)$ can be rewritten as $WCU(N_o) = Z = max_j \{max_i |Y_{i,j}|\}$, where $1 \leq j \leq N_o$, $1 \leq i \leq N_s$.

By swapping the order of the *maximization*, the *CDF* of $z_i = max_j |Y_{i,j}|$ can be calculated:

$$F_{z_i}(z) = Pr\{z_i \leq z\} = Pr\{|Y_{i,j}| \leq z\} = Pr\{-z \leq Y_{i,j} \leq z\} = \underbrace{\int_{-z}^{z} \cdots \int_{-z}^{z}}_{N_o} f_{Y_i} d\mathbf{y} \tag{A.8}$$

The independence upon i allows the CDF of $WCU(N_o)$ to be calculated by simply raising to the N_s^{th} power the CDF of z_i written in (A.8). The next equation summarizes all the involved parameters:

$$F_{WCU(N_o)}(z) = \left[\underbrace{\int_{-z}^{z} \cdots \int_{-z}^{z}}_{N_o} \frac{e^{-\frac{1}{2}\mathbf{y}^T(\sigma^2 \mathbf{M}\mathbf{M}^T)^{-1}\mathbf{y}}}{\sqrt{(2\pi)^{N_o} \cdot (N_o+1)} \cdot \sigma^{N_o}} d\mathbf{y} \right]^{N_s} \tag{A.9}$$

It is worth noting that the approach used to derive (A.9) is reversed with respect to the one used in 1.2.2; first the *maximization* over j, dealing with statistic dependence, and then over i exploiting the statistic independence. In section A.0.2, equation (1.12) is proven to be the *CDF* of a random variable Z^{ind} that is a *worst case* of the random variable $WCU(N_o)$ in the sense of the stochastic dominance.

A.0.2 Dominant Approximation of WCU for a Given Sample Size with Gaussian Noise

As asserted in 1.2.2, it can be proven that (1.12) is the *CDF* of a random variable Z^{ind} that is a *worst case* of the random variable $WCU(N_o)$ in the sense of the stochastic dominance:

$$Z^{ind} \succeq WCU(N_o) \Longleftrightarrow F_Z^{ind}(z) \leq F_{WCU(N_o)}, \forall z \tag{A.10}$$

From equations (A.8) and (A.9) it yields that $F_{WCU(N_o)}(z) = F_{z_i}^{N_s}(z)$. In [49] and [50] an inequality, found in the early $60's$, is presented, which is equivalent to *Slepian's* inequality [51] for the absolute value of Gaussian random vectors. For any N-dimensional Gaussian vector U, this

inequality states that:

$$Pr\{|U_1| \leq u_1, |U_2| \leq u_2, \cdots, |U_N| \leq u_N,\} \geq \prod_{j=1}^{N} Pr\left\{\left|U_j\right| \leq u_j\right\} \tag{A.11}$$

Inequality (A.11) shows that the joint *CDF* of dependent and jointly Gaussian random variables is always greater than or equal to the joint *CDF* of the same random variables assumed independent in the sense of factorizing the marginal *CDFs*. Such inequality can be particularized for $N = N_o$, $u_j = z, \forall\, j$ and $U_j = Y_{i,j}$ as follows:

$$F_{z_i}(z) = Pr\left\{\left|Y_{i,1}\right| \leq z, \left|Y_{i,2}\right| \leq z, \cdots, \left|Y_{i,N_o}\right| \leq z,\right\} \geq \prod_{j=1}^{N_o} Pr\left\{\left|Y_{i,j}\right| \leq z\right\} = F_{|Y_i|}^{N_o}(z) \tag{A.12}$$

The right hand equality exploits equation (1.5) and the now fully justified $i.i.d.$ hypothesis (actually only identical distributions are needed given the already factorized probabilities). Given the independence on i, both the sides of inequality (A.12) can now be raised to N_s^{th} power; by means of (1.12) and (A.9) it is eventually possible to write:

$$F_{WCU(N_o)}(z) = F_{z_i}^{N_s}(z) \geq F_{|Y_i|}^{N_o \cdot N_s}(z) = F_{Z^{ind}}(z) \tag{A.13}$$

It is worth noting that inequality (A.11) is not a direct result of *Slepian's* inequality; indeed for the case under study here, extending the lower integration limit to $-\infty$ in (A.9) would have given exactly the opposite result.

The covariance matrix of Y_i, assumed to be independent as done in 1.2.2, would be:

$$\mathbf{\Sigma}_{Y_i\, N_o \times N_o} = 2\sigma^2 \boldsymbol{I}_{N_o \times N_o} \tag{A.14}$$

Hence, $\mathbf{\Sigma}_{Y_i}(q,k) \leq \sigma^2 \mathbf{M}\mathbf{M}^T(q,k)\ \forall\, q,k$ and, due to *Slepian's* inequality, the exact CDF of the maximum of Y_i (instead of $|Y_i|$) would have been smaller or equal to the approximated one obtained by neglecting statistical dependence.

In conclusion, for white Gaussian instrumental noise, the PDF of $WCU(N_o)$ can therefore be approximated in the worst-case sense through (1.13), by simply assuming $Y_i \sim \mathcal{N}(0, 2\sigma^2)$.

Bibliography

[1] N. Mohan and T. Undeland, *Power electronics: converters, applications, and design*. Wiley India, 2007.

[2] C. Attaianese, M. Di Monaco, and G. Tomasso, "High performance power converter for combined batteries-supercapacitor systems," in *Electrical Machines (ICEM), 2010 XIX International Conference on*, pp. 1–6, 2010.

[3] W. Martinez and C. Cortes, "High power density interleaved DC-dc converter for a high performance electric vehicle," in *Power Electronics and Power Quality Applications (PEPQA), 2013 Workshop on*, pp. 1–6, 2013.

[4] S. Zabihi, F. Zare, G. Ledwich, and A. Ghosh, "A new generation of high voltage pulsed power converters," in *Universities Power Engineering Conference (AUPEC), 2010 20th Australasian*, pp. 1–5, 2010.

[5] P. Arpaia, C. Baccigalupi, M. Bastos, and M. Martino, "± 25 ppm Repeatable Measurement of Trapezoidal Pulses with 5 MHz Bandwidth," *JJournal of Instrumentation (JINST)*, vol. 9, p. P06002, 2014.

[6] M. Souders, J. Andrews, A. Caravone, J. Deyst, C. Duff, and S. Naboicheck, "A Pulse Measurement Intercomparison," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 5, pp. 1031–1036, 1998.

[7] "IEEE Standard for Transitions, Pulses, and Related Waveforms," 181-2011 (Revision of 181-2003).

[8] P. Arpaia, C. Baccigalupi, and M. Martino, "Type-A Worst-Case Uncertainty for Gaussian Noise Instruments," *Journal of Instrumentation*, vol. 10, p. P07007, 2015.

[9] G. Potter, "An Introduction to Digital Control of Switching Power Converters," tech. rep., Emerson Network Power, 2004.

[10] P. Arpaia, C. Baccigalupi, M. Bastos, and M. Martino, "Proof of Principle of an On-Line Digitizer with ±18 ppm Repeatability and 1.2 μs Real-Time for Power Converters Control Loop.," *to be submitted to ISA Transactions*, 2015.

[11] M. Battaglia, A. De Roeck, J. Ellis, and D. Schulte, "Physics at the CLIC Multi-TeV Linear Collider," tech. rep., Report of the CLIC Physics Working Group, CERN report, ref. hep-ph/0412251; CERN-2004-005, 2004.

[12] M. Aicheler, P. Burrows, M. Draper, T. Garvey, P. Lebrun, K. Peach, N. Phinney, H. Schmickler, D. Schulte, and N. Toge, "A Multi-TeV linear collider based on CLIC technology: CLIC Conceptual Design Report," tech. rep., CERN, 2012.

[13] D. Aguglia, C. Martins, M. Bastos, D. Nisbet, D. Siemaszko, E. Sklavounou, and P. Viarouge, "Klystron modulator technology challenges for the compact linear collider (clic)," in *Pulsed Power Conference (PPC), 2011 IEEE*, pp. 1413–1421, 2011.

[14] D. Aguglia, C. Martins, M. Cerqueira Bastos, D. Nisbet, D. Siemaszko, E. Sklavounou, and P. Viarouge, "Klystron Modulator Technology Challenges for the Compact Linear Collider (CLIC)," in *Pulsed Power Conference (PPC), 2011 IEEE*, pp. 1413–1421, 2011.

[15] W. Nunnally and T. Engel, "REVIEW OF KLYSTRON MODULATOR TECHNOLOGY FOR PARTICLE ACCELERATORS," in *Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International*, vol. 2, pp. 967–970, 1999.

[16] S. Blume and J. Biela, "Design procedure of an active bouncer for an ultra precise long pulse solid state modulator," in *Pulsed Power Conference (PPC), 2013 19th IEEE*, pp. 1–6, 2013.

[17] F. C. Magallanes, D. Aguglia, P. Viarouge, C. D. A. Martins, and J. Cros, "A novel active bouncer system for klystron modulators with constant AC power consumption," in *Pulsed Power Conference (PPC), 2013 19th IEEE*, pp. 1–6, 2013.

[18] K. Thotahewa and M. Yuce, "Analysis of Pulse Based UWB Transmission Techniques for Wireless Sensors," in *Communications and Information Technologies (ISCIT), 2012 International Symposium on*, pp. 245–250, 2012.

[19] F. Attivissimo, N. Giaquinto, and M. Savino, "Worst-Case Uncertainty Measurement in ADC-based Instruments," *Computer Standards & Interfaces*, vol. 29, p. 5, 2007.

[20] "Guide to the Expression of Uncertainty in Measurement."

[21] W. Bich, M. Cox, R. Dybkaer, C. Elster, W. Estler, B. Hibbert, H. Imai, W. Kool, C. Michotte, L. Nielsen, Nielsen, L. Pendrill, S. Sidney, A. van der Veen, and W. Woger, "Revision of the 'Guide to the Expression of Uncertainty in Measurement'," *IOP Metrologia*, vol. 49, p. 6, 2012.

[22] R. Brown, "Using a Manufacturer s Specification as a Type B Error Contribution," tech. rep., Agilent Technologies, Santa Clara U.S.A., 2012.

[23] L. Fabbiano, N. Giaquinto, M. Savino, and G. Vacca, "Observations On the Worst Case Uncertainty," in *J. Phys.: Conf.Ser. 459*, 2013.

[24] N. p. Hu, "Research on Price Risk of Soybean Market Based on Extreme Value Theory," in *Management Science and Engineering, 2009. ICMSE 2009. International Conference on*, pp. 824–830, 2009.

[25] L. Xiu-Min and L. Fa-Chao, "Extreme Value Theory: An Empirical Analysis of Equity Risk for Shanghai Stock Market," in *International Conference on Service Systems and Service Management*, vol. 2, pp. 1073–1077, 2006.

[26] J. Einmahl and S. S., "Ultimate 100 m World Records through Extreme-Value Theory," *CentER Discussion Paper Series No. 59*, vol. July, 2009.

[27] J. Tawn, "Estimating Probabilities of Extreme Sea-levels," *Appl. Statist.*, vol. 41, pp. 77–93, 1992.

[28] R. Duperrier and D. Uriot, "The extreme value theory to estimate beam losses in high power linacs," in *Particle Accelerator Conference, 2007. PAC. IEEE*, pp. 815–819, 2007.

[29] S. Wei, D. Goeckel, and P. Kelly, "A Modern Extreme Value Theory Approach to Calculating the Distribution of the Peak-to-Average Power Ratio in OFDM Systems," in *Communications, 2002. ICC 2002. IEEE International Conference on*, vol. 3, pp. 1686–1690, 2002.

[30] Y. Zhang, X. Li, and M. G. Amin, "Real-time acquisition and tracking of sniper bullets using multi-sensor multi-frequency radar techniques," in *Statistical Signal Processing, 2009. SSP '09. IEEE/SP 15th Workshop on*, pp. 265–268, 2009.

[31] K. Enisz, D. Fodor, I. Szalay, and L. Kovacs, "Reconfigurable real-time hardware-in-the-loop environment for automotive electronic control unit testing and verification," *IEEE Instru Meas Mag*, vol. 17, no. 4, pp. 31–36, 2014.

[32] IEEE, "Standard for Digitizing Waveform Recorders, (Revision of IEEE 1057-1994), 2008," 2007.

[33] S. Coles, *An Introduction to Statistical Modeling of Extreme Values*. Springer, 2001.

[34] M. Cerqueira Bastos, M. Hammarquist, and A. Bergman, "A High-Voltage Test Bed for the Evaluation of High-Voltage Dividers for Pulsed Applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 7, pp. 2462–2468, 2011.

[35] K. Bennett, "Metrology Concepts: Understanding Test Uncertainty Ratio (TUR)," in *Calibrate with Confidence*, TRANSCAT Calibration & Repair Services, 2005.

[36] K. Lokere, T. Hutchison, and G. Zimmer, "Precision Matched Resistors Automatically Improve Differential Amplifier CMRR," tech. rep., Linear Technology, 2012.

[37] A. Corporation, "Enhancing adc resolution by oversampling," tech. rep., Application Note, 2005.

[38] P. Arpaia, C. Baccigalupi, and M. Martino, "Enhanced analogue front-end for the measurement of the high state of wide-band voltage pulses with 87 db common-mode rejection ratio and ± 0.65 ppm 1-day offset stability," *AIP RSI*, vol. 86, p. 9, 2015.

[39] M. A. L.K. Maheshwari, *Analog Electronics*, vol. 5.5. Prentice-Hall of India, 2006.

[40] W. Nunnally and T. Engel, "Review of Klystron Modulator Technology for Particle Accelerators," in *Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International*, vol. 2, pp. 967–970, 1999.

[41] "IEEE standard for transitions, pulses, and related waveforms," 2011.

[42] "International Vocabulary of Metrology - Basic and General Concepts and Associated Terms (VIM)."

[43] V. E. Johnson, "Revised Standards for Statistical Evidence," *Proceedings of the National Academy of Sciences*, vol. 110, no. 48, pp. 19313–19317, 2013.

[44] M. Martino, R. Losito, and A. Masi, "Analytical Metrological Characterization of the Three-Parameter Sine Fit Algorithm," in *ISA Transactions*, vol. 51, pp. 262–270, March 2012.

[45] M. Bertocco, C. Narduzzi, P. Paglierani, and P. D., "A Noise Model for Digitized Data," vol. 49, no. 1, pp. 83–86, 2000.

[46] G. Fernqvist, G. Hudson, J. Pickering, and F. Power, "Design and Evaluation of a 10-mA DC Current Reference Standard," *IEEE Transactions on Instrumentation and Measurement*, vol. 52, no. 2, pp. 440–444, 2003.

[47] R. Mancini, "Op Amps For Everyone, chapter 11, page 15," tech. rep., Texas Instruments, 2002.

[48] Y. Tong, *The Multivariate Normal Distribution*. Springer, 1990. ISBN-13:978-1-4613-9657-4.

[49] Z. Sidak, "On Probabilities of Rectangles in Multivariate Student Distributions: The Dependence on Correlations," *The Annals of Mathematical Statistics*, vol. 42, pp. 167–175, 1971.

[50] M. Halperin, "An Inequality on a Bivariate Student's "t" Distribution," *Journal of the American Statistical Association*, vol. 62, pp. 603–606, 1967.

[51] D. Slepian, "The One-Sided Barrier Problem for Gaussian Noise," *The Bell System Technical Journal*, vol. 41, p. 468, 1962.