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UNIVERSITA' DELLA CALABRIA

Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica

Dottorato di Ricerca in

Information and Communication Technologies (ICT)

CICLO

XXXIII

Phased array building blocks for 5G networks

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Abstract

5G will have to support a multitude of new applications with a wide variety of requirements, including higher user data rates and network capacity, reduced latency, improved energy efficiency, and so on. These aspects will lead to a radical change in network architecture from different points of view. For example, the densification of small cells in the access network will produce massive traffic to the core network and an increment of the interference due to the lower inter-cell distance. In particular, millimeter waves (mm-waves) bands, due to their large unlicensed and lightly licensed bandwidths, have become a promising candidate for the next-generation wireless communications, to accommodate users demand for multi-Gbps data rates, but this will move the attention to the complexity and the criticality of the base station antenna systems. In fact, because of the carrier frequency increment, it will be necessary to use large-scale antennas to compensate channel losses which are significant in the millimeter wave bands. Furthermore, the combined use of phased arrays and massive MIMO technologies will be required to achieve a better usage of the radio channel, by implementing more accurate spatial selectivity techniques, thus resulting in an increased network capacity and signal-to-noise (SNR) performance. Among the spectrum portions used in the access segment, the Ka-band is the most interesting and attractive to implement low-cost wideband antenna systems with high steering capability along both azimuth and elevation directions and good performance in terms of directivity. On the other side, the shift to higher frequencies required by these systems will imply a decrease in the space available for the integration of the chip containing the transceiver and all the necessary RF circuitry. Therefore, hardware

integration will be a key element to be taken into consideration for the development of the fifth-generation phased array systems.

The main object of this work is to analyze and design different building blocks of phased array systems operating in Ka-band for 5G applications. The research activities presented in this dissertation can be summarized into two parts. In the first part, a 32-element dual-polarized array operating in n257 band (26.5-29.5 GHz) for 5G phased array systems is presented, where a novel ultra-low profile dual-polarized Magneto-Electric dipole has been employed as the radiating element. This array system has been thought to be used in a 5G small cell, where the radiated beam should be directed along azimuth and elevation considering the scan range ($\pm 55° AZ, \pm 20° EL$) to increase both spatial selectivity and network capacity.

In the second part, the attention has been focused on the study and the design of variable gain amplifiers (VGAs) in a standard 0.13 μm SiGe BiCMOS technology for 5G phased array applications. At first, the performance of a Ka-band conventional single-stage NMOS voltage variable attenuator (VVA) has been compared with a novel Ka-band hybrid single-stage VVA with improved power handling capability and linearity, where two shunt HBT transistors act as varistors to change continuously the attenuation state of the cell. At this point, a monolithically-integrated dual-stage VGA with higher power capability and wider gain tuning range based on the use of VVA circuit as control element has been developed. This component should be employed directly as an end-stage variable gain PA in Si-based 5G transmitters or as a driver in hybrid Si/GaN-based or Si/GaAs-based 5G transceivers.

Table of contents

List of figures

List of tables

1 5G Network

1.1 Introduction to 5G Networks

The exponential growth of connected devices and the huge amount of data required by latest applications as Internet-of-Things (IoT), machine-to-machine communications, smart homes/cities, Cloud Computing, Video Gaming, Augmented-Reality, Real-time control, etc. are bringing to light the limitations of the current network architecture for mobile telecommunications, 4G [1]. To overcome these technological limits, research laboratories and industries are investing in terms of human and economic effort to aim for the definition of a new fifth-generation network infrastructure whose acronym is 5G. This system targets higher data rates and capacity, lower latency, better cost, and energy efficiency to meet these new requirements. In particular, International Telecommunication Union (ITU) has outlined challenging specifications as seen in **Figure 1-1**: Peak data rates up to 10 Gb/s with a minimum cell-edge data rate of 1 Gb/s, spectral efficiency close to 10 bps/Hz, mobility up to 500 km/h, cost efficiency at least 10x better than 4G, 1M simultaneous connections per km^2 and End-to-End (E2E) latency of 1 ms [1][2].

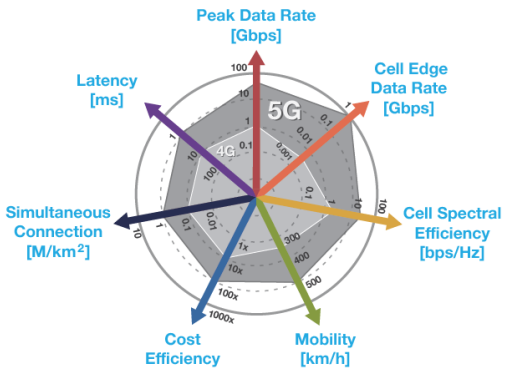


Figure 1-1: 5G requirements overview [1].

In light of this, the newest 5G system will be based on innovative technologies and the use of a new and performing network infrastructure that will be able to coexist and cooperate with other existing wireless technologies. Higher data rates can be achieved using *mm-wave bands* (30-300 GHz) that offer more bandwidth compared to the ones in the sub-6GHz spectrum. ITU-R has identified several frequency bands into the mm-wave spectrum, which are classified based on specific usage scenarios (e.g. eMBB=enhanced Mobile BroadBand, URLLC=Ultra-Reliable Low-Latency Communication) as reported in **Table 1-1** [3][4][5]:

Table 1-1: 5G millimeter-wave band allocation.

	Usage Scenarios
K band 24.25 – 27.5 GHz (n258)	eMBB URLLC
Ka band 26.5 – 29.5 GHz (n257) 27.5 – 28.35 GHz (n261) 31.8 – 33.4 GHz 37 – 40 GHz (n260)	eMBB, URLLC
V band 39 – 43.50 GHz (n259) 47 – 52.6 GHz	eMBB, URLLC
E band 66 – 71 GHz 71 – 76 GHz 81 – 86 GHz	Backhaul networks

However, as the carrier frequency increases, the losses due to atmospheric absorption and interactions between objects (e.g. buildings, foliage, etc.) increase. Experimental tests have

shown that the atmospheric absorption losses due to the presence of water molecules and oxygen at 28GHz should be 0.02 dB every 200 meters compared to ones calculated at 10GHz that are less than 0.004 dB [1]. Moreover, these values could dramatically increase if heavy rains occur; in fact, the attenuation level at 28GHz could be about 4 dB for LoS (Line-of-Sight) signal propagation. To mitigate the effect of these atmospheric losses, mm-waves 5G systems necessitate the use of *small cells* that will be densely deployed throughout the cities to achieve the required QoS in terms of data rate and network capacity. To further increase the channel capacity and decrease both connection latency and inter-user interference, these small cells will employ the latest *Multi-User (MU) massive MIMO* (Multiple-Input Multiple-Output) technologies. By this approach, since the antenna dimensions are smaller at mm-wave bands, large arrays (whose elements number N can vary from 100 to 1024) can be used to manage more high-gain radiating beams by providing services to a lot of users at the same time [2][6]. To fully exploit the benefits of MIMO technology, the radiating structures will employ "*smart" beam-forming algorithms* to implement channel optimization techniques (e.g. Space Division Multiplexing) by focusing the radiated beams to specific areas (as illustrated in **Figure 1-2**), while reducing the inter-user interference and increasing the channel BER performance.

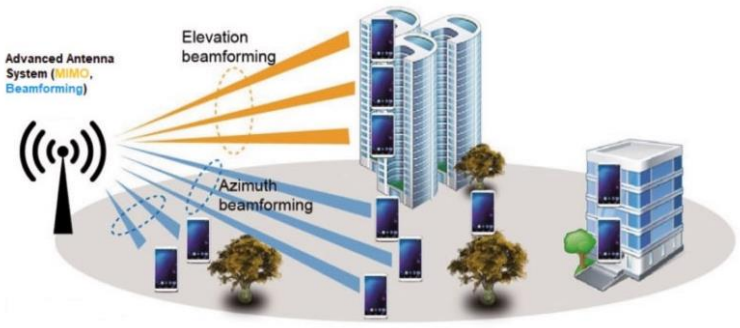


Figure 1-2: MIMO 5G antennas with 2-D beam-forming.

In order to improve the spectral efficiency and to further reduce the network latency, *full-duplex* radio operation is expected as part of 5G networks. Full duplex operation requires very high isolation between transmitting (TX) and receiving (RX) ports to reduce the impact of the multi-beam transmission in terms of mutual interference [2]. Several approaches are investigated to satisfy the full-duplex requirements, such as using two different arrays for separate TX and RX, using circulators and hybrid couplers, or employing a dual-polarization system if TX and RX share the same array. The cooperation and integration between 5G networks and the other existing wireless systems (as. 4G LTE, Wi-Fi, Wi-Max) are one of the key elements to guarantee larger network capacity and data rate per user. Multi-RAT (Radio Access Technology) is the technology used to enable this cooperation. The idea behind multi-RAT is to aggregate licensed and unlicensed bands referred to several applications, thus making "heterogeneous" the entire 5G network as reported in **Figure 1-3** [1][6]. This scenario will lead to better management of the network resources and an increment of global performance.

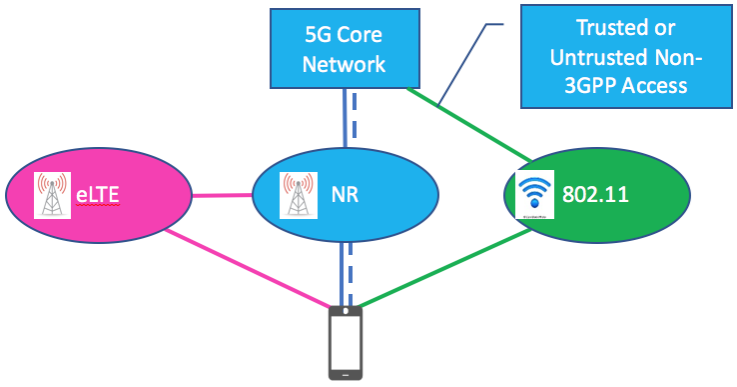
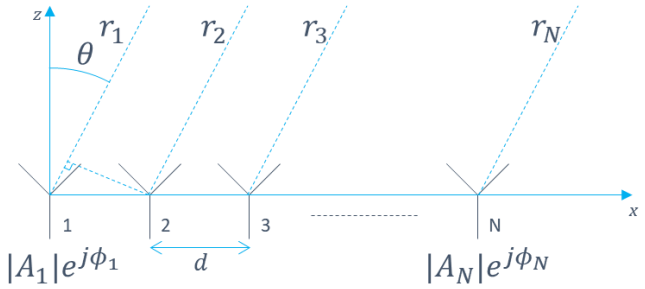


Figure 1-3: 5G multi-RAT scenario.

1.2 Phased arrays as key building blocks in 5G systems

As reported above, one of the innovation keys of the upcoming 5G networks is related to the use of MIMO antenna arrays with embedded 2-D beam-forming functionality. Phased array is the "key" to enable these technologies into the fifth-generation network infrastructure. Phased arrays comprise a radiating structure where N elements, which are arranged on one axis spaced d apart, radiate coherently along the desired direction θ_0 according to the array factor Eq. 1-1:



$$AF(\theta) = \sum_{n=0}^{N} \overline{A_n}\, e^{jkndsin\theta} \qquad \textbf{Eq. 1-1}$$

$$\overline{A_n} = A_n e^{j\phi_n} \rightarrow \phi_n = -kndsin\theta_0$$

To electronically change the phase ϕ_n of each element and, consequently, focus the main lobe along θ_0 direction, a specific control circuit called *phase shifter* should be placed at input/output of radiating structure depending on whether the antenna is working in TX or RX mode. In 5G context, this block will permit to perform beam-forming along two dimensions (azimuth and elevation) to select the desired users while reducing the mutual interference and improving the spatial selectivity of the 5G base stations. Gain control is another crucial point related to the operating of the new 5G base stations. By varying the excitation signal amplitude A_n for each array element, it is possible to change dynamically the antenna gain and, consequently, the EIRP value of the communication link. If a specific

amplitude pattern $A_1 \dots \dots \dots \dots \dots A_n$ is used on the array terminals (based on different distributions e.g. Taylor, Chebyshev, etc.), an amplitude tapering can be applied on the radiation pattern to reduce the side-lobe level (SLL) value and the unwanted inter-user interference. Attenuator and Variable Gain Amplifiers (VGAs) are two circuits designed to perform these functions. By incorporating both phase shifter and attenuator/VGA within a single electronic circuit, called *beam-former*, gain control and beam steering operations could be performed directly on the phased array. **Figure 1-4** reports an example of a hybrid beam-forming system [7]. These two functions can be managed by phase shifters and attenuators in the RF domain and a numeric beam-former in the digital domain.

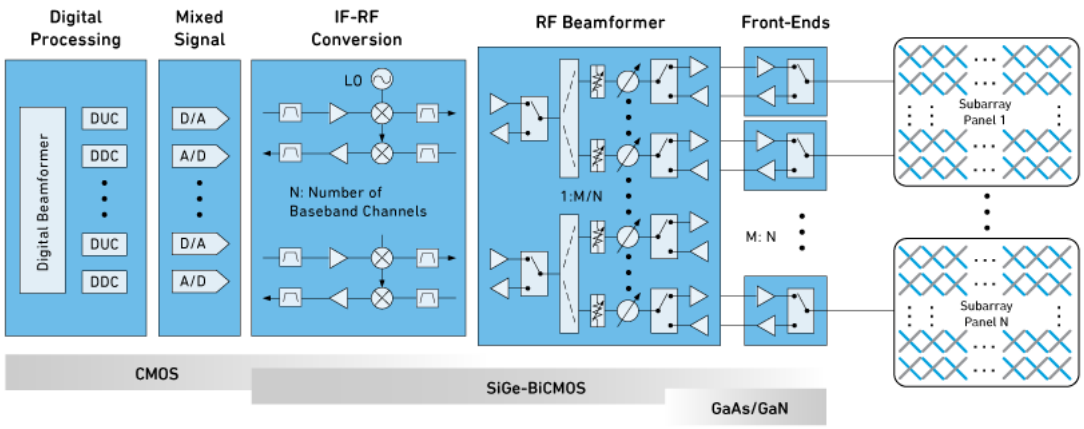


Figure 1-4: Example of a hybrid beam-forming system [7].

Advances in MMIC technologies and their massive use have made commercial mm-wave systems readily available and cost-efficient [1]. As miniaturization levels of the most recent silicon (CMOS, SiGe-BiCMOS) and III-V (GaAs, GaN) technologies are increased, different building blocks as mixers, IF amplifiers, attenuators / VGAs, PAs, LNAs, T/R switches, phase shifters, filters and power combiners/splitters can be integrated all in a single package containing the entire transceiver. Depending on the network scenario in

which phased array systems will be employed, if the required power levels are lower than 20/ 25 dBm and noise figure values are higher than 5dB, the building blocks of TRX, RF beam-former and analog front-end sections could be realized considering a single low-cost CMOS and/or BiCMOS MMIC technology. Otherwise, some building blocks such as Pas, T/R switches and LNAs should be designed in more powerful MMIC processes, as like GaAs or GaN, thus creating a multi-technology structure like the one shown in **Figure 1-4**. By exploiting the increased integration level of the MMIC technologies, mm-wave transceivers and antenna arrays can be incorporated in a single structure to form highly-integrated 5G phased array systems as reported in **Figure 1-5** [8].

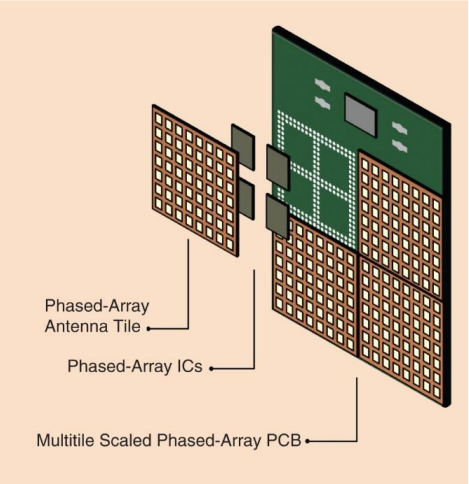


Figure 1-5: Multi-tiles PCB phased array system [8].

1.3 Thesis organization

In this thesis, the design and characterization of building blocks for a 5G phased array system operating in Ka-band will be proposed. A phased array overview, including some details about the integration and packaging and the fundamental concepts regarding the phased arrays theory, will be shown in chapter 2. A specific design flow, which is

defined to characterize phased antenna arrays by Ansys HFSS software, will be reported in chapter 3. To satisfy the requirements of the newest 5G small cells, a 32-elements rectangular array in multi-PCB technology operating at 28GHz, which is based on the use of a novel ultra-low profile dual-polarized Magneto-Electric dipole, will be depicted in chapter 4. The ability to change the gain of the antenna array dynamically and, consequently, control the "shape" of the radiation pattern will be achieved using Variable Gain Amplifiers (VGAs). In this work, an attenuator-based Ka-band Variable Gain PA realized in 0.13um SiGe BiCMOS technology will be shown in chapter 5. In particular, conventional NMOS Voltage Variable Attenuator (VVA) and a novel hybrid NMOS/HBT VVA will be designed and their performance will be analyzed. By using the conventional NMOS VVA circuit as a gain control block, the design aspects and the performance of a 0.13um SiGe BiCMOS dual-stage Variable Gain PA circuit will be reported in detail.

2 Phased arrays

2.1 Introduction

A single radiating element exhibits a relatively low directivity, meaning that the radiation is "uniform" in all directions [2]. By deploying a collection of radiating sources in some ordered lattice, it is possible to create a more directive radiating structure which is called array. Arrays can be planar (mono-dimensional and bi-dimensional lattices) or conformal to some curved surfaces, as reported in **Figure 2-1**. If the phase of each source is controlled properly (i.e. with a constant phase taper between each adjacent element), the main beam can be steered away from the normal direction along a specific area. Moreover,

if the amplitude of each radiating element is controlled properly (i.e. by applying a weighting window), the side lobe levels, as well as beam null positions, can be adjusted accordingly. Therefore, the main role of phased arrays is to improve and to "shape" the radiation energy along a certain direction which can be dynamically changed.

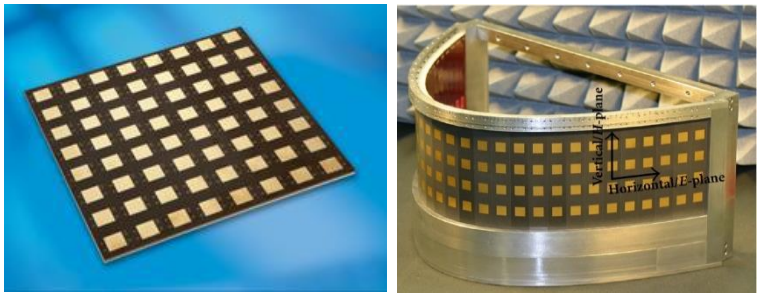


Figure 2-1: Example of antenna arrays. 2-D planar (left); 2-D conformal (right).

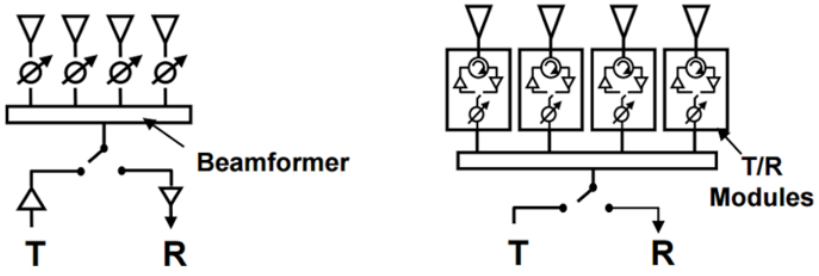
Given the features listed above, the phased array systems have played an important role since the beginning of World War II. One of the first implementations of phased arrays for short-wave reception based on the use of mechanical phase shifters was presented in 1937 by Friis and Feldman [9]. In response to military needs during World War II, Luis Alvarez designed the first electronically steered array operating in X-band, used in an airborne mapping radar system called *Eagle*, at the MIT Radiation Lab. The potential of electronic beam-forming for military applications has led to the development of the first phased arrays for civil radar applications. In the last decades, the relatively lower costs and the higher level of circuit miniaturization achieved by MMIC technologies have led to their use in satellite links such as the Globalstar network for satellite-based data and voice services [9]. Phased arrays have also been widely used in radio astronomy, where the signals from several small antennas are combined to emulate an antenna with a large aperture. An example is a system called Very Large Array (VLA), currently operational in New Mexico. Recently, the use of mm-wave bands (e.g. K/Ka bands, V band, E band etc.) and the new

requirements in terms of circuit integration level, power, feasibility and costs have driven the development of newer and more advanced phased array systems used for different applications:

- Medical (e.g. tumor detection radar system [9])
- Automotive (e.g. collision-avoidance radar system [9])
- Defense
- Imaging
- Wideband, high data-rate satellite and mobile communications (e.g. 5G NR links, 5G SatCom).

Phased arrays can be classified into two families: PESA (Passive Electronically Scanned Array) and AESA (Active Electronically Scanned Array). PESA arrays use a single transmitter/receiver (indicated by TX power amplifier and RX low noise amplifier) connected to the input of the beam-former network for all the antenna elements. In this configuration, each radiating element has a phase shifter which is used to change the signal phase as required by the antenna to regulate the beam direction, as shown in **Figure 2-2 - a**. Passive Electronically Steered Antenna Arrays can be thought of as the first generation of Phased Array Antennas and have been used in various military radar applications [10] (e.g. Mammut PESA radar developed by GEMA company in 1944, Zaslon PESA radar for MiG-31 aircraft developed by NIIP in 1975, etc.) and commercial services (GEO radar systems, low-cost sensor networks, etc.). The Active Electronically Steered Array (AESA) represents the second generation of phased array antennas developed since the 1970s/1980s. In the AESA topology, each radiating unit is connected to a small transmit/receive module (TRM), which are currently realized in the more advanced MMIC

processes such as CMOS/BiCMOS or GaAs/GaN, and phase shifters are put inside the transceivers (**Figure 2-2 -b**). All the functions such as beam-steering, gain control, channel selection, etc. can be managed by software. Unlike PESAs, AESA arrays can transmit/receive multiple radiation beams at multiple frequencies simultaneously [10]. This aspect allows the implementation of MIMO algorithms on phased array structures to enhance the network capacity, the data-rate per user, and the performance in terms of inter-user or inter-cell interference and signal-to-noise (S/R) ratio.



a) b)

Figure 2-2: Phased array classification. a) PESA; b) AESA.

2.2 Phased array architectures

As mentioned previously, beam-forming is the key feature of modern phased array systems. Depending on the application, this technique can be conventionally implemented either in analog or digital domains [11][12]. By exploiting the advantages of both analog and digital configuration, another technique, which is called “hybrid”, has been developed and it results more attractive mostly in the latest wireless communication systems that use MIMO technologies (e.g. 5G small cell) [11]. In the following sections, these three beam-forming architectures will be treated and their features will be reported.

2.2.1 Analog beam-forming architecture

Phase shifting in the analog domain has been the dominant architecture of phased arrays ever since they were developed [12]. As shown in **Figure 2-3** three beam-forming techniques, which are implemented considering the use of phase shifters (PS) in three different points in the analog domain, have been found in the literature [12].

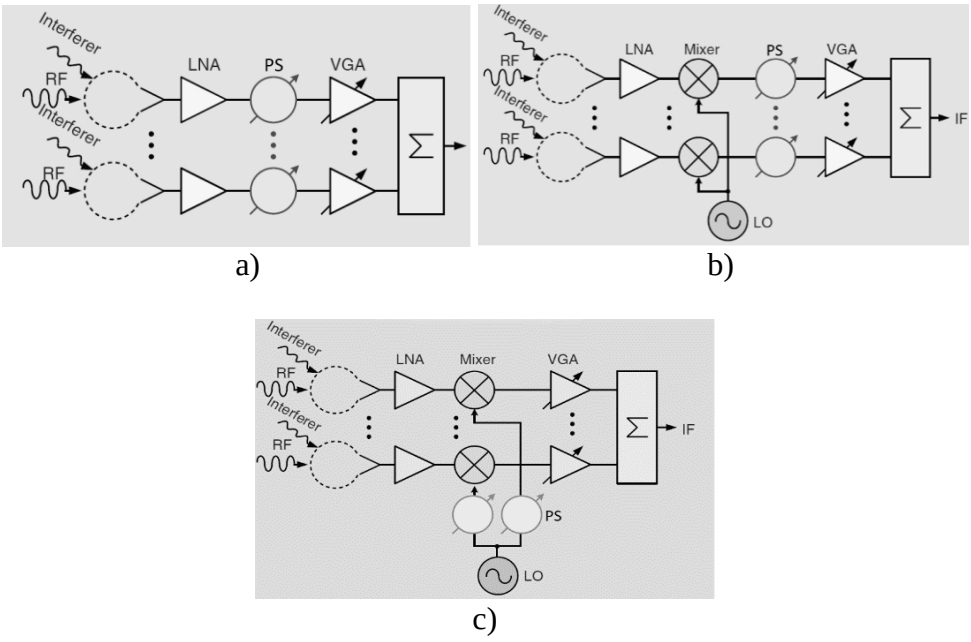


Figure 2-3: Analog beam-forming architectures [12]. a) RF domain; b) IF domain; c) LO domain.

For each reported architecture, the role of various building blocks does not change. In particular, a phase shifter (PS) is used to control the phase of the received/transmitted signal from/to a single antenna or group of antennas in the array (depending on the array configuration), thus modifying the pointing direction of the radiated beam (*beam steering* operation). Variable gain amplifiers (VGAs) or Attenuators is used for a dual purpose: reduction of the side-lobe levels (SSL) on beam pattern (by applying a specific amplitude tapering function such as Taylor, Chebyshev, etc.), and gain control of the main lobe

(adjustment of EIRP value) [12][13]. VGAs are typically put after the LNA in the RX chain and before the PA in the TX chain.

The main advantages of the RF-domain beam-forming (**Figure 2-3 -a**) are its simplicity, system-level linearity, low power consumption in the phase shifters and power combining/splitting networks, and the possibility to integrate with a single MMIC circuit all the building blocks of T/R module. Another advantage is that the signal after the RF combiner (in RX mode) has a high pattern directivity and can substantially reject an interferer before the receiver, thus improving the circuit's linearity and signal-to-noise performance. Phased arrays based on the IF and local oscillator (LO) phase-shifting architectures have also been proposed [12]. The advantage of these architectures is that the phase shift is done in the IF path or in the LO path (there are not phase shifters in the RF signal path), as shown in **Figure 2-3 -b** and **Figure 2-3 -c**, and both systems result in a straightforward IF power combining network. These configurations could be convenient for narrow-band phased array systems. However, a mixer is required at each radiating element, which is subjected to interference because of the wide antenna element patterns, thus leading to an increment of both phase noise and inter-modulation distortion [12]. These architectures also require the use of an LO distribution network, which can be an issue in terms of complexity and occupied area of the array. To keep the phase noise of these systems lower, the only solution is to replace the on-chip LO with an external oscillator, such as a dielectric resonator [12]. However, this arrangement removes the advantage of integrated on-chip oscillators and increases both circuit complexity and the occupied area.

An example of a 64-elements organic-based multi-layered Antenna-in-Package (AiP) phased-array with RF-domain beam-forming architecture is reported in **Figure 2-4**. As mentioned in [13], each 32-channels MMIC TRX transceiver, which is realized in a 0.13um

SiGe BiCMOS process, manages a 4x4 sub-array and the phase/amplitude control is applied, by distributed-line PSs and phase-invariant VGAs, on each dual-polarized stacked patch antenna. Moreover, each TRX FE shares the same building blocks between TX and RX in time division duplex (TDD) mode by using a $\lambda/4$ T-line T/R switch. By this array configuration, it is possible to control 8 simultaneous beams in a beam-scanning range of $\pm 50°$ in azimuth and $\pm 30°$ in elevation with a beam resolution of 1.4°. The four IC transceivers are flip-chip attached to the bottom side of the package and the latter are mounted to an external PCB via BGA balls. The proposed beam-forming circuit occupies a small area and achieves very high phase resolution (equal to 5°) with lower values of RMS phase error. The overall DC power consumption of the IC transceivers is reduced below 2.5W (DC power dissipation for channel < 0.15 W).

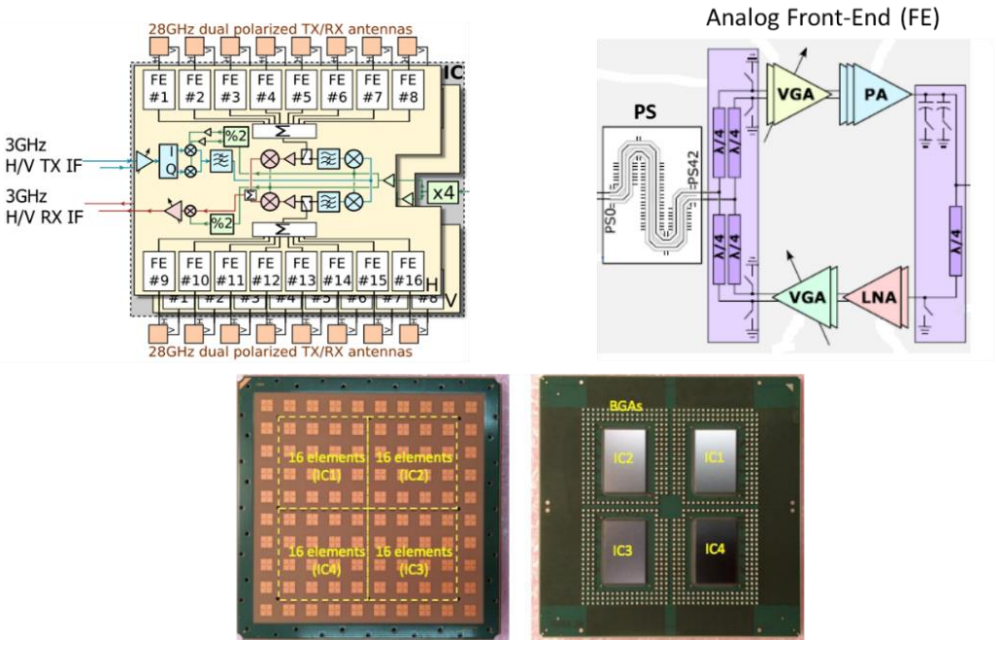


Figure 2-4: AiP phased array with analog RF domain beam-forming [13].

2.2.2 Digital beam-forming architecture

In phased arrays based on digital beam-forming (DBF) techniques, each antenna is connected to an in-phase/quadrature (I/Q) transceiver, and the received (or transmitted) I/Q signals are digitized by ADC blocks and sent to a baseband DSP network (**Figure 2-5**) [12]. The DSP applies the required amplitude and phase weighting to each antenna element to result in a number of simultaneous patterns (typically two to four), each with its own scan angle, side-lobe level, and bandwidth. Compared with the other architectures, DBF architectures are used in the most versatile phased arrays because of the highest precoding freedom, flexible multi-beam ability, fast beam-steering speed, and high beam-forming precision. On the other hand, these suffer from high power consumption, significant size and weight [14].

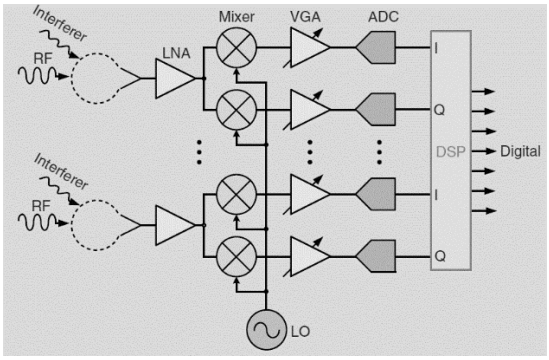


Figure 2-5: Digital beam-forming architecture [12].

As the case at hand, a millimeter-wave massive MIMO with digital beam-forming (DBF) architecture (**Figure 2-6**) operating at 28 GHz has been proposed in [14]. The proposed transceiver has a (16x4) 64-element antenna array configuration. A printed Yagi-Uda antenna element combined with a microstrip balun structure was chosen as the radiating element in the transceiver because of its compact size, ease of fabrication, high gain and

low-cost factors. The experimental reflection coefficient of the designed array is lower than -14 dB at 28 GHz with a bandwidth of more than 3 GHz. The wide azimuthal angular beam-scanning achieved by the proposed DBF-based phased-array system is $\pm 67°$, while the measured scan range along elevation is $\pm 28.5°$. The overall DC power consumption, including all mm-wave transceiver front-ends, IF system and baseband DSP/DBF circuit, is higher than 1 kW.

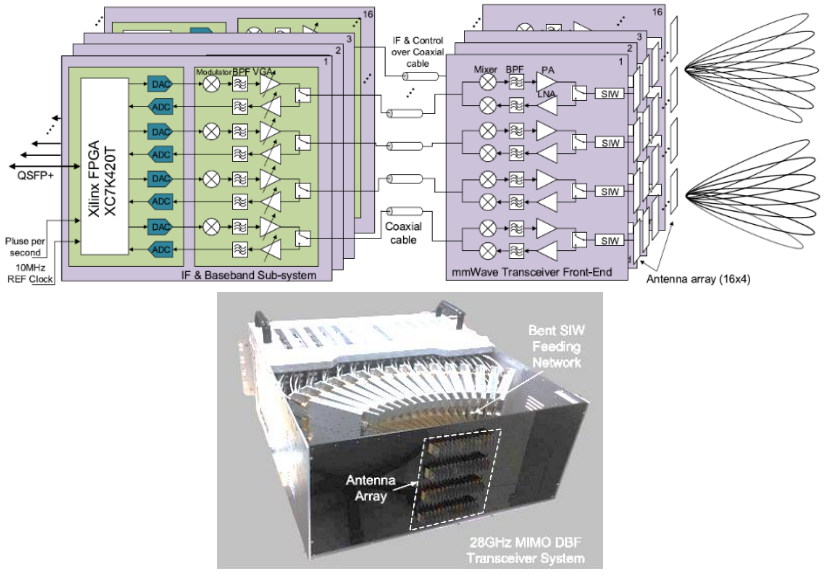


Figure 2-6: DBF-based 64-elements phased array [14].

2.2.3 Hybrid beam-forming architecture

Large-scale antenna systems (LSAS), where a large number of mm-wave front-end transceivers have been employed, are attractive for the development of more advanced massive MIMO systems, because of better performance in terms of beam-forming (BF) gain, network capacity, etc. However, the implementation of the conventional beam-forming techniques on LSAS systems will be difficult due to high cost, energy consumption, and excessive demand for real-time data processing with high beam-forming

gains [6][11]. Using the analog beam-forming approach, the number of transceivers can be reduced if each mm-wave transceiver is connected to a group of active array elements and the signal phase of each antenna can be managed by a network of phase shifters. Designs with transceivers number smaller than elements number can be developed. Still, the architecture might introduce severe inter-user interference for inadequate spatial separation between users (or channels), thus leading to a reduction of signal-to-noise (S/N) value [6]. To further enhance the performance, digital beam-forming can be utilized over transceivers to achieve multiple data beam precoding on top of analog beam-forming, but this one leads to have an increment of occupied area, power dissipation and costs. By exploiting the advantages of analog BF and digital BF, a *hybrid beam-forming* architecture can be implemented and used in the latest mm-wave massive MIMO systems. An example of hybrid architecture [12], where each of the N transceivers is connected to M antennas, is reported in **Figure 2-7**. In this configuration, analog BF is performed over only M RF paths in each transceiver, and digital BF is performed over N transceivers. Therefore, fewer DACs will be used and this will lead to a reduction in the inter-channel interference levels, power consumption and area occupied.

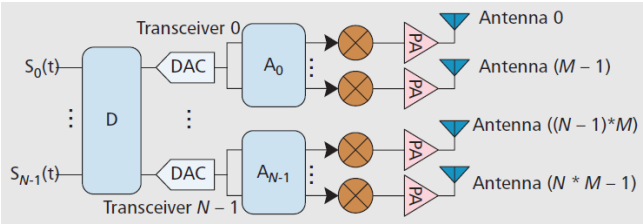


Figure 2-7: Example of hybrid-BF based phased array architecture [12].

An interesting hybrid-BF based phased array operating at 28 GHz has been analyzed in [15]. The array of 32 elements is organized in four active sub-arrays of eight elements, as depicted in **Figure 2-8**. Each unit is controlled by an RF transceiver where is implemented

an analog beam-forming precoding technique through the use of a phase-shifting network. At this point, a baseband sub-system, that contains the DBF precoding circuit, is used to further control the beam scan angle and the amplitude of the digitized streams. In this configuration, four simultaneous beams can be managed and the direction of these patterns can be varied in a beam-scanning range of $\pm$ 45° along the azimuth plane. The measured phase resolution of the IF phase shifting unit, which is based on the use of vector modulators, is lower than 1.5° with a very low RMS phase error of 0.62°, while the achieved beam-steering resolution is less than 1°. The DC power of the entire system is significantly lower than the one obtained in the digital architecture reported in [14].

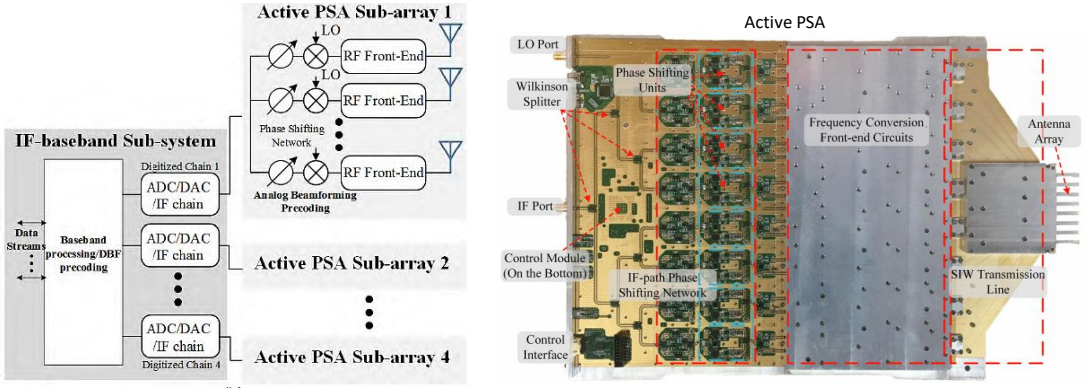


Figure 2-8: 32-elements hybrid BF-based phased array [15].

2.3 Fundamental concepts of phased arrays

2.3.1 Array factor

Assume that N isotropic sources, which are spaced d apart, are arranged along the x-axis, as shown in **Figure 2-9**, and that the coupling effect between elements is ignored [16].

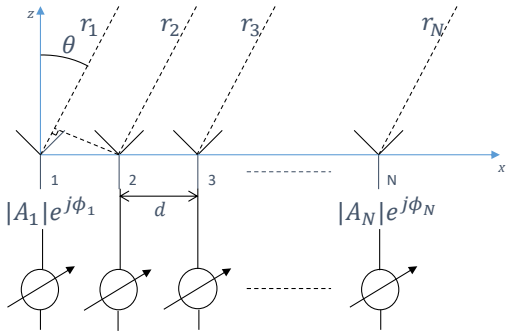


Figure 2-9: A linear array of N radiating elements.

If we consider that both the amplitude and phase of N excitation signals are uniform (A_1= ……. = A_N= A), the radiated field of the array is essentially the sum of N identical far-field single element radiation patterns. Therefore, by using the far-field radiation formula of the single isotropic element:

$$\psi_n(r,\theta) = A_n \frac{e^{-jkr}}{r} \qquad \textbf{Eq. 2-1}$$

The total radiation of the array can be performed by the following formula:

$$\Psi(r,\theta) = \sum_n \psi_n(r,\theta) = \sum_n A_n \frac{e^{-jkr_n}}{r_n} \qquad \textbf{Eq. 2-2}$$

$\Psi(r,\theta)$ can be also calculated by indicating the superposition of the individual fields [16] as follows:

$$\Psi(r,\theta) = A\sum_n^N \frac{e^{-jk(r-ndsin\theta)}}{r} = A\frac{e^{-jkr}}{r}\sum_n^N e^{jkndsin\theta} = A\frac{e^{-jkr}}{r}AF(\theta) \qquad \textbf{Eq. 2-3}$$

Where:

$$k = \frac{2\pi}{\lambda}$$

It can be seen from Eq. 2-3 that the total field of the array is equal to the field pattern of a single element at a selected reference point (usually the origin), multiplied by a factor which

is widely referred to as the array factor $AF(\theta)$. The array factor is a function of the number of elements N, their geometrical arrangement (lattice shape, inter-element spacing d), their relative amplitudes and phases [16]. At this point, if the excitation phase for the n-th radiating element of the array is set, by a specific phase shifting circuit, based on the following expression:

$$\phi_n = -kndsin\theta_0 \qquad \textbf{Eq. 2-4}$$

the array will focus the main radiation lobe along θ_0 direction. Therefore, the array factor in scanning mode $AF(\theta)$ will become:

$$AF(\theta) = \sum_n^N \overline{A_n}\, e^{jkndsin\theta} = \sum_n^N e^{jknd(sin\theta - sin\theta_0)} \qquad \textbf{Eq. 2-5}$$

$$if\ A_1 = \ldots\ldots = A_N = 1$$

Eq. 2-5 confirms that the radiation pattern has a maximum at $\theta_0 = 0°$ where $AF(\theta_0) = N$. **Figure 2-10** shows the array factor of a linear array in scanning mode. As it can be noted, the beam-steering results in a translation of the entire array factor along theta direction.

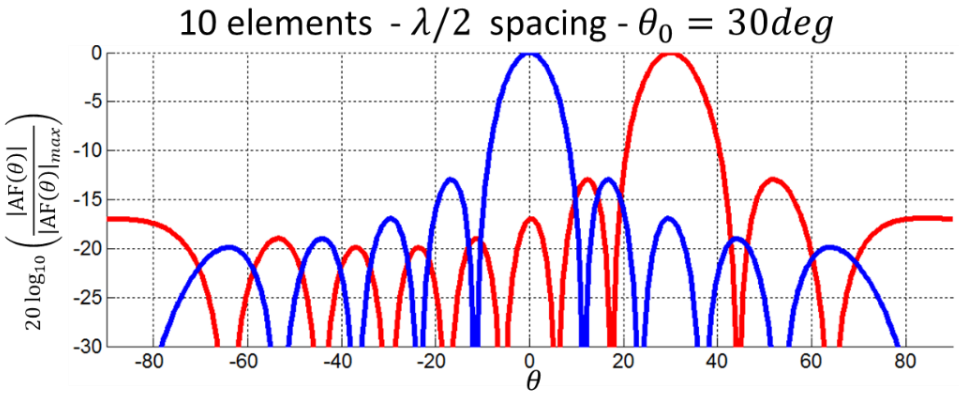


Figure 2-10: Beam steering of the array factor.

2.3.2 Grating lobes analysis

Phased arrays change the progressive phase by the term $e^{jknd(sin\theta - sin\theta_0)}$ to shift the main beam in the $[-\frac{\pi}{2}, \frac{\pi}{2}]$ visible space [16] [17] (as depicted in **Figure 2-10**). Since the array factor is a periodic function of $\frac{\pi d}{\lambda}(sin\theta - sin\theta_0)$ then:

$$|AF(\theta)| \text{ has a maximum for } \pi\frac{d}{\lambda}(sin\theta - sin\theta_0) = \pm m\pi \text{ with } m = 0,1,2,\ldots \quad \textbf{Eq. 2-6}$$

From expression (2.6) it is clear that the first maximum of $|AF(\theta)|$ at $\theta = \theta_0$ (which corresponds to the main lobe) occurs when $m = 0$. Therefore, the second maximum appears in the visible space when:

$$m = 1 \rightarrow \pi\frac{d}{\lambda}(sin\theta - sin\theta_0) = \pm 1 \quad \textbf{Eq. 2-7}$$

This second lobe that has the same amplitude as the main lobe is called *grating lobes*. As an example, in **Figure 2-11** is reported the case where a grating lobe occurs in the visible space when the main beam of a linear phased array is directed at $\theta_0 = 30°$.

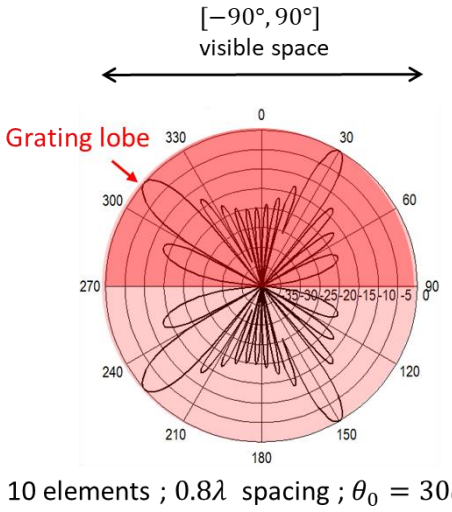


Figure 2-11: Grating lobe in the visible space of a linear phased array.

This unwanted lobe marks a limit on the scan performance of phased arrays since it should not appear in the visible space during the beam steering operation. As indicated in Eq. 2-7, the presence of grating lobes in $[-\frac{\pi}{2},\frac{\pi}{2}]$ depends on the scan angle θ_0, the inter-element spacing d and the wavelength (calculated at a single frequency) [17][18]. In particular, if the following condition is verified:

$$\frac{d}{\lambda} < \frac{1}{max(|sin\theta - sin\theta_0|)} => \frac{d}{\lambda} < \frac{1}{|1 + sin\theta_0|} \; with \; \theta \in [-\frac{\pi}{2},\frac{\pi}{2}] \qquad \textbf{Eq. 2-8}$$

the grating lobe doesn't occur in the visible space. As it can be noted in **Figure 2-12**, from the scan angle value it is possible to choose correctly the inter-element spacing to avoid grating lobes in the visible space at a certain frequency. In particular, if the spacing value is lower than half wavelength, for any θ_0 value from 0 to $\frac{\pi}{2}$, grating lobes don't theoretically occur in the visible space.

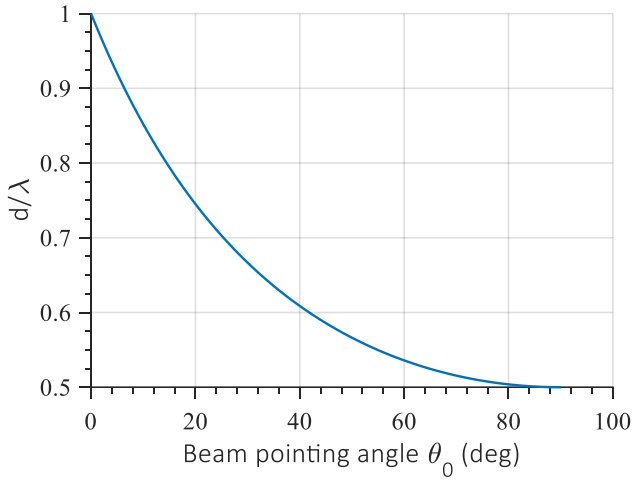


Figure 2-12: Relationship between spacing and scan angle.

2.3.3 Beamwidth

Beamwidth provides a figure of merit regarding the angular resolution of the antennas [19]. Beamwidth is usually defined by the half-power beamwidth (HPBW)

parameter. HPBW represents the angular interval in which the amplitude of the radiation pattern decreases by 50% (or -3 dB) from the peak of the main lobe. For uniform linear array, an approximation for HPBW [19] is given as:

$$0.886\frac{\lambda}{Ndcos\theta_0} \qquad \textbf{Eq. 2-9}$$

HPBW versus beam direction for several elements number, when the element spacing is λ/2, is reported in **Figure 2-13**. From this graph, it is worth noting that for any scan angle value, the HPBW value decreases when the size of the array increases and vice versa. Moreover, by fixing the element number of the array, as the scan angle increases the HPBW increases as well.

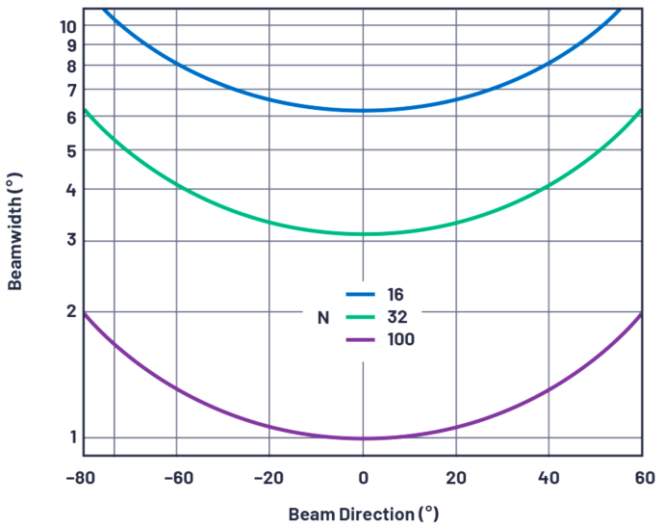


Figure 2-13: Relationship between HPBW and beam direction [19].

2.3.4 Scan losses

As it is shown previously, if the scan angle is increased, the half-power beamwidth increase as well. This increment leads to a gain reduction of the steered main lobe. Since the array factor $AF(\theta)$ is an explicit function of $(\sin\theta - \sin\theta_0)$ and the HPBW varies as

$1/\cos\theta_0$, the scan loss will depend on the single element pattern [16]. Therefore, it is possible to estimate the scan loss value (in dB scale) of the array from the single element pattern (which can be expressed in the form $\cos^n(\theta)$) by the following formula:

$$10\log_{10}(\cos^n\theta_0) \qquad \textbf{Eq. 2-10}$$

From Eq. 2-10, it can be noted that if the directivity of the single element is higher (e.g. the cosine exponential n is greater), the scan loss evaluated at θ_0 grows as well, as depicted in **Figure 2-14**.

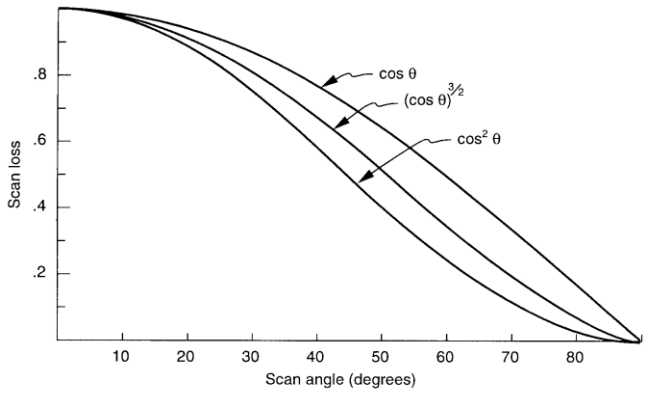


Figure 2-14: Scan loss (linear scale) versus scan angle.

In **Figure 2-15** is reported an example of how the element pattern affects the radiation performance of a linear array that operates in scanning mode [19]. Considering the $\cos\theta$ pattern of the single element, at θ_0 = 45° the amplitude of steered main lobe is 1.5dB lower than the one of the main lobe at boresight direction. This amplitude gap is the scan loss calculated by Eq. 2-10.

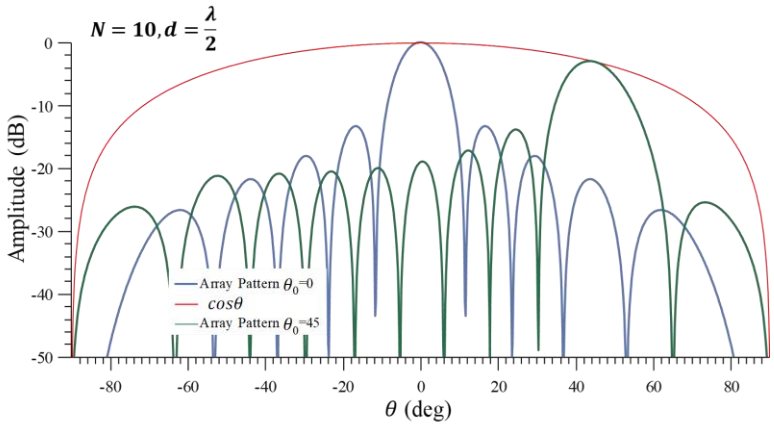


Figure 2-15: Amplitude variation evaluated when the array is scanning the main lobe.

2.3.5 Array directivity and gain

The directivity can be simply calculated as a function of either the occupied area A_{array} (which can be indicated in wavelengths) or the number of elements N of the array by the following expressions:

$$D = 10\,log(\frac{4\pi}{\lambda^2}A_{array}) \quad or \quad D = 10\,log(N) \qquad \textbf{Eq. 2-11}$$

These formulas are valid if an isotropic element pattern that has a directivity equal to 0dBi is considered in the array analysis. If a more directive element pattern is used, in the formulation above the element directivity should be added:

$$D = 10\,log(\frac{4\pi}{\lambda^2}A_{array}) + D_{elem}(dB) \quad or$$
$$D = 10\,log(N) + D_{elem}(dB) \qquad \textbf{Eq. 2-12}$$

At this point, the array gain can be obtained as the product between directivity and efficiency:

$$G = \eta(\frac{4\pi}{\lambda^2}A_{array}\,D_{elem}) \quad or \quad G = \eta(ND_{elem}) \quad \text{(linear scale)} \qquad \textbf{Eq. 2-13}$$

In **Figure 2-16** is reported the directivity versus element spacing of 217-element uniform-amplitude hexagonal array for various element beamwidths [17]. This plot confirms that,

for a fixed inter-element spacing, as the element beamwidth increases, the array directivity and gain improve, too.

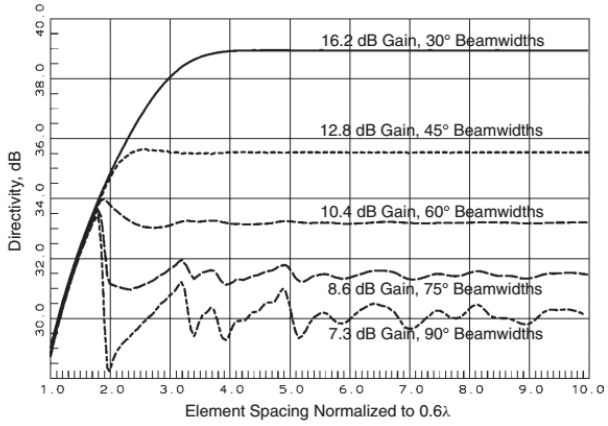


Figure 2-16: Directivity versus normalized spacing for various element beamwidths [17].

In light of the above, the choice of the single element pattern affects the performance of the array under different aspects. In particular, lower directivity elements are ideal to limit the scan losses, but this behavior does not help to suppress grating lobes that could appear in the visible space [16][17]. The position of grating lobes is controlled by directly changing the inter-element spacing. Otherwise, if higher directivity elements are used, both array gain at boresight direction and the suppression of grating lobe levels can be improved, but the increment of the scan losses could be an issue [17].

2.3.6 Active impedance

In a real array, the radiating elements interact with each other because they receive a portion of the power radiated from nearby ones. This behavior alters the currents and thus impedances seen by each element compared to the case where the elements were isolated. This interaction, called *mutual coupling*, changes the current magnitude, phase, and field distribution of each element [18]. By changing the feeding coefficients of the array

elements, the radiated beam can be steered in the visible space. This mechanism changes the element input impedance [16][18], which is called *scan impedance* or *active impedance*. Mutual coupling can be modeled by a circuit formulation based on the impedance or scattering matrix. If we consider the impedance matrix formulation, an array of N elements (**Figure 2-17**) can be treated as an N-port network where:

$$[V] = [Z][I] \qquad \textbf{Eq. 2-14}$$

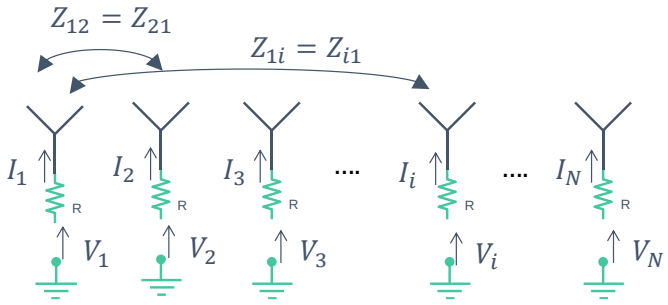


Figure 2-17: An array of N elements with impressed current/voltage excitations.

From Eq. 2-14 the impressed voltage on the i-th element can be expressed as:

$$V_i = \sum_{n=1}^{N} Z_{in} I_n e^{-j(n-1)kd\sin\theta_0} \qquad \textbf{Eq. 2-15}$$

Expanding Eq. 2-14, it is possible to obtain the active impedance of the i-th element as follows:

$$Z_i^{active} = \sum_{n=1}^{N} Z_{in} \frac{I_n}{I_i} e^{-j(n-1)kd\sin\theta_0} \qquad \textbf{Eq. 2-16}$$

where I_i and I_n are the impressed currents on both i-th and n-th elements and Z_{in} represents the mutual impedance between the i-th and n-th elements of the array. It is worth noting that the active impedance value is affected by the scan angle θ_0, which changes both the impressed currents values and mutual impedance Z_{in} [16]. Specifically, the mutual impedance (or mutual coupling) variations are due to three mechanisms:

1. Spatial coupling between array elements
2. Surface waves (in printed circuits only)
3. Coupling induced by array beam-forming networks

The spatial coupling is unavoidable because it is related to the spacing between elements. Therefore, if the spacing is increased, the effect of the spatial coupling on the active impedance decreases [18]. To reduce the impact of the surface waves on mutual coupling, there are different solutions in literature as using a metallic cavity (or vias cage) to surround each element of a printed array or employing an Electromagnetic Band Gap structure (EBG). Typically, the third mechanism related to the feeding networks causes minor effects on the mutual coupling. In the real phased array applications, the changes of the active impedance due to higher scan angle values ($\theta_0 > 40°$) cause impedance mismatching, which could significantly reduce the performance in terms of bandwidth. In literature, exist different techniques used to limit this effect, such as improving the matching level of the radiating cell (internal technique) or using a WAIM dielectric layer on the top of the array (external technique).

2.3.7 Active element pattern and scan blindness

Mutual coupling not only affects active impedance, but also radiation properties such as far-field pattern and polarization. Therefore, the array pattern must include the variations in the excitation currents as well as the patterns of each element acting under the influence of all coupling effects [18]. Formally, the element pattern affected by mutual coupling is called *active* or *embedded element pattern (AEP).* AEP is defined as the radiation pattern when only one element of the array is fed while all the others are terminated on a matched load (as shown in **Figure 2-18**). AEP differs from the *isolated*

element pattern, because in the latter is not considered the coupling effects of the array and, therefore, this can be seen as the ideal benchmark.

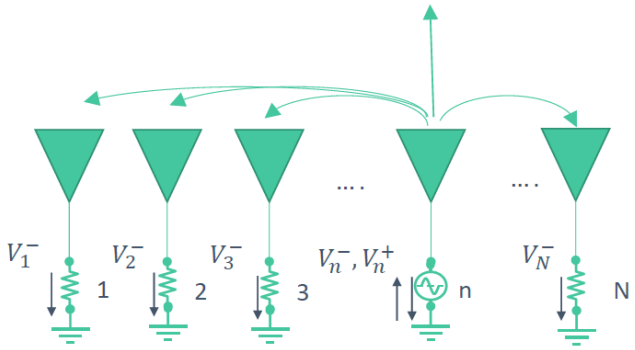


Figure 2-18: AEP definition on an array of N elements.

The "shape" of the active element pattern also depends on the element's position which is fed in the array. Typically, the edge element pattern is more distorted than the center element of the array (Figure 2-19) because of the diffraction effects introduced by edges of the structure [18].

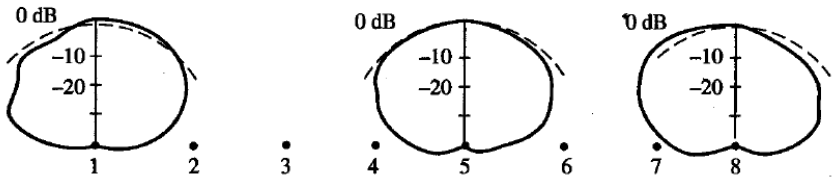


Figure 2-19: Comparison between AEP (solid line) and isolated pattern (dashed line) for three different element positions in an 8-elements linear array [18].

Figure 2-19 reveals that worst-case mutual coupling is acceptable if the discrepancy between the AEP of the center element and the isolated pattern is minimal. By taking both active gain pattern of the center element ($G_{AEP}(\theta, \phi)$) and the array factor, it is possible to perform the array gain pattern as:

$$G_{array}(\theta, \phi) = G_{AEP}(\theta, \phi) AF(\theta, \phi) \qquad \textbf{Eq. 2-17}$$

where:

$$G_{AEP}(\theta,\phi) = G_{isol}(\theta,\phi)(1-|\Gamma_{active}(\theta,\phi)|^2) \qquad \textbf{Eq. 2-18}$$

Eq. 2-17 and Eq. 2-18 confirm that the gain of AEP and, consequently, the array gain pattern is affected by the active input reflection coefficient Γ_{active}, whose value changes as the scan angle θ_0 varies. When a phased array is scanned, at certain values of θ_0 the input reflection coefficient of every element rapidly increases to 1 [17]. The array fails to radiate and forms a null on the radiation pattern. This effect, which is called *scan blindness*, is difficult to predict accurately except where the array structure supports surface waves (e.g. printed arrays, dielectric-covered waveguide arrays). The Floquet theory affirms that scan blindness occurs when a grating lobe enters in the visible space and radiates along the surface of the array [17]. In this case, the array can exhibit scan blindness when the electrical distance d/λ between the elements equals the surface-wave propagation phase shift:

$$\left|cos\theta_{gr}\right| = \frac{\lambda}{d} - \frac{k_{sw}}{k} = \frac{\lambda}{d} - P \qquad \textbf{Eq. 2-19}$$

where P is the relative propagation constant with a value > 1 for a surface wave. Scan blindness will occur approximately at an angle near this value [17]. This angle can be shifted to higher values and the null dip can be reduced, if the array element spacing d array is smaller (or the unit cell size is smaller) and the beamwidth of the active element pattern (AEP) is narrower. Another solution used to shift the scan blindness angle out of visible space is to fill the waveguide with dielectric materials that have a commercial $\varepsilon_r \geq 3$ (this arrangement is applied mostly to the waveguide arrays).

3 Analytical approach for phased arrays design

3.1 Simulation procedure in Ansys HFSS

In chapter 2 have been defined the basic elements used to design properly phased arrays. By studying these parameters is also possible to understand how some related phenomena can affect the performance of these radiating structures. For instance, the impact that the mutual coupling has on the impedance bandwidth when an array is scanning can be analyzed by the active impedance values evaluated at the input of each array element. From an analytical perspective, a simulation flow must be defined to manage efficiently the design of a phased array. Recently, a three-step workflow (**Figure 3-1**) for 5G phased arrays has been proposed by Ansys technical staff [20]. By using three different analysis methods, it is possible to evaluate several aspects related to the phased array operation such as the presence of grating lobes, the effects of mutual coupling, scan blindness and scan loss variations when the array operates in scanning mode. These simulation steps will be examined separately in the following sections.

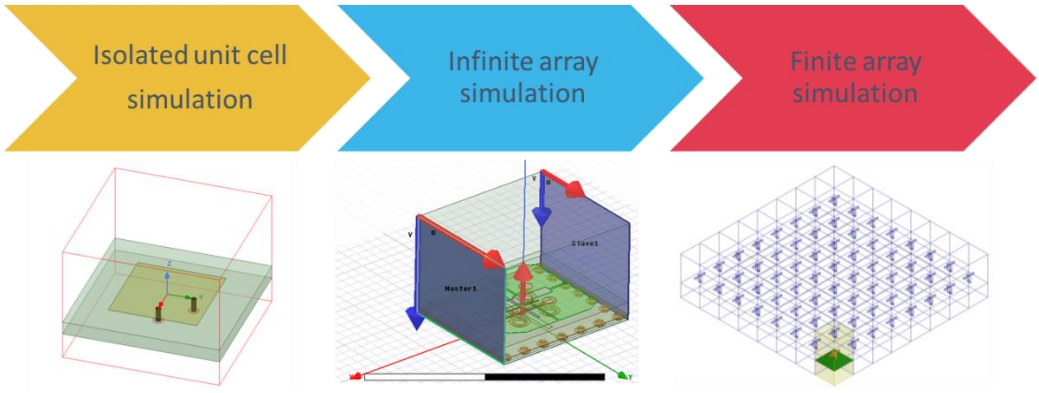


Figure 3-1: Three-step design flow in Ansys HFSS.

3.2 Isolated unit cell analysis

The unit cell is defined as the smallest periodic portion of the array. In this first step, the correct sizing of the unit cell is essential to avoid that the presence of grating lobes within the visible space of the array can lead to a power spreading to unwanted directions and an increment of spatial aliasing. As indicated in chapter 2, when a radiant cell is used within a phased array, this condition of free grating lobes should be guaranteed in the band of interest considering the maximum scan angle value θ_{0max} along azimuth and/or elevation direction. For instance, if a unit cell is arranged in a rectangular lattice configuration, the well-known conditions to be satisfied are reported in Eq. 3-1.

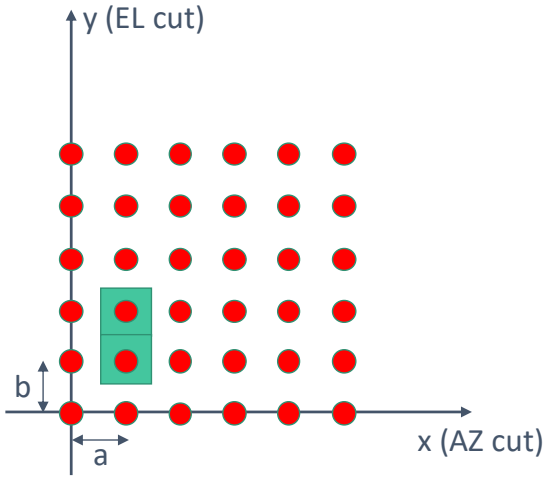


Figure 3-2: Arrangement of the cells in a rectangular lattice.

$$a < \frac{\lambda_{min}}{|1 + sin\theta_{0AZmax}|}; \qquad b < \frac{\lambda_{min}}{|1 + sin\theta_{0ELmax}|} \qquad \textbf{Eq. 3-1}$$

These formulas give an upper bound to the inter-element distance before grating lobes appear in the $(u - u_0, v - v_0)$ space. By applying the 2-D Floquet series expansion at the unit cell used in **Figure 3-2**, it is possible to calculate by Eq. 3-2 the frequency where grating lobes could manifest in the visible space as a function of the inter-element spacing.

$$f_{GL\_AZ} = \frac{c_0}{a|1 + sin\theta_{0AZ}|}; \qquad f_{GL\_EL} = \frac{c_0}{b|1 + sin\theta_{0EL}|} \qquad \textbf{Eq. 3-2}$$

According to the Floquet theory [16][18], a gain blind spot in the steered radiation pattern of the array could appear at frequency values close to the grating lobe ones f_{GL_AZ} and f_{GL_EL}. As mentioned in chapter 2, when a grating lobe appears at a certain frequency in the $(u - u_0, v - v_0)$ space at θ_{GL_AZ} and θ_{GL_EL}, a gain blind spot could manifest very close to these angular directions. Therefore, if the surface waves effect is negligible, the angles where grating lobes may appear can be calculated by Eq. 3-3.

$$\theta_{GL\_AZ} = sin^{-1}\left(\frac{\lambda}{a} - 1\right); \qquad \theta_{GL\_EL} = sin^{-1}\left(\frac{\lambda}{b} - 1\right) \qquad \textbf{Eq. 3-3}$$

In light of this, the correct sizing of the cell should also guarantee the nonexistence of scan blindness spots in the required scan range $[-\theta_{0max}, \theta_{0max}]$ along azimuth and elevation planes for all the frequencies in the band of interest.

In the HFSS simulation environment, a single isolated radiating cell should be designed and some fast full-wave simulations should be performed to evaluate roughly if the element performance (e.g. return loss, radiation gain, HPBW, etc.) meet the design requirements. To solve the radiation problem, only radiation boundaries are applied to the air box of the isolated cell. The mutual coupling effects (e.g. scan blindness, impedance mismatch when scanning) are ignored in this phase.

3.2.1 Isolated unit cell sizing and preliminary simulations.

As an example, it is reported the design of an isolated radiating cell used for a 32-element rectangular phased array operating in 5G n257 band (26.5 ÷ 29.5 GHz). As indicated previously, the radiating cell should be tailored to avoid grating lobes in the visible space when the array directs the beam in the range ($\pm 55° \, AZ, \; \pm 20° \, EL$).

Considering the single polarized radiating element depicted in **Figure 3-3**, by selecting a value of $a_{cell} = 5.2mm$ and $b_{cell} = 6.8mm$, the grating lobes should not appear in the $(u - u_0,\ v - v_0)$ space of the rectangular lattice, because these values satisfy the two conditions shown by Eq. 3-4.

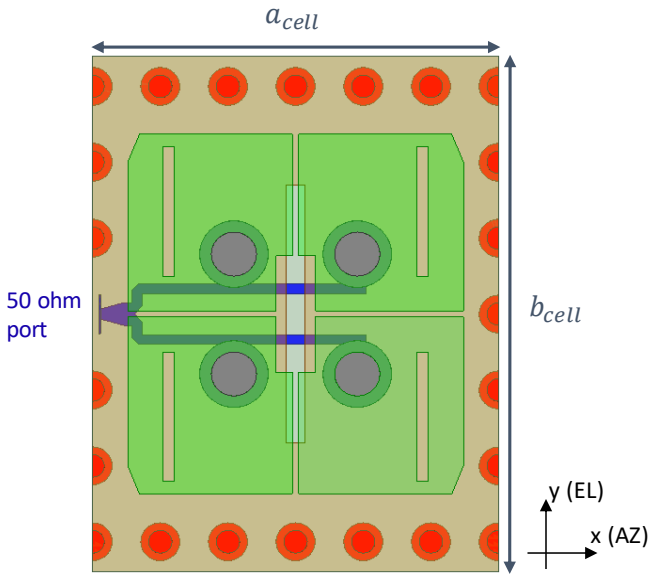


Figure 3-3: Top view of the radiating unit cell (Magneto-Electric dipole antenna).

$$a_{cell} < \frac{\lambda}{1+sin(\vartheta_{0\ maxAZ})} = 0.55\lambda\ (5.6mm\ at\ f_{max} = 29.5GHz)$$

$$b_{cell} < \frac{\lambda}{1+sin(\vartheta_{0\ maxEL})} = 0.74\lambda\ (7.5mm\ at\ f_{max} = 29.5GHz)$$

Eq. 3-4

These spacing values a_{cell} and b_{cell} ensure that the gain blind spots along two planes might be visible for frequency values near f_{GL_AZ} and f_{GL_EL}, which are outside the n257 band (Eq. 3-5). Moreover, by this sizing of the cell, the approximate values of the angles where the gain blind spots could appear are outside the required scan range (Eq. 3-6).

$$f_{GL_{AZ}} = \frac{c_0}{a_{cell}|1 + sin\theta_{0maxAZ}|} = 31.7GHz$$

$$f_{GL_{EL}} = \frac{c_0}{b_{cell}|1 + sin\theta_{0maxEL}|} = 32.8\,GHz$$

Eq. 3-5

$$\theta_{GL_{AZ}} = sin^{-1}\left(\frac{\lambda}{a_{cell}} - 1\right) = 73° \quad \theta_{GL\_EL} = sin^{-1}\left(\frac{\lambda}{b_{cell}} - 1\right) = 30°$$

Eq. 3-6

As mentioned previously, this first step of phased array design procedure is useful to understand roughly if the results obtained by full-wave HFSS simulations of the antenna meet the project requirements. In **Figure 3-4 -a** and **Figure 3-4 -b** are reported the S-parameters and the radiation performance of the radiating element, respectively. As it can be noted, the preliminary S11 bandwidth cover the entire 5G n257 band, while the boresight gain is very flat in the same frequency range. Moreover, at f_0 = 28GHz the radiator shows good characteristics in terms of cross-polarization level, front-to-back (F/B) ratio and HPBW on both planes as shown in **Figure 3-4 -c**.

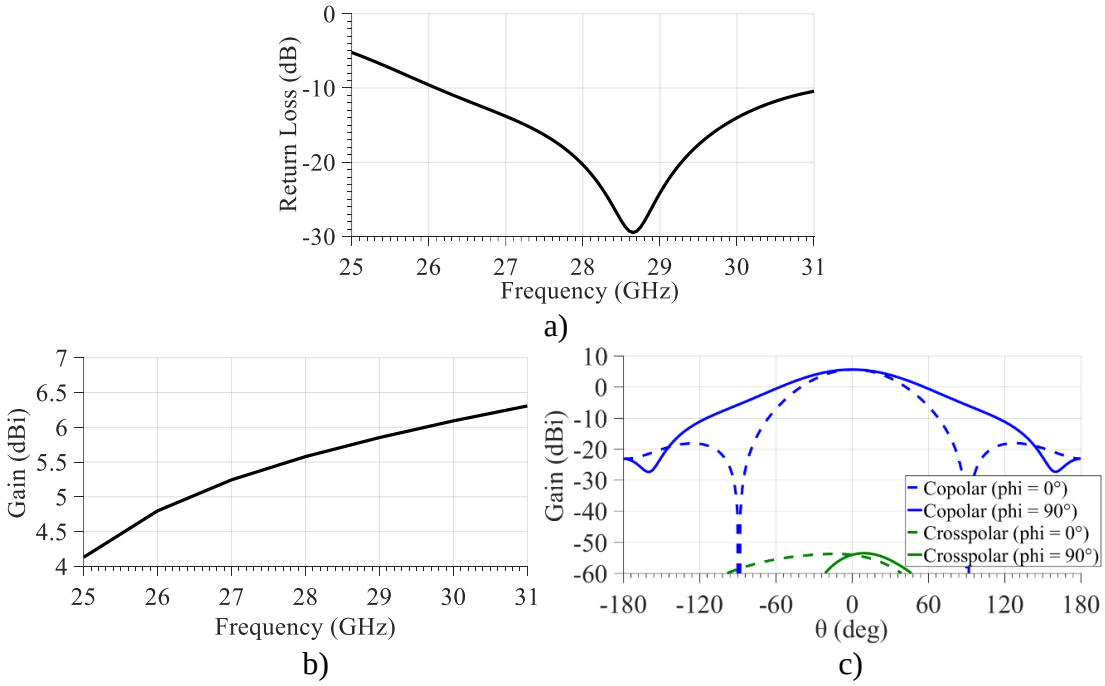


Figure 3-4: HFSS full-wave simulation of the unit cell. a) Return Loss vs frequency; b) Gain vs frequency; c) Co-polar and cross-polar gain at 28 GHz on both E and H-planes.

3.3 Infinite array analysis

The infinite array analysis applied to the unit cell plays a key role in the study of the phased antenna array for several reasons [16]:

- Radiating cells in the central region of an electrically large array ($N \geq 7 \times 7$ elements) have similar active impedance characteristics as that of an element in an infinite array.
- The Active (or Embedded) Element Pattern that includes mutual coupling effects can be determined directly from the infinite array results.
- The infinite array results are applied to predict the mutual coupling between the elements in an array environment.
- The performance of a finite array can be determined accurately utilizing infinite array results.

Mathematically, an infinite array antenna is equivalent to an array of infinite source functions. As mentioned in [16], the radiation problem of an array of infinite elements placed at regular interval can be solved by applying the Fourier transform theory. If the amplitude and phase of these sources have two different periodicities, the radiation problem of the infinite array can be treated more easily by applying a Fourier-like series called a Floquet series. The basic functions that constitute the Floquet series are called Floquet modal functions. This implies that an infinite array of sources can be represented as a superposition of Floquet modal functions.

Assume that the unit source is replicated infinitely along x and y axes on a general periodic grid structure as shown in **Figure 3-5**.

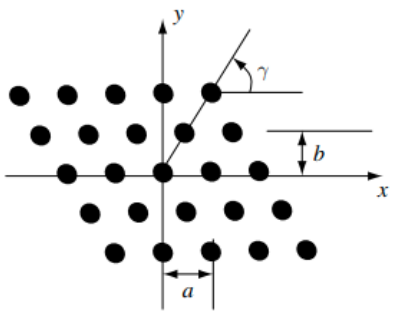


Figure 3-5: General grid structure of a planar periodic array antenna.

For a two-dimensional Floquet modal function, the surface current should have the following form:

$$\vec{I}(x,y) = \hat{y} \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} f(x - x_{mn}, y - y_{mn}) e^{-jk_{x0}x_{nm}} e^{-jk_{y0}y_{nm}} \qquad \textbf{Eq. 3-7}$$

where (x_{mn}, y_{mn}) are discrete grid points on the x,y-plane; k_{x0} and k_{y0} are two constants that determine the discrete phase shift between the adjacent cells. For a generic grid lattice, x_{mn} and y_{mn} are indicated as follows:

$$x_{mn} = ma + \frac{nb}{tan\gamma}; \quad y_{mn} = nb \qquad \textbf{Eq. 3-8}$$

Expanding the current source (Eq. 3-7) into a Floquet series, we obtain:

$$\vec{I}(x,y) = \hat{y} \frac{4\pi^2}{ab} \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} \tilde{f}(k_{xmn}, k_{ymn}) e^{-jk_{xmn}x} e^{-jk_{ymn}y} \qquad \textbf{Eq. 3-9}$$

From Eq. 3-9, it is possible to calculate the components of the radiated electric field as:

$$E_x, E_y, E_z \sim \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} \tilde{f}(k_{xmn}, k_{ymn}) e^{-jk_{xmn}x} e^{-jk_{ymn}y} e^{-jk_{zmn}z} \qquad \textbf{Eq. 3-10}$$

The x, y components of the wave vector can be defined as:

$$k_{xmn} = k_{x0} + \frac{2m\pi}{a}; \quad k_{ymn} = k_{y0} - \frac{2m\pi}{atan\gamma} + \frac{2n\pi}{b} \qquad \textbf{Eq. 3-11}$$

The (m, n) terms in the above infinite series are associated with the TM_{xym} (transverse magnetic) Floquet mode. A Floquet mode becomes a radiating or propagating mode only if the following condition is satisfied:

$$\sqrt{k_{xmn}^2 + k_{ymn}^2} \leq k_0^2 \qquad \textbf{Eq. 3-12}$$

The main lobe or fundamental Floquet mode is selected when $(m, n) = (0,0)$, while the grating lobes or higher order Floquet modes are taken into account for $(m, n) \neq (0,0)$. If the condition in Eq. 3-12 is not satisfied, then the corresponding Floquet mode is an evanescent mode that decays along the z-direction.

In a 2-D infinite array scenario, the number of simultaneous propagating Floquet modes and their directions of propagation can be determined graphically. If we consider a rectangular grid ($\gamma = 90°$), the mode numbers for the (m, n) Floquet mode can be obtained as:

$$k_{xmn} = k_{x0} + \frac{2m\pi}{a}; \quad k_{ymn} = k_{y0} + \frac{2n\pi}{b} \qquad \textbf{Eq. 3-13}$$

Combining the Eq. 3-13 and Eq. 3-12, we obtain the Eq. 3-14 that represents a family of circular regions of radii k_0, as depicted in **Figure 3-6**.

$$(k_{xmn} - \frac{2m\pi}{a})^2 + (k_{ymn} - \frac{2n\pi}{b})^2 \leq k_0^2 \qquad \textbf{Eq. 3-14}$$

Each (m, n) Floquet mode is depicted by a circle of center $(\frac{2m\pi}{a}, \frac{2n\pi}{b})$. The shaded circle centered at the origin corresponds to the dominant Floquet mode. The circular area inside the dominant mode circle represents the visible scan region. The other circles around the dominant one refer to the higher order Floquet modes (grating beams/lobes). When higher order mode circles intersect with the dominant-mode circle, the grating lobes enter in the visible scan region of the main lobe as reported in **Figure 3-6**. A necessary condition for

this does not occur is that $k_0 < \frac{\pi}{a}$ and $k_0 < \frac{\pi}{b}$. Thus, an array will have only main beam in the entire visible region $[-\frac{\pi}{2}, \frac{\pi}{2}]$ if the following conditions are satisfied:

$$a \leq \frac{\lambda_0}{2}; \quad b \leq \frac{\lambda_0}{2} \qquad \textbf{Eq. 3-15}$$

Where λ_0 represents the wavelength in free space (calculated at a certain frequency f_0).

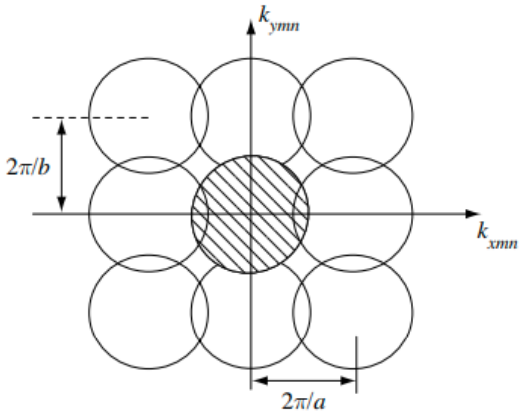
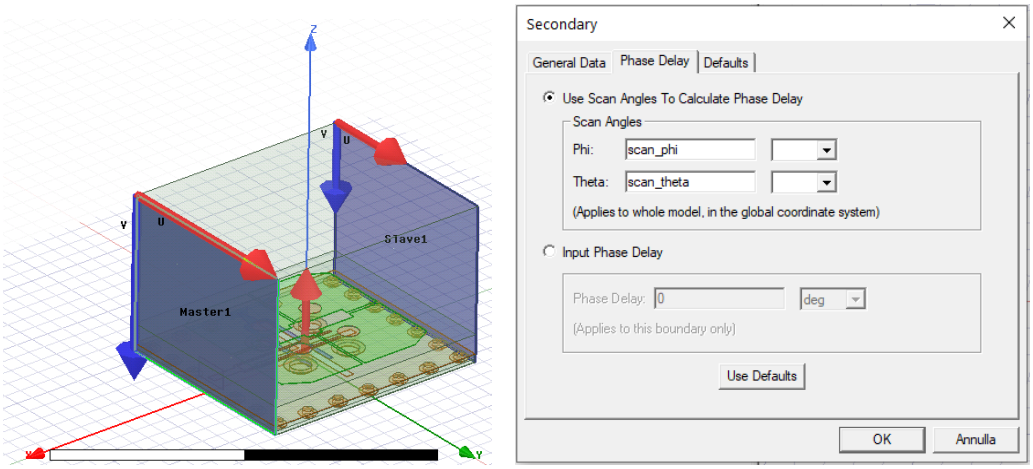


Figure 3-6: Floquet modes diagram for rectangular lattice.

The above analysis can demonstrate that the obtained results for a rectangular grid are similar to those that could be obtained by applying the conventional method of the Fourier series expansion (as shown in section 3.2).

In Ansys HFSS environment, a two-dimensional infinite array can be represented by enforcing field periodicity on the lateral faces of the unit radiating cell through master/slave boundaries pairs as reported in **Figure 3-7 -a**. This means that the Floquet series expansion can be performed along two dimensions to solve the radiation problem of a 2-D infinite array. By this analysis is possible to evaluate the mutual coupling effects on some array parameters, such as Active Impedance and Active Element Pattern, when the scan angle of the array changes. In particular, HFSS gives the possibility to set two different scan angle

variables on the slave boundary (**Figure 3-7 -b**) of the unit cell to observe the mutual coupling effects along the azimuth and elevation planes [21].



a) b)

Figure 3-7: Unit cell in infinite array (Ansys HFSS). a) master/slave boundaries; b) setting of the scan angle variables on slave boundary.

The biggest advantage of using this procedure is that the performance in terms active reflection coefficient and active element pattern of large phased arrays can be estimated accurately considering very short simulation times and a minimum RAM and storage space usage [21]. The only limitations related to this method are listed below:

- The effects of the edge elements are ignored because the infinite array simulation is performed on the unit cell.
- The magnitude taper is not allowed because only an excitation signal is applied at the unit cell.
- The mutual coupling terms are not available in post-processing. Only by finite array simulations it is possible to get the mutual coupling data.

3.3.1 Simulation of a unit cell in infinite array environment

In the following, it is reported an example of infinite array analysis performed by HFSS on the unit cell shown in section 3.2.1. As reported in **Figure 3-8**, when the isolated radiating cell is put in an infinite array scenario, the presence of mutual coupling Z_{in} in the Eq. 2-16 causes a mutual variation of the impressed currents of both neighboring elements and the unit cell and, consequently, an alteration of the array behavior in terms of Active impedance or Active Reflection Coefficient (ARC).

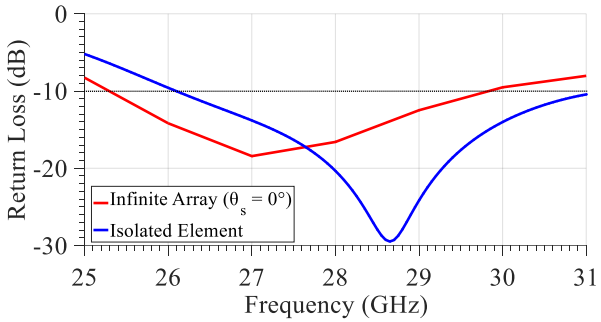


Figure 3-8: Return loss (E plane or AZ cut) comparison between isolated cell and unit cell in infinite array scenario.

If the direction of the radiating beam is changed along azimuth and elevation planes, the mutual coupling will affect the active impedance (Eq. 2-16) differently depending on the scan angle value θ_0 and the selected scan plane as shown in **Figure 3-9 -**a and **Figure 3-9 -b**. Although the mutual coupling effect is taken into account in the simulation of the unit cell, for a scan range of ±55deg in azimuth and ±20deg in elevation the ARC is lower than -10 dB from 26.5 to 29.5 GHz (n257 band). Moreover, no spikes appear on ARC plots along azimuth and elevation directions (or, equivalently, E and H planes) into the band of interest, which means that there will not be gain blind spots at different frequencies. This aspect can be confirmed by the values of the grating lobe frequencies, obtained by the Floquet conditions listed in Eq. 3-5, which are outside the n257 band.

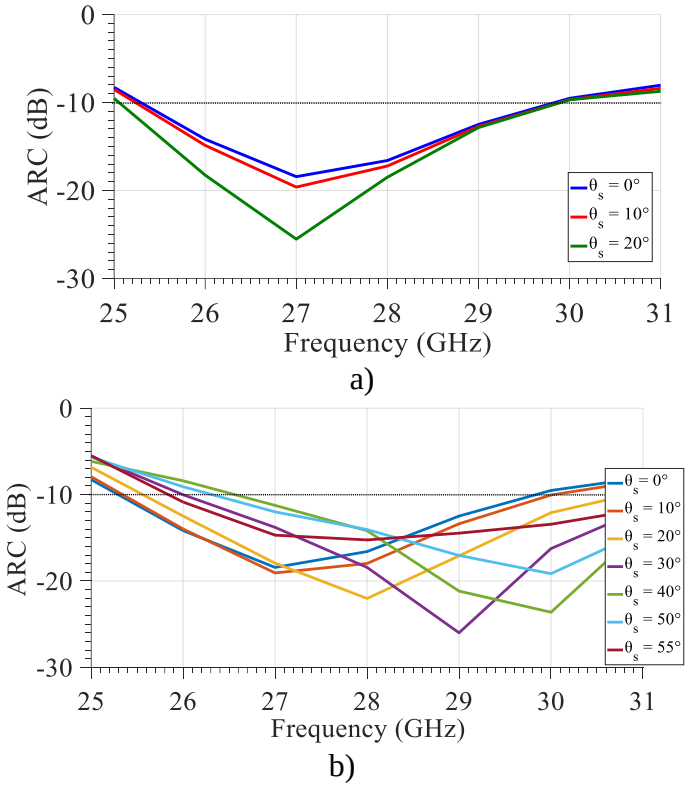


Figure 3-9: Active Reflection Coefficient (ARC) of the unit-cell into an infinite array for different scanning angles. (a) elevation; (b) azimuth.

3.4 Finite array analysis

This last step of the design process is important in several aspects. First of all, the simulation of the finite array is the most accurate as all the electromagnetic phenomena occurring in the structure are taken into consideration. Hence, it is possible to evaluate the mutual coupling effects between array elements (*horizontal approach*) due to the spatial interactions, the presence of surface and/or leaky waves inside the PCB stack-up etc. Moreover, if the BFN networks are considered in the layout, it is also possible to include the mutual interactions between feeding lines of different radiating elements for the computation of the coupling terms [16]. As second aspect, by comparing the ARC and AEP results of the radiating cells in the central region of a large array with the ones obtained by

infinite array analysis, it can be estimate graphically the degree of accuracy of the infinite array simulations [16]. In the HFSS environment, the most intuitive method that can be adopted for creating a finite-sized array is to replicate manually the unit cell according to the physical dimension of the lattice. Compared to the infinite array method, no field periodicity by master/slave condition is applied on the unit cell. Therefore, an *explicit simulation* will be directly performed in this domain [21][22]. In addition to the above considerations, the designer can modify in the post-processing phase the direction of the radiating beam by changing dynamically the phase of the excitation signal for each element. Moreover, magnitude tapers such as Taylor, Chebyshev, etc. can be applied to shape the radiation pattern of the array. A big drawback of this method is that the requirements in terms of RAM and storage space could be critical if large arrays are taken into account. In this scenario, a greater complexity of the meshing process and an increased number of excitation signals can lead to an exponential growth of the simulation times [21][22]. Just to give an idea, using 12 CPU cores to run the explicit simulation of a dual-polarized Vivaldi antenna array with 256 excitation ports [22], the solving time increases up to 122 hours with a RAM usage of 211 GB.

In Ansys HFSS software has been recently introduced a new, innovative simulation approach called *Domain Decomposition Method (DDM)*. This procedure offers the possibility to create a planar and/or linear antenna array by replicating the unit cell in a finite number of elements as shown in **Figure 3-10**. To achieve this purpose, the field periodicity is forced by master/slave conditions on the lateral faces of the radiating cell. In this scenario, there is no need to create manually all the array ports, as the software will replicate them by assigning a name according to the position of the element in the array. This aspect will lead to a reduction of setup times compared to ones of the explicit case.

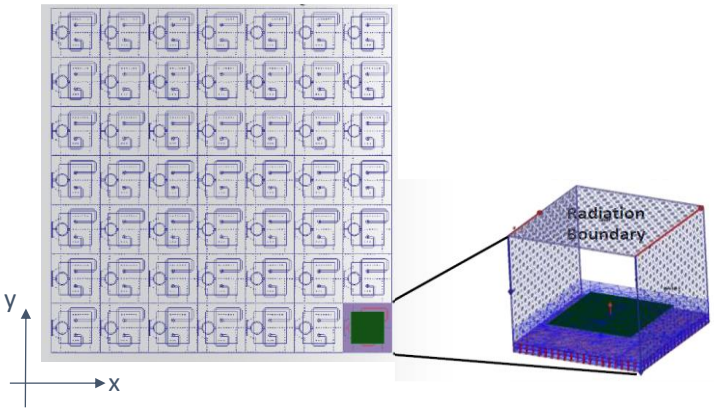


Figure 3-10: Creation of 2-D finite array by DDM method.

Similar to the explicit simulations, all the information such as the mutual coupling terms evaluated as the scan angle varies, the edge element effects and others can be treated by DDM in the post-processing phase. Moreover, a specific magnitude/phase taper can be applied on the ports of the finite array to change dynamically the radiation pattern characteristics. The great advantage of using the DDM approach is that very accurate results which match the HFSS explicit simulations can be obtained with a reduced use of hardware resources. In particular, by using the same mesh of the master/slave cell for the finite array and enabling a distributed multi-core analysis, the simulation times and the RAM usage can be reduced drastically [22]. For instance, in [21] the performance of a DDM finite array and an explicit array, both using 64 dipole antennas, have been compared. Considering the same array size and hardware computation power, DDM uses up to 63% less RAM it is 2.2X faster, while providing similar results with respect to the explicit simulation as reported in **Figure 3-11**.

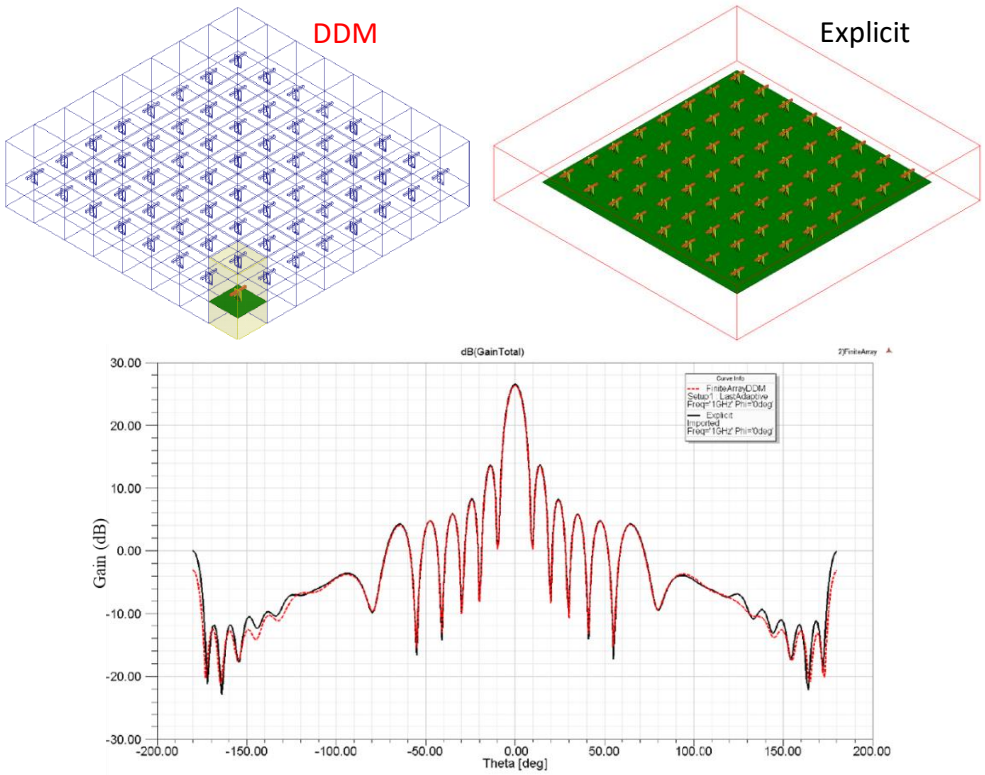


Figure 3-11: Comparison between DDM (red) and explicit 64-element array (black) [21].

If only the radiated fields of the DDM finite array are saved during the simulation, the solve time can be further reduced because the software will not save the field inside the array structure (e.g. PCB substrate) [20]. Moreover, if it is necessary to determine the array performance considering a specific amplitude/phase pattern at the excitation ports, the user can set the feeding option called *composite excitation* on the HFSS layout project. Hence, the software will analyze the structure considering only this excitation pattern, thus reducing significantly both solve time and disk space [22].

3.4.1 Finite domain simulation of a phased array

In this section, a finite array of 32 elements was analyzed by applying the *explicit* approach due to the lower complexity of the structure and sufficient availability of

computing resources. The radiating cell used to create manually the array refers to the one used in the section 3.2.1. Only radiated fields are included in full-wave simulation setup to reduce the solve time in this domain. In **Figure 3-12** is reported the 4 x 8 rectangular array, where the spacing values along x and y axes are chosen equal to $a_{cell} = 5.2mm$ and $b_{cell} = 6.8mm$ to avoid grating lobes in the scan range ($\pm 55°$ AZ, $\pm 20°$ EL).

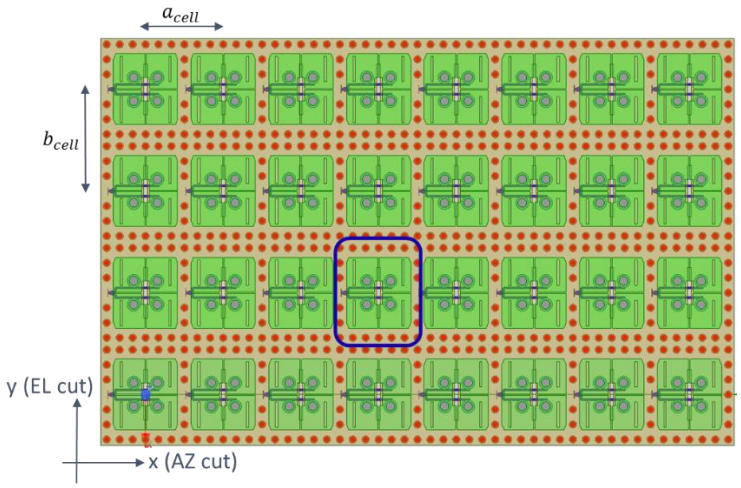


Figure 3-12: Explicit 4x8 rectangular ME dipole array.

Comparing the ARC of an element located in the central area of the array (marked in blue in **Figure 3-12**) together with the one of the infinite array for different scanning angles along elevation (H plane) and azimuth (E plane), it can be seen that as the number of array elements increases the ARC curves start to fit to the one of the infinite array. Therefore, **Figure 3-13** confirms that if the array is electrically large, the results of the infinite array are a good approximation of the ones obtained in the finite domain.

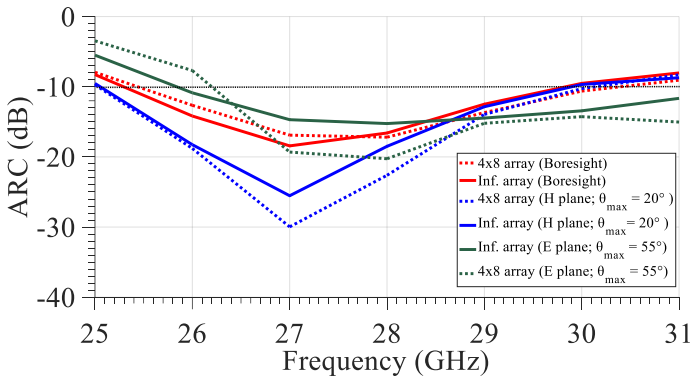


Figure 3-13: ARC comparison between Finite and Infinite array simulations.

Figure 3-14 shows that the mutual coupling between elements in an array causes distortions on the radiation pattern of the central element (the blue one in **Figure 3-12**) compared to the ideal case of the isolated element. Moreover, this analysis confirms that there are not gain blind spots on AEP of the central element in the specific scan range.

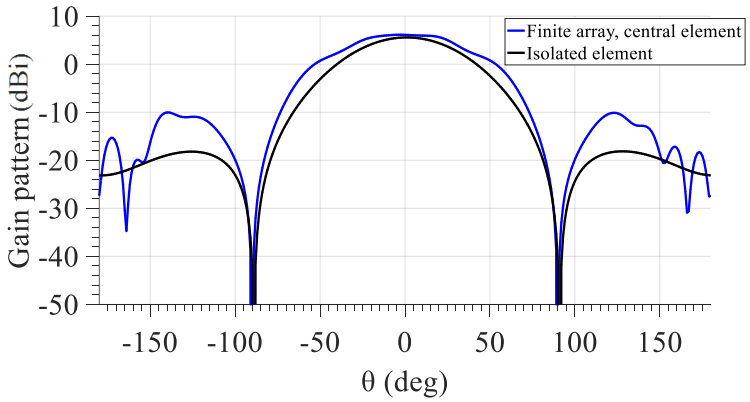


Figure 3-14: Comparison between AEP of the array central element and radiation gain of the isolated element at 28GHz.

Finally, the radiation patterns at 28 GHz of the 4×8 array when scanning along elevation and azimuth are reported in **Figure 3-15 -a** and **Figure 3-15 -b**. As expected, when the scan angle along azimuth and elevation planes increases, the half-power beamwidths and, consequently, the scan losses increase as well according to the E-plane and H-plane amplitude patterns of the single radiating element.

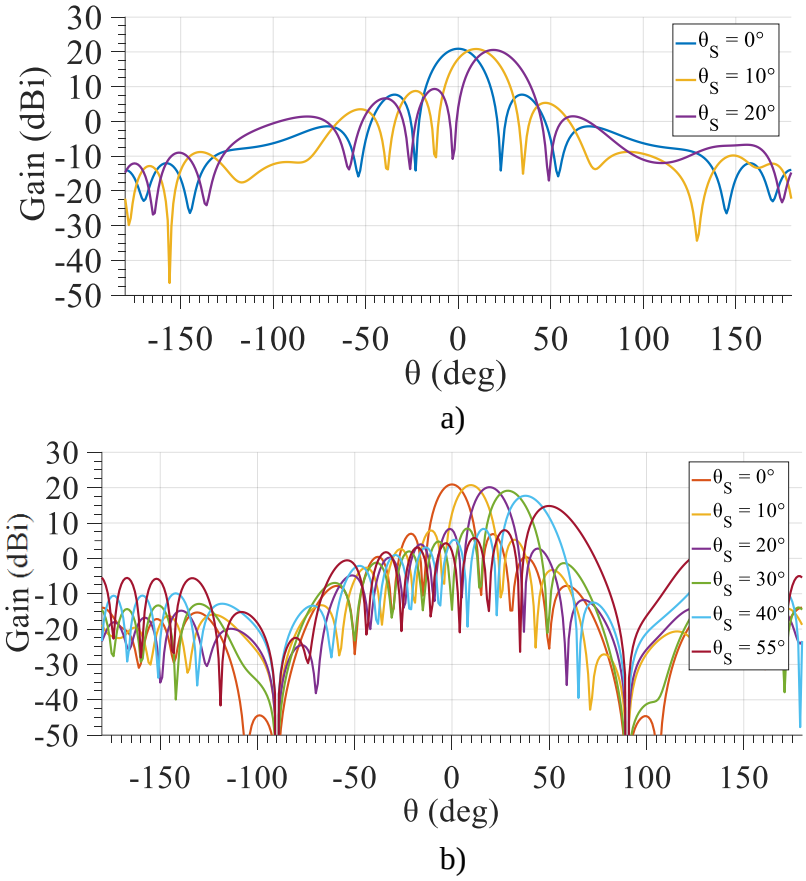


Figure 3-15: Array radiation pattern at 28GHz for different scanning angles. (a) elevation plane; (b) azimuth plane.

4 Ka-band antenna array for 5G small cells

4.1 Introduction

As described in chapter 1, the next generation of wireless communication systems, which is called 5G, aims to significantly improve the performance of the actual mobile technology (4G) in terms of data-rate, network latency and capacity, link robustness, etc. This scenario will be achieved thanks to the development of innovative network

infrastructure to satisfy ever-increasing user expectations of Quality of Experience (QoE) [13] [23]. Among the new features mentioned above, the use of phased arrays at mm-wave bands will permit a path to support multiple users, which are located in a specific area, with high data rates by establishing high-bandwidth directional links between the base station (BS) and mobile user terminals. By implementing massive MIMO technologies, phased arrays will manage multiple simultaneous beams to serve more terminals, using spatial multiplexing, and each BS will steer the beams electronically to serve the latter using time division multiplexing (TDM) access. In **Figure 4-1** is shown a potential 5G network scenario [6] [23] consisting of:

- millimeter-wave 5G phased-array small cells, that require operating power values lower than the macro BSs, placed on buildings or street lamps communicating with user handheld terminals.
- 5G auto-cells in cars communicating with millimeter-wave 5G base stations to provide high data-rate and low latency connectivity.
- point-to-point mm-wave links that provide a connection between phased-array small-cells and backhaul network.

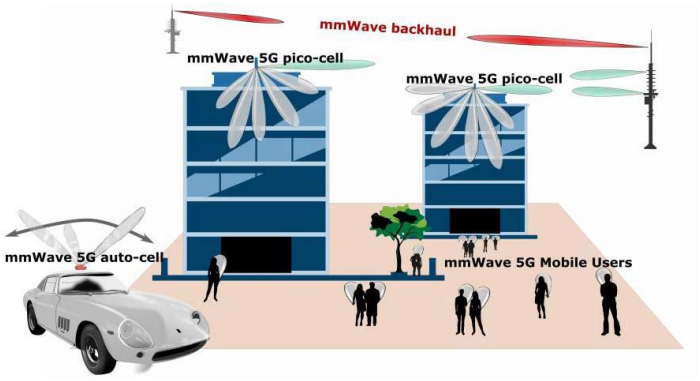


Figure 4-1: Potential 5G network scenario [13].

4.2 Array requirements

To realize a dense, heterogeneous network scenario like the one shown in **Figure 4-1**, each 5G phased array small-cells should be placed at a distance that varies from 100 to 300 m to increase both coverage area and the capacity of the network and to support multiple user connections. Regarding the operating frequencies of the base stations in the 5G NR (radio access network), in the latest ITU recommendations have been identified different frequency portions in Ka-band such as the aggregate 26.5-29.5 GHz (n257 band) with $f_0 = 28GHz$. System requirements also indicate that EIRP values should vary from 40 to 75 dBm for communication distances between BS and user equipment ranging from 100 to 300m [24] [25]. To achieve these EIRP values, the radiating elements number for each array in BS should be between 32 to 1024 (depending on the transmitters power). The modulation schemes up to 256-QAM should be used to establish directional links with a data rate per user $R_b \geq 1Gbps$. The work reported in [24] confirms that an array of 32 elements can enable 2D-MIMO in Ka-band 5G small-cell with EIRP value higher than 40dBm and a data rate ~ 1Gbps at 16QAM for a link distance of 300m. The latest works in literature have revealed that a method to increase channel capacity by up to 2X is to use the two available orthogonal polarizations [26][27]. This solution not only leads to an increment of the maximum number of simultaneous users that can be supported but also opens a path to the implementation of self-backhauling [28], where one polarization can be used to establish a link between small-cell and backhaul network. In this scenario, the isolation between V and H polarization channels must be sufficiently high to ensure low inter-user interference values. Due to massive MIMO, each group of antennas, which is selected on the array surface, can manage at least a radiating beam to connect the user to

the network. Therefore, the mutual coupling between antennas should be as low as possible to avoid that higher values of inter-channel interference can lead to a significant decrement of the signal-to-noise (S/N) performance. Finally, the phase resolution of phase shifters should be as high as possible to minimize the beam steering error and to improve the side-lobes suppression [13]. To satisfy all planning system constraints listed above, all the requirements used for the design of phased array are in **Table 4-1**.

Table 4-1: Phased array requirements.

Technology	Multi-layer AiP
Operation BW	26.5 – 29.5 GHz
Reflection Coefficient	< -10 dB
Polarization	Dual linear
H to V isolation	> 25 / 30 dB
Cross-polarization pattern	< -30 dB
Isolation between antenna elements	> 15 / 20 dB
Maximum beam steering range	$\pm 55° H, \pm 20° V$
Side lobe level	< -13 dB
Boresight Gain	> 18 / 20 dBi per tile
Array configuration	4 x 8 per tile; 8 tiles

4.3 Array architecture

The shift of operating frequency in mm-wave band, required by the 5G phased array systems, implies a decrease in the size of the array (considering a fixed number of radiating elements) and a consequent reduction in the available space for both the realization of RF routing lines inside the antenna stack-up and the integration of the MMIC TRX chip. To

make the integration aspects even more complex, there is certainly the need to control multiple beams irradiated from different portions of the array, while performing beam-steering operations along with two directions (azimuth and elevation). Moreover, the support of dual-polarization operation leads to both an increment of the channel number on the TRX chip and a further reduction of the available space to accommodate more RF transmission lines inside the antenna stack-up. Therefore, it is important to find a solution to realize all the antenna functionality in a package with a smaller form-factor. The solution adopted in [26] was to use four 28 GHz TRX chips with a smaller channel number (equal to 32), each of which is connected to a 4x4 sub-array identified on a square lattice of 64 - $\lambda/2$ spaced radiating elements. The stacked-patch antennas are placed on the top layer of the stack-up and an air cavity is formed between the lid and base substrates in the package to increase antenna bandwidth, and, at the same time, reduce the impact of surface waves. Quasi-coaxial multi-layer feeding lines are implemented in the base substrate of the package and they are used to drive the signal from the RFIC ports to the antennas and vice-versa. By this configuration, each transceiver manages a TX/RX beam per polarization in TDD mode. Regarding the integration process, each IC transceiver is flip-chip attached to the bottom side of the multi-layer stack-up and each connection is carried out to an external PCB via BGA solder balls as reported in **Figure 4-2**.

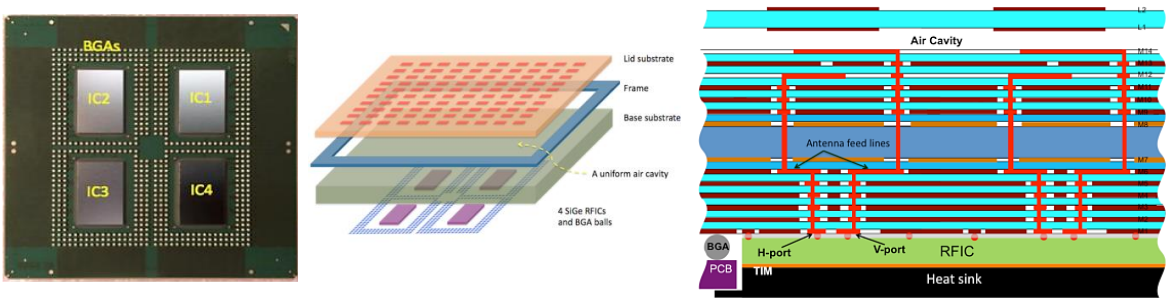


Figure 4-2: Architecture of an AiP phased array and its integration process [26].

In this work, a similar approach to [26] is used for the design of a dual-polarized 32-elements rectangular array operating at 28GHz. **Figure 4-3** shows the multi-layer stack-up which is conceived for the full integration of a system-in-package as it includes both layers dedicated to the antenna integration and specific layers for the accommodation of transmit (TX) and receive (RX) beam forming networks (BFNs) as well as the DC biasing and control lines. This stack-up consists of a regular structure, where two dielectric layers are bonded together by a very thin prepreg layer, which is repeated periodically to form a quasi-symmetrical structure that includes 14 metal layers, 7 dielectric cores and 6 prepreg slabs. The overall thickness of the multi-layer package is 2.2mm. The dielectric core and prepreg materials and their relative dielectric permittivity and thickness are shown in **Figure 4-3**. In most of the examples proposed in the literature [26][29], complex packages use air-gaps or thick dielectric cores to increase bandwidth, but this solution could reduce both yield and reliability over time and increase the manufacturing complexity of the antenna. Moreover, the increment of antenna stack-up thickness could be not practical for many low-profile applications. Therefore, the use of thin dielectric core D1 with thickness of 508 um in the proposed stack-up could be a solution to overcome these limitations.

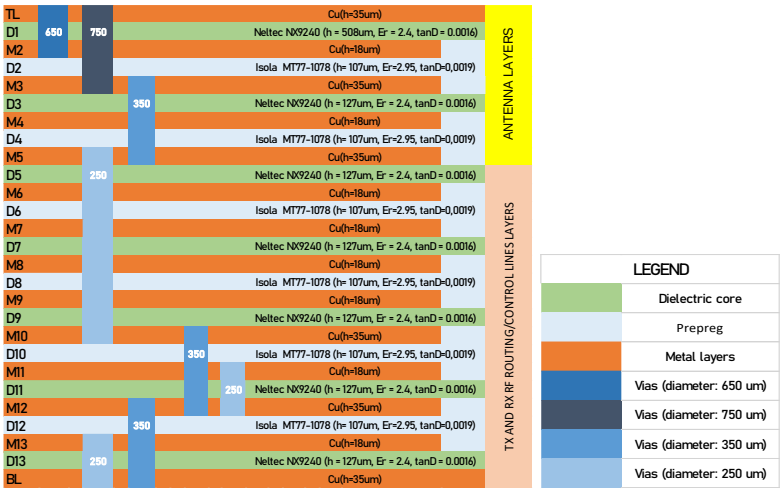
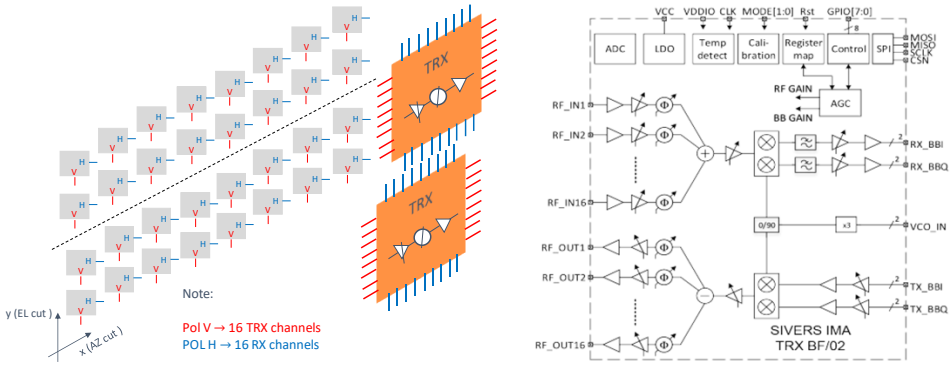


Figure 4-3: Proposed multi-layer stack-up.

To enable both MIMO and spatial multiplexing in full-duplex mode, the proposed array should manage multiple beams per polarization. To achieve this goal, two 32-channels TRX chips with an integrated analog beam-forming system will be used. Each IC transceiver, that controls half of the array, has 16 transmit (TX) channels and 16 receive (RX) channels which are connected separately to the two polarizations as reported in **Figure 4-4 -a**. From this configuration, 8 horizontal beams and 4 vertical beams per polarization can be generated. Two TRX chips are flip-chipped to the bottom layer of the multi-layer stack-up and the entire system will be connected to an external PCB via BGA solder balls as for the reference architecture in [26].



a) b)

Figure 4-4: 32-element dual-polarized phased array tile. a) architecture; b) circuit scheme of TRX chip.

In the following is presented the design of the isolated radiating element, which will be realized in the multi-layer stack-up shown in **Figure 4-3**, which operates in the 26.5 – 29.5 GHz band (n257) and supports the dual-polarization operation. At this point, the design of a 32-elements dual-polarized array with beam-steering capability along azimuth and elevation planes has been reported. The scanning performance of this structure, including the impact of mutual coupling effects, has been proved by infinite array analysis in HFSS and the obtained simulations have been compared to the ones found with the DDM finite

array method. Prototypes of both the isolated antenna element and the passive structure of the array (without the two beam-forming TRX circuits) have been realized and the measurements have been performed by a specific software-based system in an anechoic chamber.

4.4 Ka-band dual-polarized antenna

4.4.1 State of the art on wideband antennas

Millimeter-wave antennas can be used for the implementation of ultra-wideband (UWB) systems to satisfy the requirements, in terms of data rate per user and the capacity, of the future 5G network. Therefore, the design of these radiating structures must be done with the purpose to improve both the impedance bandwidth and the radiation characteristics. The most common wideband antenna topologies found in literature are: stacked patch antennas [26][29][30]; slotted patch antennas [31][32][33]; parasitically-coupled patch antennas [34][35] and slot antennas [36][37][38]. In the first configuration a printed antenna, which is indicated as the excitation patch, is used to drive an additional parasitic patch, which is located vertically on a different metal layer. This vertical coupling mechanism introduces an additional resonance, compared to the single patch configuration, thus enlarging the impedance bandwidth and also improving the gain. Dielectric layers or air-gaps are usually used to separate the driving patch from the parasitic one. As an example, the design of a Ka-band dual-polarized stacked patch, with a feeding network based on the use of two orthogonal, independent feeding slots, is reported in [29]. In this structure, an air-gap of thickness equal to 1.65mm ($0.16\lambda_0$ at 29 GHz) between upper and lower patch is used to enlarge the percent bandwidth up to 23% at f_0. The use of air-gap

and the presence of a metal grid surrounding the antenna leads to an improvement of the gain, that is 6dBi at f_0, due to the suppression of surface wave modes. In the second topology, some cuts that have a specific geometry (e.g. E-shaped, H-shaped etc.) are realized on the radiating surface of a patch antenna. These discontinuities create multiple paths where the current can flow and radiate, and this behavior generates more resonances, thus improving the impedance bandwidth of the radiator. In the work proposed in [33], an E-shaped cut is made on a printed antenna that is realized on a multi-layer stack-up with a height of 1.12mm ($0.15\lambda_0$ at 40GHz). In this case, an aperture realized on a SIW transmission line is used to excite the patch, thus further improving the impedance bandwidth and the antenna radiation characteristics. In the third family, some metallic elements are coupled horizontally to the main patch that is located on the same metal layer. Similar to the stacked patches, this interaction generates additional resonances, thus extending the operating bandwidth of the antenna. In the structure shown in [35], a U-shaped parasitic patch is coupled to a patch antenna operating at 28 GHz which is printed on a low-profile multi-layer stack-up. The measurement results in terms of impedance bandwidth are similar to the one obtained in [29]. Finally, the slot antennas are radiating structures realized by a slot in a conducting surface which is excited by a specific feeding system (e.g. coaxial probe, microstrip line, etc.) [39]. As in slotted patch antennas, the performance in terms of impedance bandwidth and cross-polarization change depending on the shape of the slot [32]. Slot antennas can be implemented in waveguide structures [36], printed on dielectric layers [38] or realized in SIW technology [37]. The dual-polarized radiator proposed in [37] was conceived considering a low profile SIW cavity where a crossed slot is cut on the top of this resonant structure and fed differentially by two off-center microstrip probes per polarization. This feeding mechanism generates a double

resonance thus improving the impedance bandwidth up to 19% and achieving a H-V isolation higher than 28dB. Although fractional bandwidth from 15 to 40% for VSWR ≤ 2 and directional radiation characteristics can be achieved by these conventional topologies, the beamwidth could change rapidly across the frequency as well as the radiation gain [40] [41]. Moreover, high cross-polarizations usually appear, especially in the upper frequency band portion, but this effect could be mitigated by using some techniques such as antiphase cancellation, twin - L probes coupled feed and irregular shaped ground plane [41].

Recently, a novel complementary antenna named Magneto-Electric (ME) dipole has been proposed [40]. By exciting simultaneously a magnetic dipole and an electric dipole, this composite antenna achieves excellent performance in terms of bandwidth (43% for VSWR ≤ 1.5) and other electrical characteristics such as low cross-polarization, low back radiation, symmetric E-plane and H-plane radiation patterns, and very stable gain across frequency [40][41]. In light of this, researchers and designers have taken advantage of these features for the realization of more performing array structures [42][43] to employ in the latest mobile communication systems.

4.4.2 Magneto-Electric dipole theory

The ME dipole consists of a horizontal half-wavelength planar patch antenna (operates as an electric dipole) and a vertical-oriented quarter-wave shorted patch antenna (operates as a magnetic dipole) [40][41], which form a kind of complementary antenna as depicted in **Figure 4-5**.

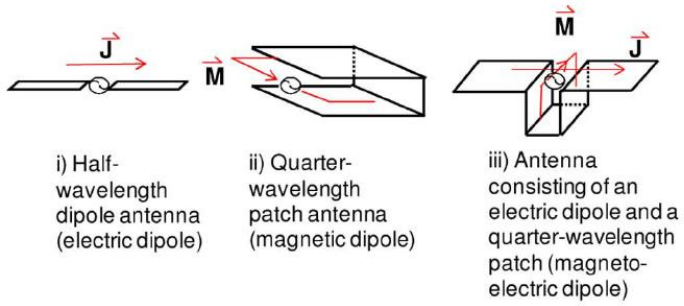


Figure 4-5: Principle of operation of the antenna [41].

The radiation results due to the combination of them can be described by **Figure 4-6**. From dipole theory, it is well known that electric dipole has an '8'-shaped radiation pattern on the E-plane and an omnidirectional radiation pattern on the H-plane. The magnetic dipole has a complementary behavior, which means an '8'-shaped radiation pattern in the H-plane and an omnidirectional radiation pattern in the E-plane. By combining a y-aligned electric dipole and an x-aligned magnetic dipole, the forward radiation of the ME dipole is reinforced, whereas the back radiation is reduced. Therefore, if both dipoles are excited simultaneously with proper amplitude and phase, symmetrical radiation patterns along both E- and H- planes can be obtained as reported in **Figure 4-6**. The total electric field of the ME dipole in the far-field region can be expressed as follows [44]:

$$\vec{E} = j\frac{E_y dxdy}{2\lambda r}\left[e_\theta \sin\varphi\,(1+\cos\theta) + e_\varphi cos\varphi(1+cos\theta)\right]e^{-jkr} \qquad \textbf{Eq. 4-1}$$

$$F(\theta) = \frac{(1+cos\theta)}{2}$$

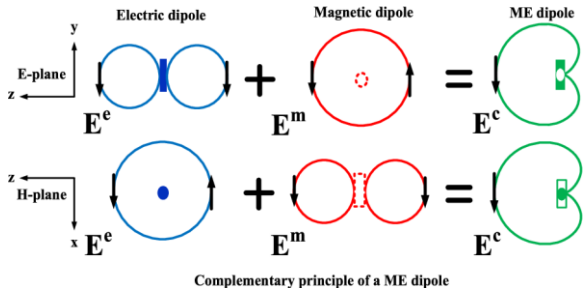


Figure 4-6: Synthesis of the ME dipole patterns [44].

According to Eq. 4-1, when θ = 180°, F(θ) = 0, which shows that the ME dipole has a low back lobe. From a technological perspective, this type of antenna was not originally conceived for integration in PCB structures. Only one decade ago, it has been demonstrated how this type of radiator can be effectively integrated into a standard multi-layer PCB for millimeter-wave applications. In the last few years, thanks to the recent studies on the ME integration on PCB, several examples of printed ME dipole have been proposed in the literature by varying the shape of the radiating elements or by using different feeding configurations [45]. However, to date, most of the proposed solutions are all based on dielectrics with a thickness of $0.25\lambda_0$ (λ_0 is the free-space wavelength at f_0) which are not practical in many applications. To overcome this issue, several evolutions of the original design are proposed in literature. For instance, in [46] the possibility to capacitively load the vertical plates of the magnetic dipole is investigated for metal-only structures, whereas in [47] a trapezoidal-shaped magnetic dipole is used to reduce the height of the radiator. Another solution applied on a multi-PCB ME dipole [44] exploits the combined effect of a slotted elliptical electric dipole and a defected ground layer to reduce significantly the profile of the antenna. In this work, the design of a novel ultra-low profile dual-polarized Magneto-Electric dipole operating at 28GHz for 5G phased array applications has been proposed. This structure has been realized considering the original work in [48].

4.4.3 Description of the radiating structure

As mentioned above, the proposed antenna is designed to operate in the n257 frequency band ($f_0 = 28\ GHz$) considering high isolation levels between two polarizations. The radiator, including the H and V power dividers, is built in the first part of the multi-layer stack-up as shown in **Figure 4-7**:

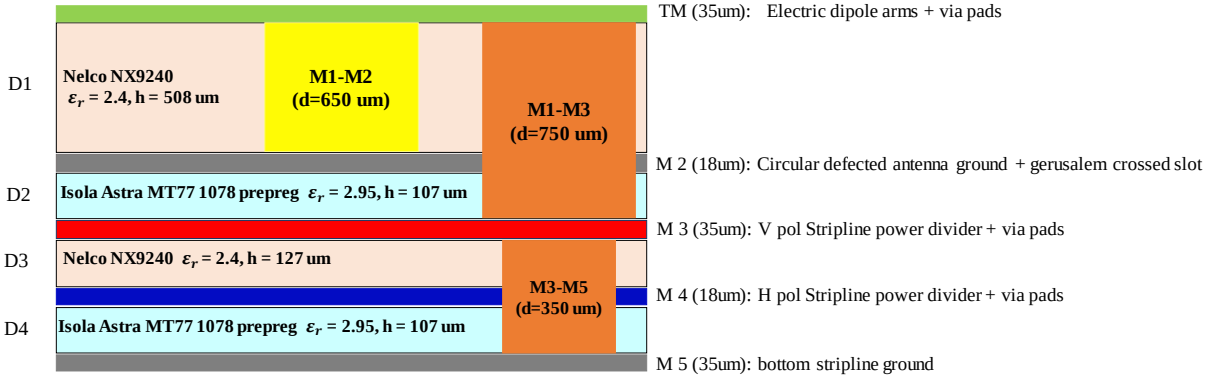


Figure 4-7: Antenna stack-up.

In **Figure 4-8** is reported the geometry of the Magneto-Electric dipole. Since this radiating cell will be used to realize a rectangular lattice array, the dimensions W_{cell} and L_{cell} (reported in **Table 4-2**) have to be chosen to avoid grating lobes in the $(u - u_0,\ v - v_0)$ visible space when $\vartheta_{0\ maxAZ}$ = 55° (along azimuth or y-direction) and $\vartheta_{0\ maxEL}$ = 20° (along elevation or x-direction) based on the following formula:

$$L_{cell} < \frac{\lambda}{1+sin(\vartheta_{0\ maxAZ})} = 0.55\lambda_0\ (5.89\ mm\ at\ f_0 = 28\ GHz)$$

$$W_{cell} < \frac{\lambda}{1+sin(\vartheta_{0\ maxEL})} = 0.74\lambda_0\ (7.92\ mm\ at\ f_0 = 28\ GHz)$$

Eq. 4-2

As shown in **Table 4-2**, W_{cell} it has been chosen $> 0.74\lambda_0$ for feasibility and technical constraints related to the accommodation of the array feeding networks. For this spacing

value, grating lobes could appear in the visible space along the elevation plane at the operating frequency f_0.

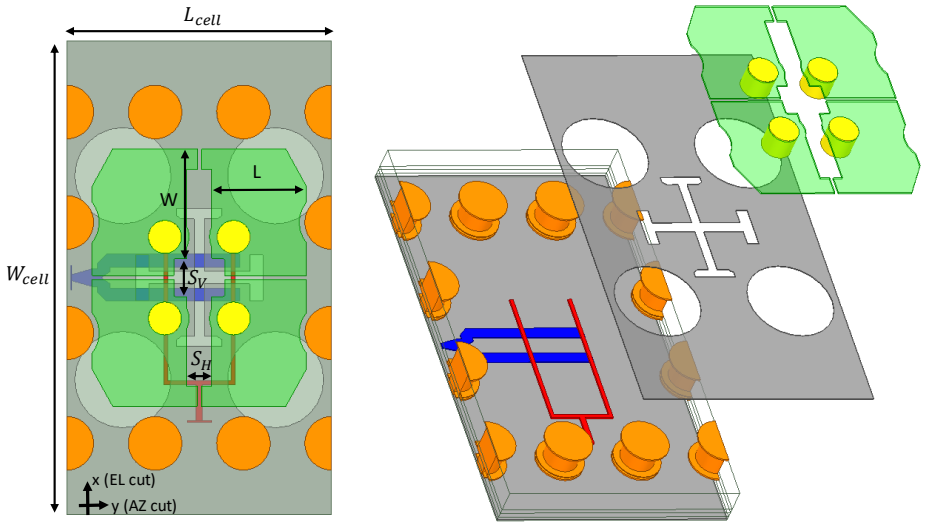


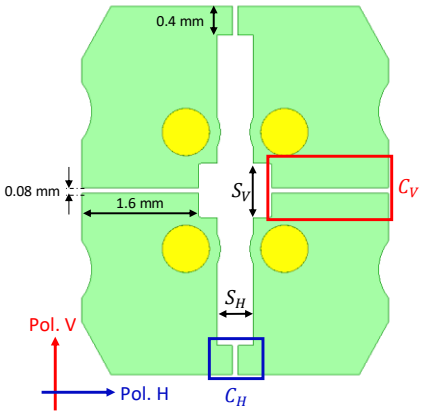
Figure 4-8: ME dipole geometry. a) top view; b) 3D exploded view.

Table 4-2: Characteristics of the antenna.

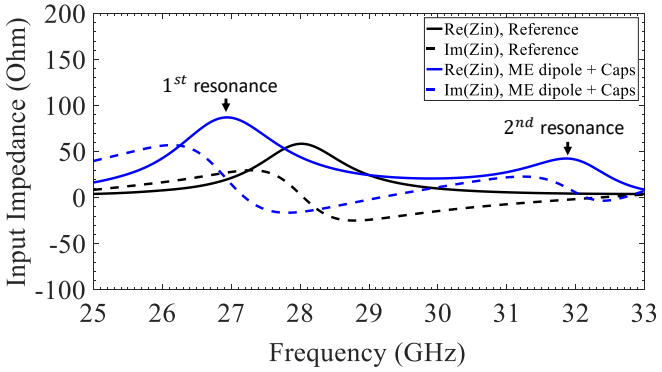
Parameters	L_{cell}	W_{cell}	**L**	**W**	S_V	S_H	**h**
Values	5.2 mm (0.485 λ_0)	9.3 mm (0.87 λ_0)	1.85 mm	2.15 mm	0.75 mm	0.5 mm	0.884 mm (0.083 λ_0)

Considering the layout depicted in **Figure 4-8**, four planar patches placed on top metal (TM) layer act together to form an electric dipole. The length L and the width W of each patch are respectively 1.85 mm and 2.15 mm, which are equal to 0.26 λ_g and 0.31 λ_g (λ_g = guided wavelength at f_0 for ε_r = 2.4). M1 – M2 blind vias (i.e. the yellow ones in **Figure 4-7**), that connect the patches to a ground plane on M2 layer, produce a magnetic dipole. As reported in [44][49], when the antenna height is decreased from the conventional value of $\lambda_g/4$, the second resonance frequency related to the vertically-oriented loop antenna (i.e. magnetic radiator) is shifted upward. This profile reduction also leads to an increase of the

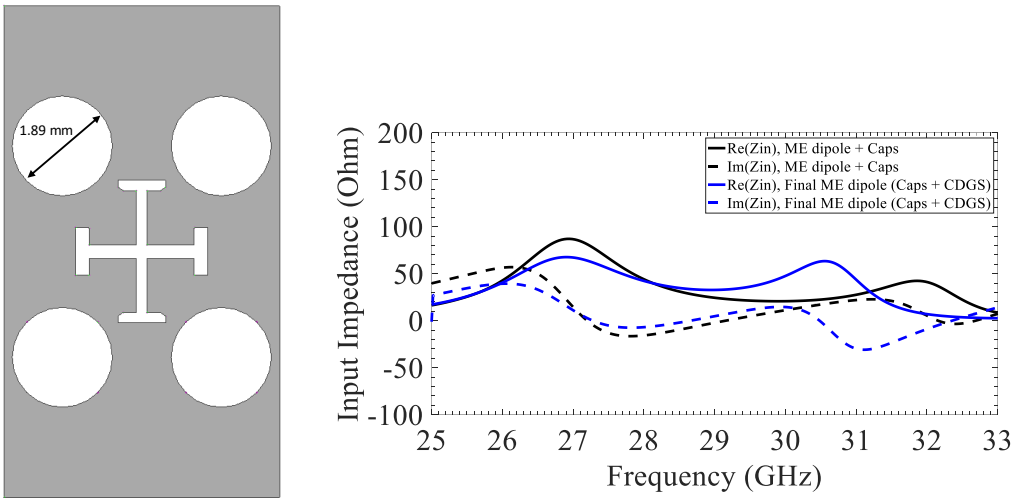
impedance mismatch in the band of interest. To overcome this issue, the only-metal ME dipole in [46] uses two discrete capacitors C_L, connected between the vertical plates of magnetic dipole whose height is $0.1\lambda_0$, to shift the position of the magnetic resonance to lower frequencies, thus achieving a good matching level (VSWR < 2) in a wide bandwidth. In this work, the magnetic dipole was embedded in a dielectric core D1 having a height equal to 508um ($0.073\lambda_g$ or $0.047\lambda_0$ at 28 GHz). To compensate the effects of the antenna profile reduction, two printed coupled-line capacitors are placed horizontally between arms of the electric dipole to load capacitively the antenna feeding gaps S_V and S_H, referred to H and V polarizations, as depicted in **Figure 4-9 -a**. The values of capacitors $C_H = 10fF$ and $C_V = 47fF$ were estimated directly in HFSS by replacing them with sheets where ideal capacitive boundaries have been used. Compared to the reference structure, this additional capacitive effect generates a second resonance close to the first resonance of the electric dipole as reported in **Figure 4-9 -b**. This aspect leads to a reduction of return loss for both polarizations on a broader frequency band (due to better equalization of the real/imaginary part of the input impedance) as shown in **Figure 4-10 -a** and **Figure 4-10 -b**.



a)



b)



c) d)

Figure 4-9: Details on proposed ME dipole. a) geometry of coupled-line capacitors; b) effects of the capacitors on impedance response (shown only for V polarization); c) circular defected ground structure (CDGS) on M2 ground layer; d) CDGS effects on impedance response (shown only for V polarization).

As illustrated in **Figure 4-8 -a** and **Figure 4-9 -a**, the corners of the patches have been cut to adjust the impedance matching level at the edge frequencies [30]. Considering the section referred to the feeding system, two stripline balanced power dividers are placed orthogonally on two different metal layers, i.e. M3 for V polarization and M4 for H polarization as reported in **Figure 4-7**. These elements are used to enable dual-polarization mechanism by exciting a Jerusalem slot which is cut on M2 ground layer. It is well-known in the literature that the balanced feeding system brings considerable advantages as it reduces the cross-polarization of the microstrip antennas while providing more stable radiation patterns at higher frequencies [30].

In this work, another component called Defected Ground Structure (DGS) is used to improve the antenna performance in terms of return loss [44]. In particular, four cuts are used to realize a circular defected ground structure (CDGS) on M2 layer as illustrated in **Figure 4-9 -c**. By creating these discontinuities on the ground plane, the length of the

magnetic current path for both polarizations is extended. Consequently, the equivalent length of the magnetic dipole is increased, while maintaining a low profile of the antenna ($0.073\lambda_g$ or $0.047\lambda_0$ at $28\ GHz$). This results in a shift of the second resonance that makes the trends of the input resistance/reactance flatter (**Figure 4-9 -d**), thus further improving the impedance bandwidth for both polarizations as shown in **Figure 4-10 -a** and **Figure 4-10 -b**. Finally, an external cage realized by stacked M1-M3 and M3-M5 vias (marked in orange in **Figure 4-8 -b**) is used to avoid the presence of parallel-plate modes in the stripline section and reduce the inter-element mutual coupling due to the surface wave propagation.

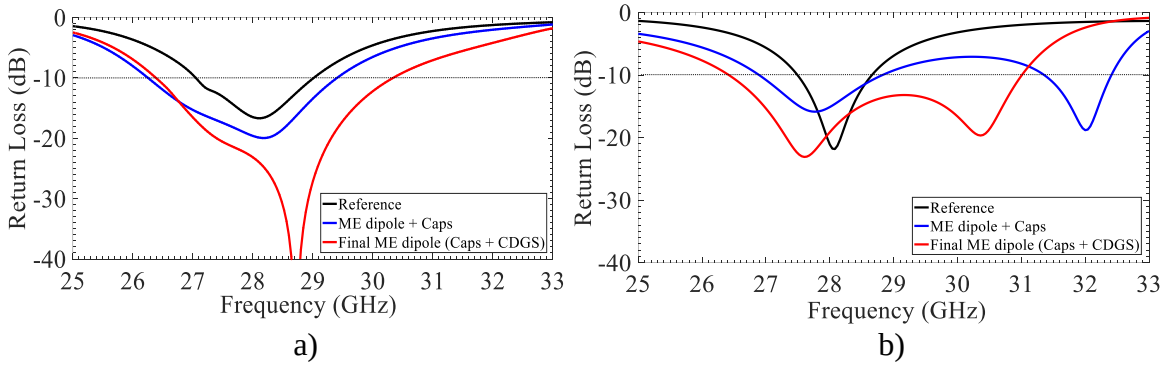


Figure 4-10: Effects of two different techniques over Return Loss response. a) H polarization; b) V polarization.

All mentioned simulations were performed by Ansys HFSS software considering a value of port impedance for both polarizations equal to 50 Ω. The simulated current distributions at 28GHz for V polarization in the proposed low-profile ME-dipole antenna are shown in **Figure 4-11**. It can be seen that at times t = 0 and T/2, the radiation is dominated by the current that is located inside the gap on the inner edges of the horizontal patches, which indicates that the magnetic dipole is excited [42]. On the other hand, at time t = T/4 and 3T/4, the current is concentrated on the major portion of the horizontal patches outside the gap, which indicates that the electric dipole in x direction is excited. Therefore, the planar

electric dipole and the vertical magnetic dipole are excited alternately with similar strength, thus obtaining the complementarity of the antenna [42].

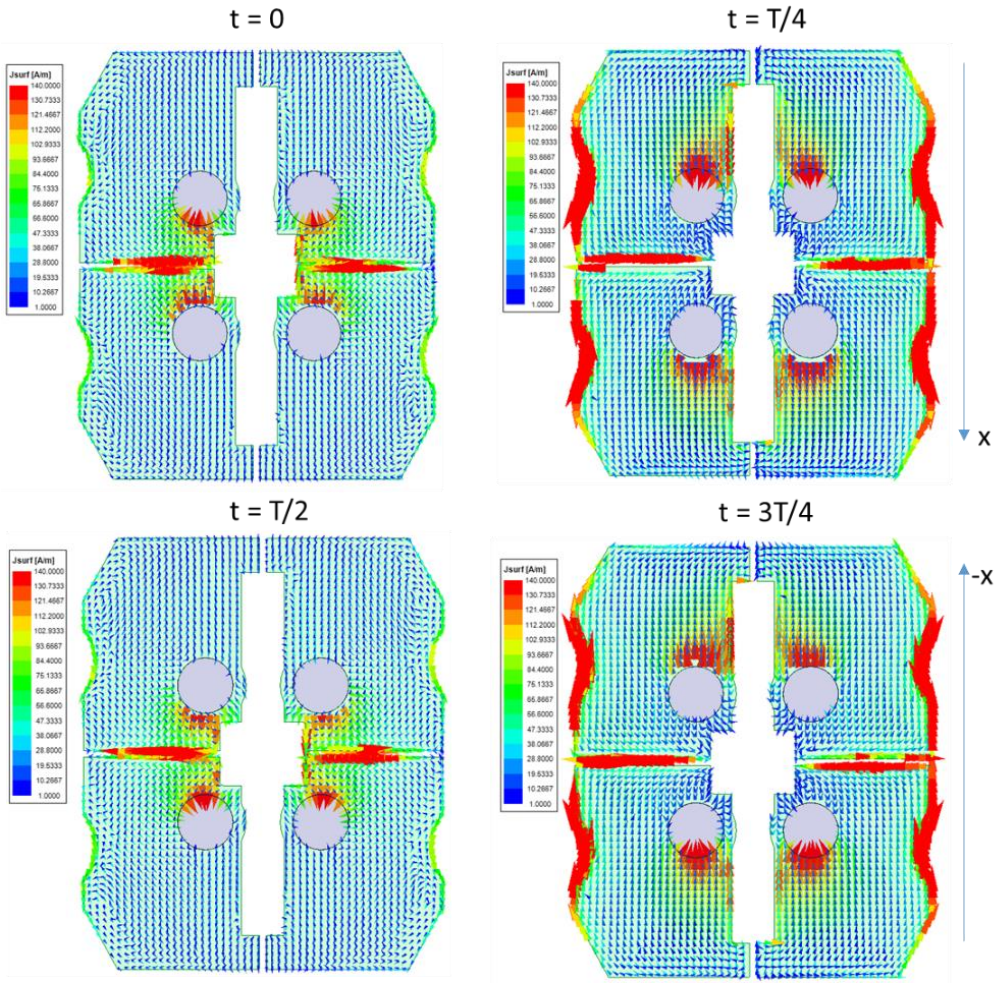
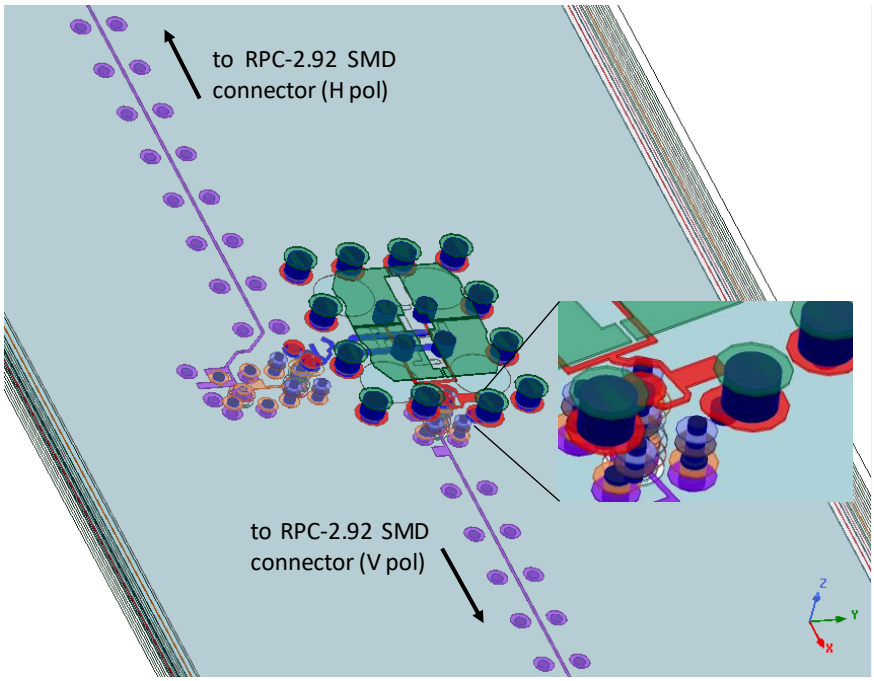


Figure 4-11: Current distributions in the proposed antenna for different periods (shown only for V polarization).

Regarding the implementation of the feeding networks for the antenna prototype, multi-level quasi-coaxial RF transitions are built in the lower part of the stack-up as reported in **Figure 4-3**. The role of these elements is to direct the signals of both polarizations from the connectors, whose access points are located on the bottom layer (BL) away from the radiating element, to the inputs of two power dividers in TX mode or vice versa in RX mode (**Figure 4-12 -a**). In particular, for the H polarization circuit are employed two multi-

layer transitions (**Figure 4-12 -b**), the first one routes the signal from M4 to M11 layer and the second one directs it from M11 to M13 layer, while for the V polarization network is used a single M3 to M13 quasi-coaxial transition (**Figure 4-12 -c**). To better accommodate an open stub connected near the input of the V pol. power divider, only one M1-M3 via of the antenna cage is moved outward as depicted in **Figure 4-12 -a**. Each RF transition is made by using metallic vias defined between layers of the multi-layer stack-up (**Figure 4-3**). In **Figure 4-13** is reported the complete layout of the antenna, which includes the footprint of the connector used in this project (RPC-2.92 SMD connector from Rosenberger) and the access via that connects the CPW line of the connector (BL layer) with the input of the M13 long stripline used to drive both H and V signals.



a)

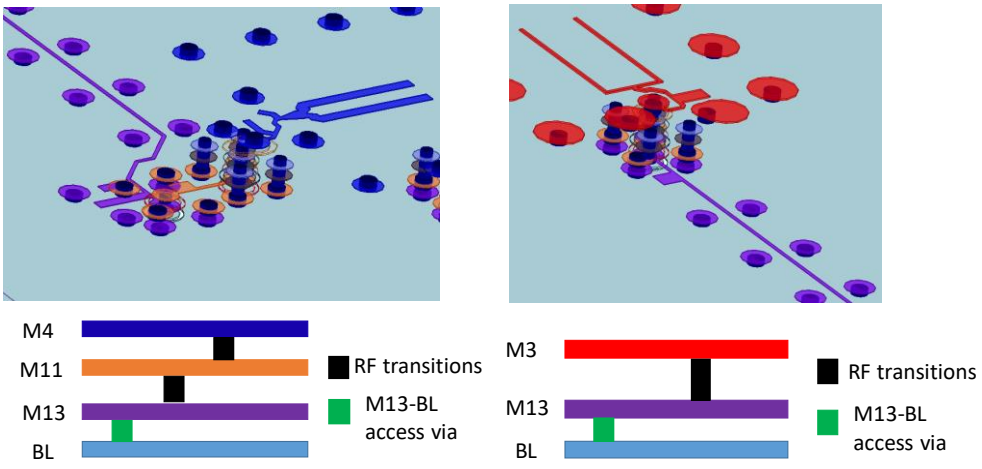


Figure 4-12: Realization of H pol. and V pol. feeding networks. a) dual-polarized ME dipole with multi-layer transitions; b) H polarization feeding system with the indication of the RF routing map; c) V polarization feeding system with the indication of the RF routing map.

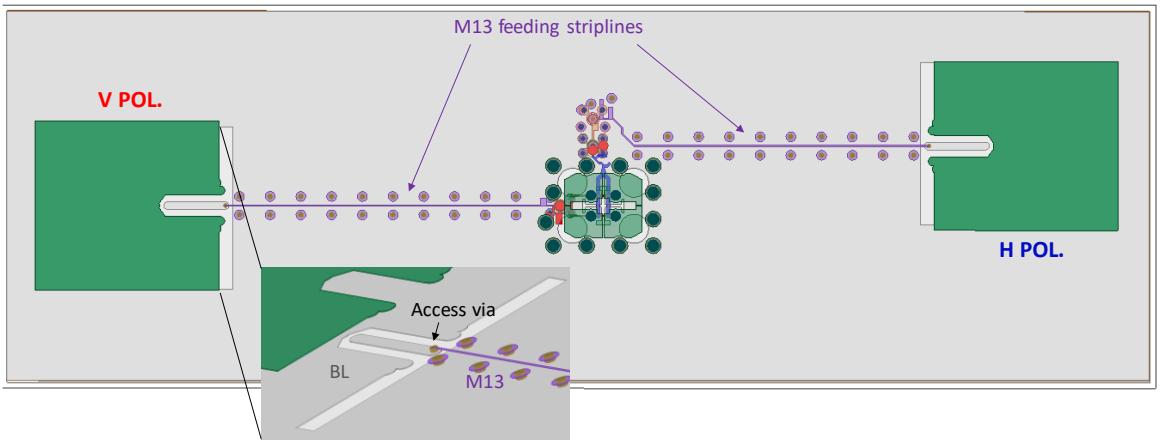


Figure 4-13: Layout of the ME dipole prototype.

4.4.4 Results and measurements

To demonstrate the performance of the proposed ultra-low profile dual-polarized ME dipole, a commercial electromagnetic solver (Ansys HFSS) has been employed. The simulations were performed considering all the ports matched to 50 Ω on the radiating structure, depicted in **Figure 4-8**, where both multi-layer transitions and long M13 feeding

striplines mentioned above have not been taken into account. As shown in **Figure 4-14**, return losses for both H and V polarizations are less than -10 dB and the H to V coupling level is less than -25 dB in the n257 frequency band (26.5 ÷ 29.5 GHz).

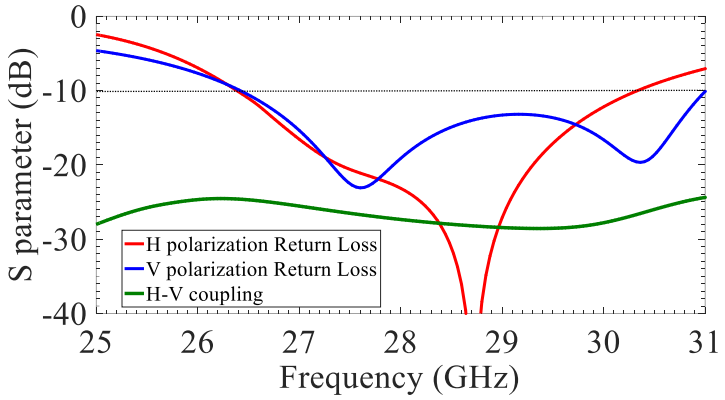


Figure 4-14: Simulated S-parameters of the radiator.

Considering the radiation performance for both polarizations, the realized boresight gain at 28 GHz is ≥ 6dBi, while the gain variations are kept below 1.5 dB in the band of interest as reported in **Figure 4-15**. From the normalized gain patterns evaluated at 28 GHz, which are depicted in **Figure 4-16 –a** and **Figure 4-16 –b** for both polarization, the radiator shows a front-to-back ratio higher than 15 dB and normalized cross-polarization levels less than -25 dB on both E and H planes. Moreover, the HPBW evaluated on both E and H planes is wider than 58° for both polarizations.

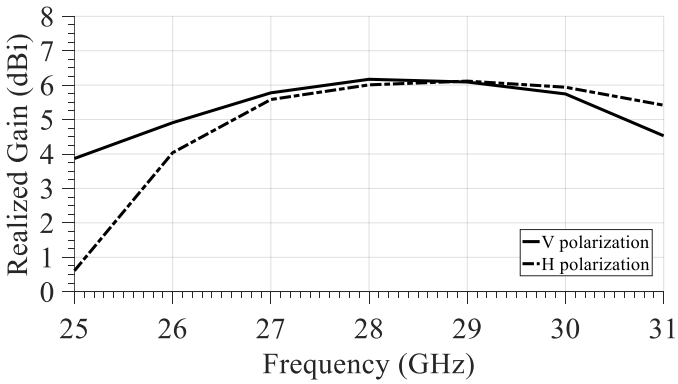


Figure 4-15: Realized boresight gain of the radiator.

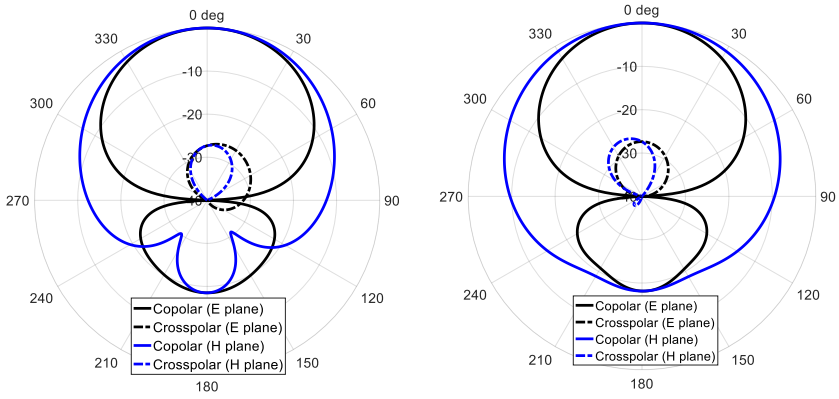


Figure 4-16: Simulated radiation patterns. a) H polarization; b) V polarization.

A picture of the realized prototype is reported in **Figure 4-17** (top view). The dual-polarized antenna has been fed with two Rosenberger RPC-2.92 SMD connectors, which are mounted so that the internal pins can touch the CPW lines placed on the lowest metal layer of the stack-up (bottom layer) as indicated in **Figure 4-13**. To perform the measurements of the gain, the antenna has been tested in an anechoic chamber by using a specific measurement system. As depicted in **Figure 4-18**, the antenna under test (AUT) and a wide-band standard horn were positioned one in front of the other at a distance of 88 cm which, considering that the longest side of the horn is 5.5cm, is the far field one. The characteristics of the wide-band horn are reported in **Table 4-3**.

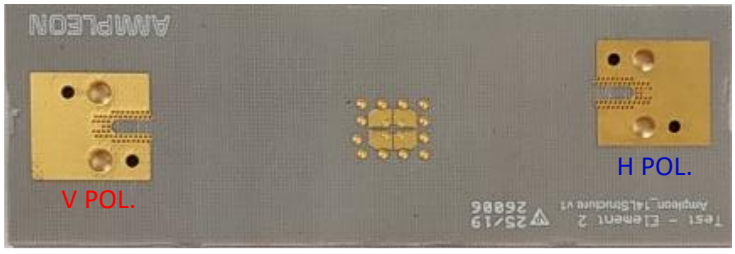


Figure 4-17: Top view of the realized prototype.

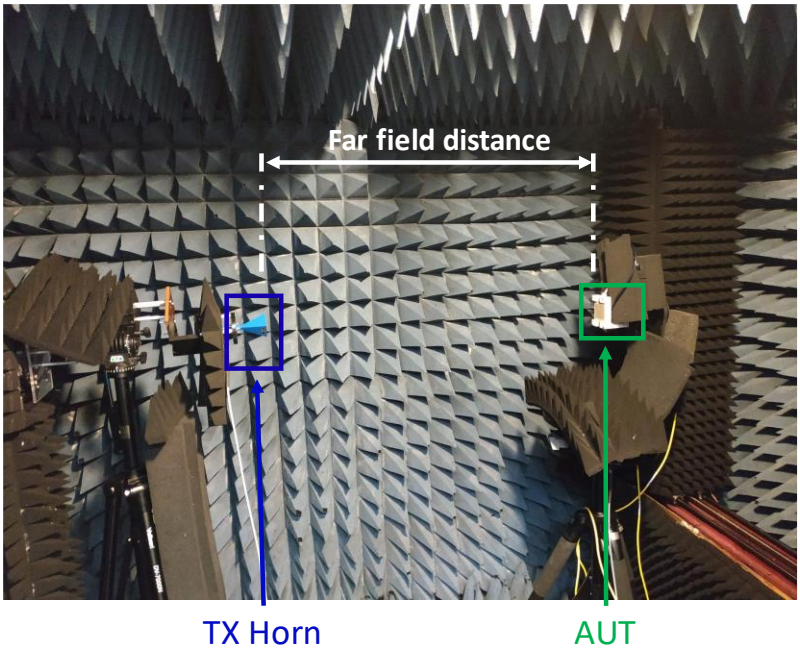


Figure 4-18: AUT and TX standard horn in the anechoic chamber.

Table 4-3: Gain values of the wide-band standard horn.

Frequency (GHz)	Gain (dBi)	Frequency (GHz)	Gain (dBi)
26.5	19.23	34.60	20.57
27.85	19.63	35.95	20.70
29.20	19.82	37.30	20.93
30.55	20.05	38.65	21.00
31.90	20.17	40.00	21.14
33.25	20.44		

In this setup, the horn is the TX source, while the AUT operates in RX mode. The horn is connected to the first channel of a vector network analyzer (VNA), while the H and V signals are sent in turn to the second channel of the VNA. A specific software reads these data from the VNA by GPIB interface and processes them. Finally, a specific MATLAB code uses these processed values to compute the gain patterns of the radiator. The

comparisons between measured and simulated copolar radiation patterns (E and H planes) for both polarizations are shown in **Figure 4-19 -a** and **Figure 4-19 -b**. Since no de-embedding procedure was performed to compensate for the effects of two long M13 feeding striplines and the losses of the connectors and adapters used in the measurement setup, only normalized plots have been taken into account in this analysis. As it can be seen, the discrepancies between simulation and measurement results are mainly due to the manufacturing process variations, which can be critical especially in Ka-band. Moreover, the EM effects of long multi-layer quasi-coaxial transitions could also affect the flatness of the measured radiation patterns.

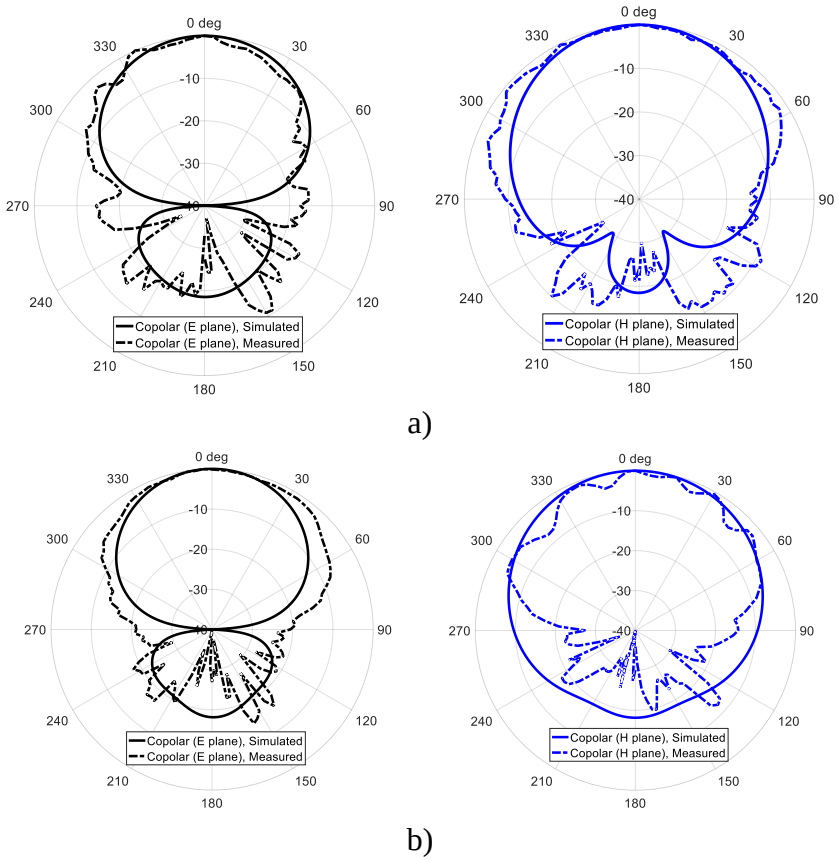


Figure 4-19: Comparison between simulated and measured normalized radiation patterns. a) H polarization; b) V polarization.

The measured S parameters were plotted separately in **Figure 4-20 -a**, **Figure 4-20 -b** and **Figure 4-20 -c**. As it can be noted, the strong impedance mismatch detected in the band of interest is because no TRL de-embedding procedure, which is used to mainly compensate the mismatch and losses introduced by long M13 feeding striplines shown in **Figure 4-13**, has been performed on the measured data yet. Therefore, the measured results were not compared with the simulated ones to avoid misunderstandings.

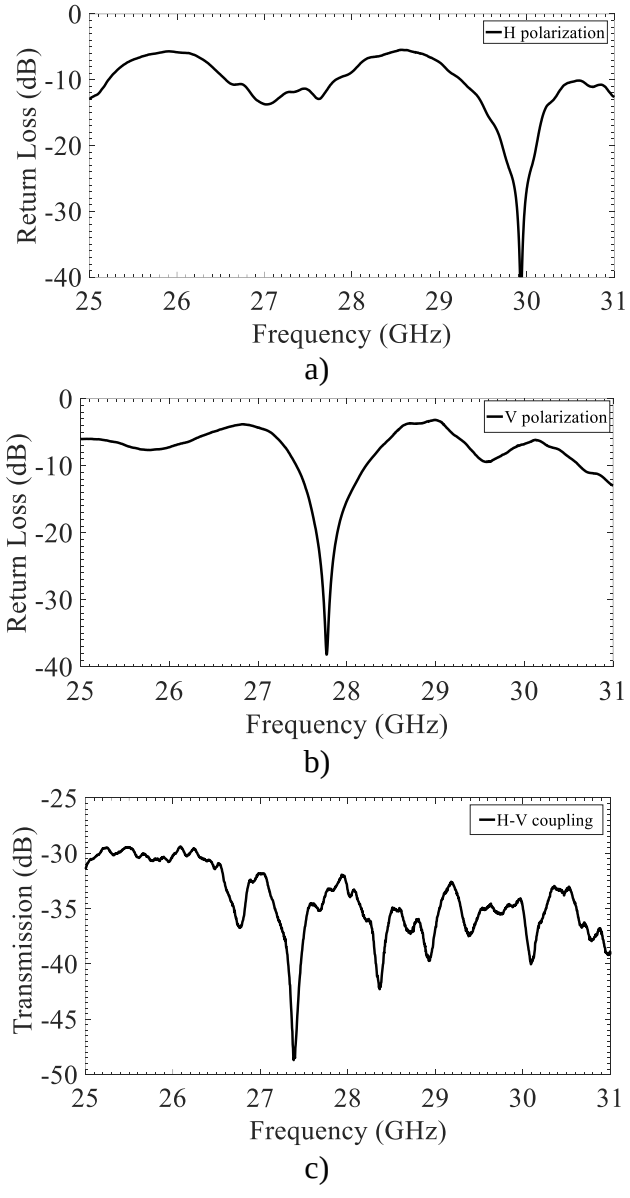


Figure 4-20: Measured S parameters of the radiator. a) H polarization return loss; b) V polarization return loss; c) H-V coupling response.

4.5 Ka-band dual-polarized antenna array

Following the design procedure described in chapter 3, the proposed radiating unit cell will be simulated in an infinite array environment, to evaluate the active reflection coefficient or active VSWR and the presence of the gain blind spots when scanning the beam along two planes (azimuth and elevation). The scan gain performance will be examined by simulating the unit cell in a 32-element rectangular finite array by DDM method. Finally, the measurement results of the passive dual-polarized array prototype will be reported and analyzed.

4.5.1 Infinite array analysis

In this section, the dual-polarized ME dipole antenna depicted in **Figure 4-8** is employed as the radiating unit cell in the infinite array simulation. As mentioned in section 3.3, an infinite array is modeled by enforcing field periodicity, along azimuth and elevation planes, through master/slave boundary pairs applied on the lateral faces of the radiating cell. By this analysis, it is possible to evaluate the effects of the mutual coupling in scanning on this infinite array of ME dipole antennas which are spaced W_{cell} along elevation direction and l_{cell} along azimuth direction. In **Figure 4-21** and **Figure 4-22** are reported the active VSWR plots for both polarizations when the beam is steered along azimuth and elevation directions up to 55° and 20°, as shown in the array specification in **Table 4-1**. When wider scan ranges are taken into account, the values of 2.5 and/or 3 are usually used as benchmarks to analyze the VSWR performance of the most phased arrays [50][51]. Considering the results for the H polarization, when the main beam is steered out boresight direction up to 30° along azimuth plane (E plane), the matching level in terms of active

VSWR improves from 3 to 2.5 at 29.5 GHz and from 2.5 to 2 at the operating frequency of 28 GHz. When the scan angle is higher than 30°, the mutual coupling behavior changes drastically, thus affecting heavily the VSWR values in all the band of interest. Considering the beam steering along elevation plane (or H plane), from 0° to 20° the matching level changes differently (from 3 to 1.5 at 29.5GHz and from 2.7 to 1.7 at f_0 = 28 GHz) compared to the one evaluated in the same scan range along azimuth plane (or E plane). This aspect is because the mutual coupling in the printed antennas is inherently unequal between E and H plane [16][17]. In any case, **Figure 4-21 -a** and **Figure 4-21 -b** show that the active VSWR is less than 3 in all the n257 band (26.5 ÷ 29.5 GHz) for all the scan angles values along two planes, except for the case where θ_S = 55° in azimuth direction.

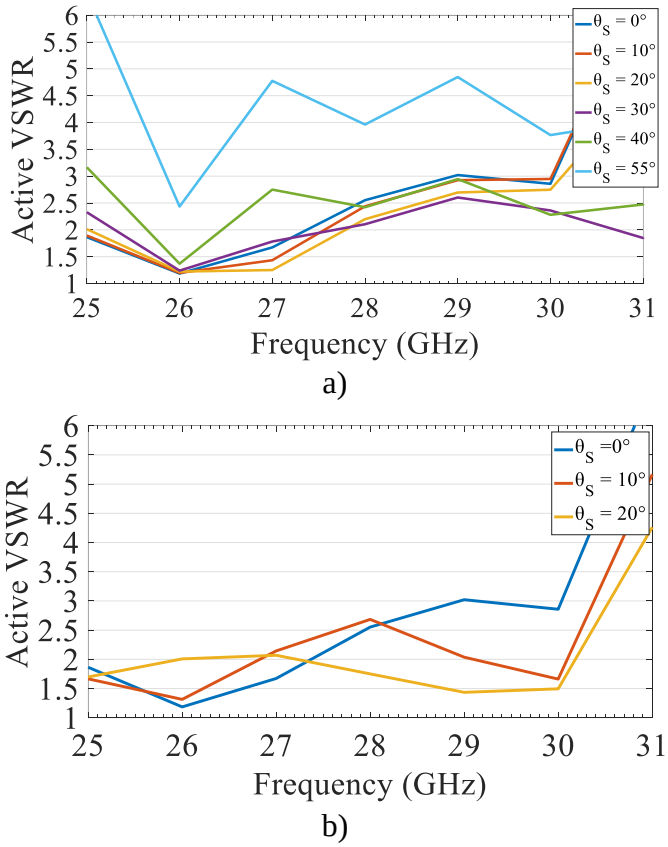


Figure 4-21: Active VSWR for H polarization. a) azimuth plane; b) elevation plane.

Observing the results obtained for V polarization, as the scan angle of the main beam increases along azimuth and elevation planes, the matching level decreases mostly in the highest part of the n257 band. This behavior is more evident along the azimuth plane (or H plane) compared to the elevation plane (or E plane) for the same reasons mentioned previously. **Figure 4-22 -a** and **Figure 4-22 -b** show that the active VSWR is less than 2.5 in all n257 band for all the scan angle values along azimuth and elevation planes, excepted for three specific pointing angles, namely 30°, 40° and 55° where the VSWR achieves a value of 3 close to 29.5 GHz as indicated in **Figure 4-22 -a** and **Figure 4-22 -b**.

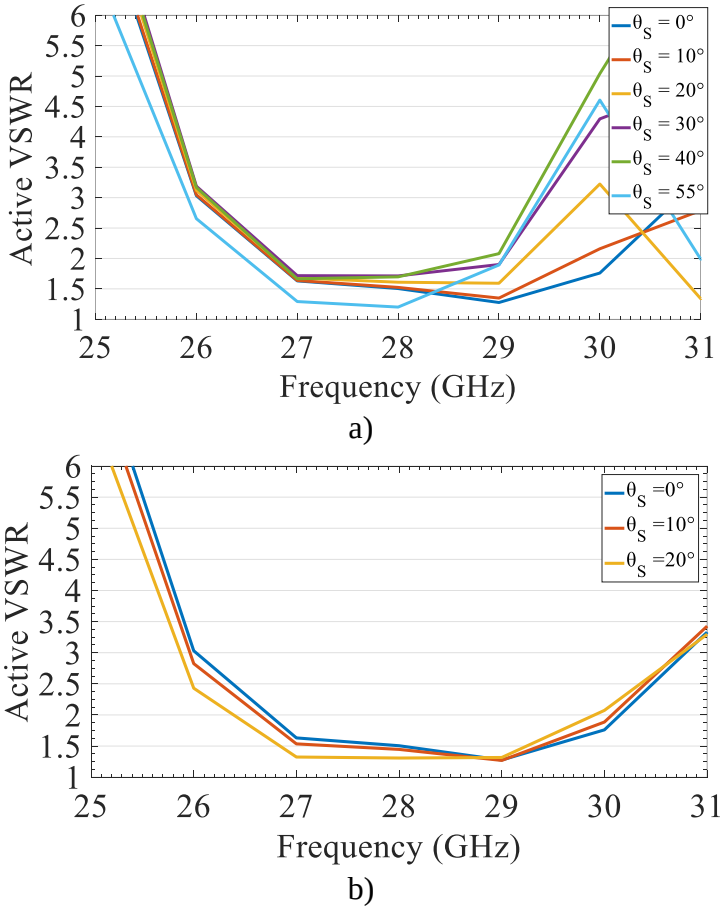


Figure 4-22: Active VSWR for V polarization. a) azimuth plane; b) elevation plane.

Figure 4-21 and **Figure 4-22** show that no positive spikes appear on active VSWR trends into the band of interest, which means that there will not be blind spots on the embedded element patterns for both polarizations, as confirmed by the radiation plots evaluated, for example, at f_0 = 28 GHz (**Figure 4-23 -a** and **Figure 4-23 -b**).

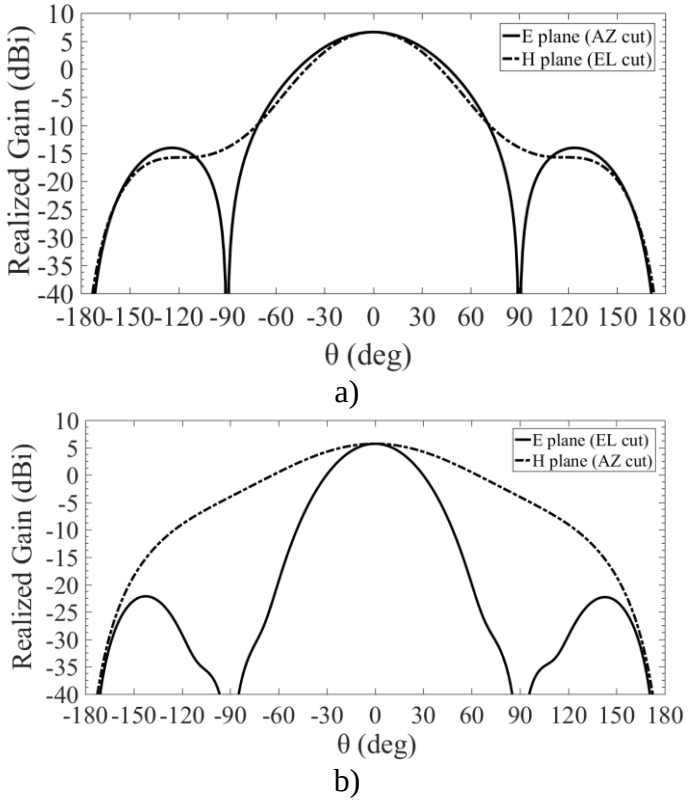


Figure 4-23: AEP patterns of the unit cell in the infinite array environment at 28 GHz. a) H polarization; b) V polarization.

4.5.2 Finite array analysis

Using the DDM procedure of Ansys HFSS mentioned in section 3.4, the simulation of a rectangular array of 32 dual-polarized antennas (i.e. 64 excitation ports) has been performed. In particular, the dual-polarized ME dipole depicted in **Figure 4-8** has been replicated equally along two planes (AZ and EL cuts), considering the x-axis and y-axis spacing values equal to cell dimensions, W_{cell} and l_{cell}, as shown in **Figure 4-24**.

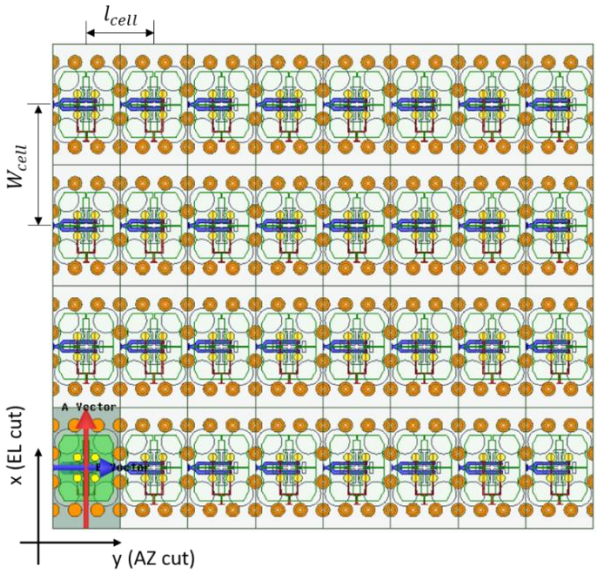


Figure 4-24: 32 element finite array (DDM method).

Figure 4-25 and **Figure 4-26** show the comparison between the active VSWR of an element located in the central area of the finite array and the active VSWR evaluated by infinite array analysis for both polarizations on specific scan angle values. The fitting between curves confirms that the infinite array results can be used to predict accurately the effect of the mutual coupling between the elements in a finite array of large dimensions. Therefore, the active VSWR results reported in **Figure 4-21** and **Figure 4-22** can be taken as a reference in this analysis.

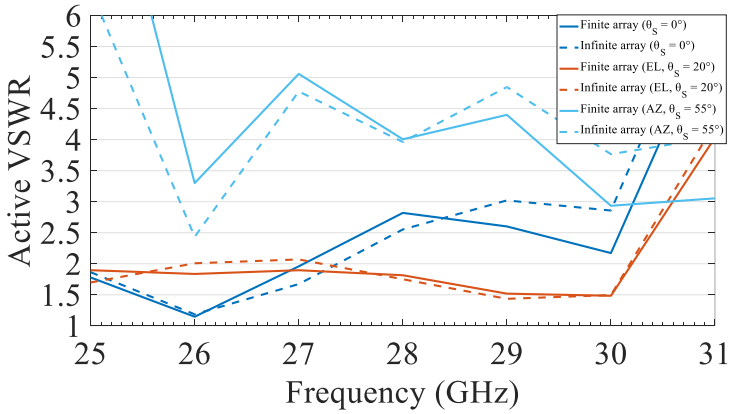


Figure 4-25: Performance comparison in terms of active VSWR (H polarization).

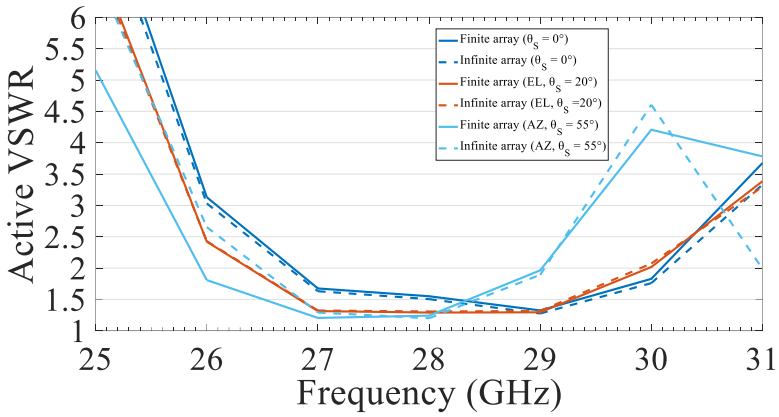


Figure 4-26: Performance comparison in terms of active VSWR (V polarization).

The radiation patterns at 28 GHz of the finite array, when scanning along two directions in the scan range ($\pm 55° AZ, \pm 20° EL$), are reported in **Figure 4-27** and **Figure 4-28**. As it can be seen, the maximum scan losses at 55°AZ and 20°EL are different between the two polarizations. This aspect is because the HPBW values on the embedded element pattern evaluated in the infinite array scenario (**Figure 4-23 -a** and **Figure 4-23 -b**), which represents a good approximation of the one referred to the central element in the finite array structure, vary between two planes for both polarizations. The gain profile, that can be drawn on the radiation patterns of the array, shows that there are no blind gain spots at 28 GHz in the specific scan range. Due to the choice of the W_{cell} mentioned in the description of unit radiating cell (section 4.3.2), grating lobes appear in the $(-\frac{\pi}{2}, \frac{\pi}{2})$ visible space along elevation direction and their amplitude level is lower than 7 dB respect to the maximum of main lobe at 20° for both polarizations. Furthermore, the SSL values of the radiation patterns at 55° EL and 20° AZ decrease up to 10 dB.

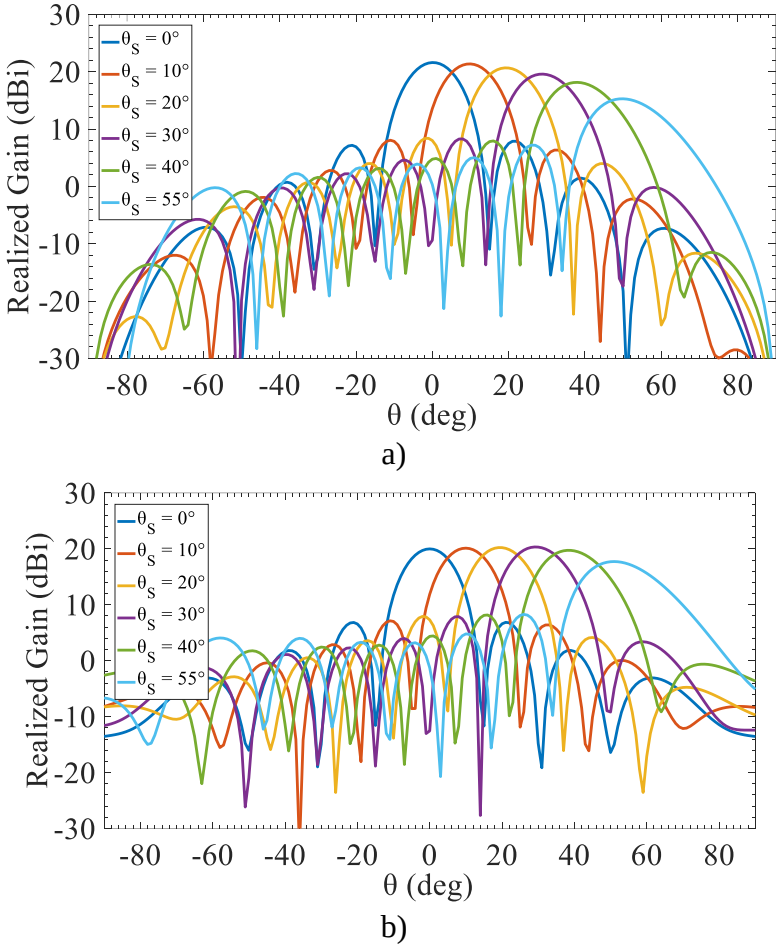
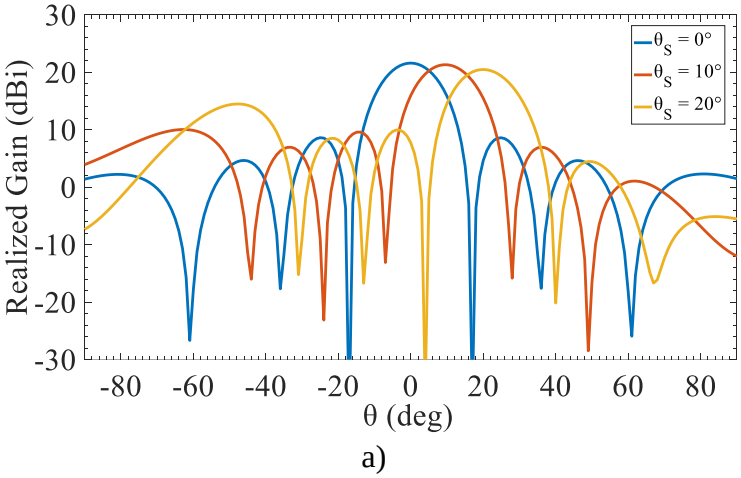
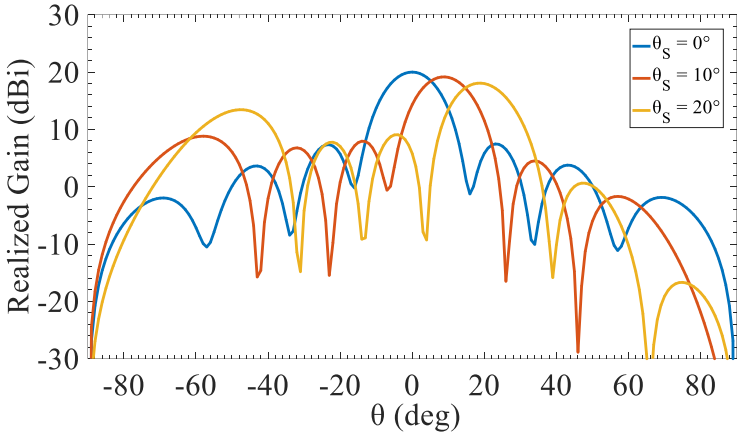


Figure 4-27: Array radiation patterns at 28 GHz when scanning in azimuth direction. a) H polarization; b) V polarization.





b)

Figure 4-28: Array radiation patterns at 28 GHz when scanning in the elevation direction. a) H polarization; b) V polarization.

Although a passive array prototype has been realized in this work, the measured embedded element patterns of a central element (marked in red) in **Figure 4-29** confirm that no scan blindness appears in the scan range along two planes. Therefore, no gain blind spots should be observed in the radiation patterns of the phased array when scanning the beam along both azimuth and elevation directions.

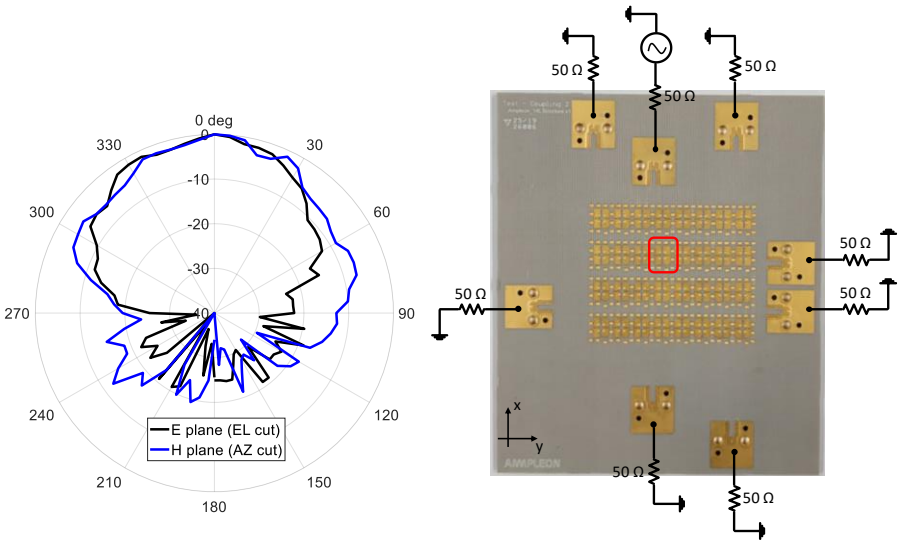


Figure 4-29: measured AEP of a central array element (only V polarization) while the rest is terminated on a 50 Ω load.

Simulated copolar gain plots across the frequency in boresight direction are shown for both polarizations in **Figure 4-30**. As it can be seen, the array gain at 28GHz is equal to 20 dBi for V polarization, while this value increases up to 21.6 dBi in the H polarization case. Globally, this value is greater than 18 dBi from 26.5 GHz to 29.5 GHz for each polarization according to the system requirements listed in **Table 4-1**.

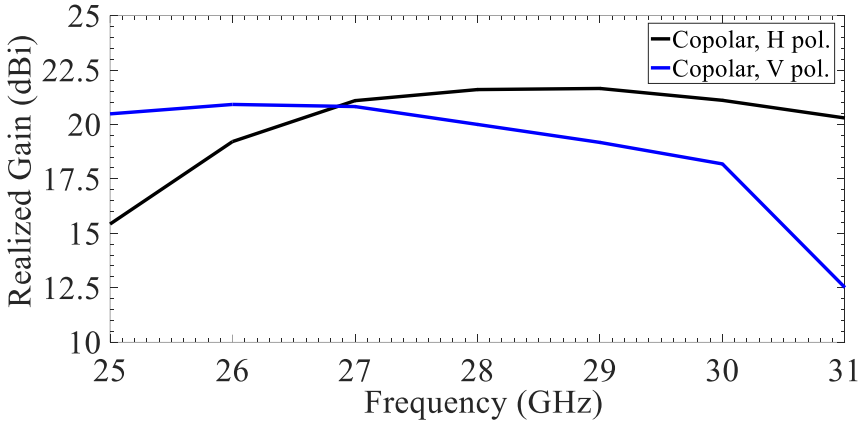
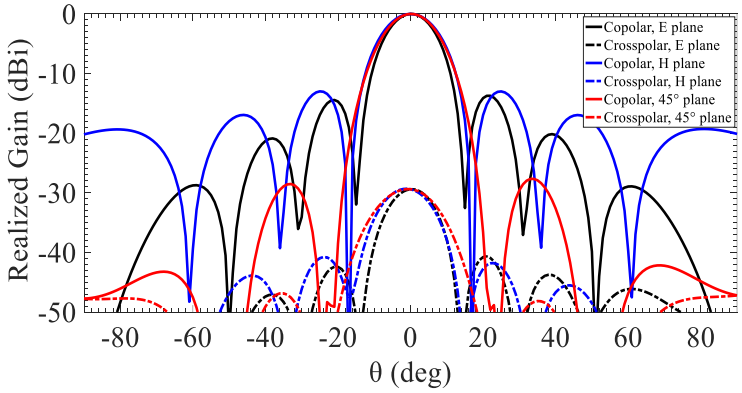
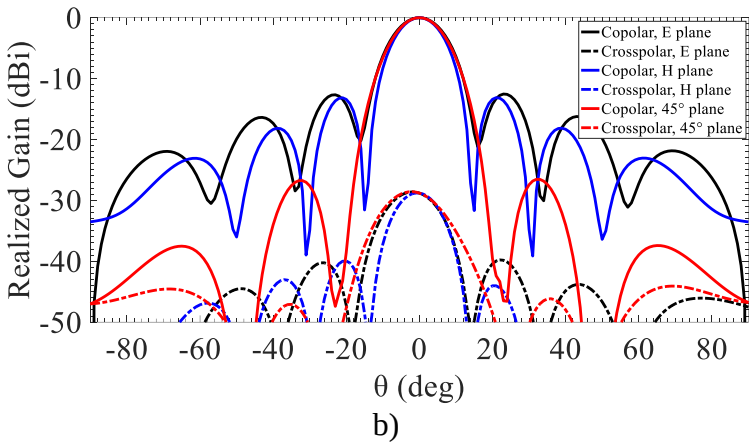


Figure 4-30: Simulated boresight array gain across frequency.

The boresight radiation patterns at 28 GHz reported in **Figure 4-31 -a** and **Figure 4-31 -b** for both polarizations show that the HPBW value is lower than 15° along all the radiation planes (E, H and 45° plane). This radiating structure also provides a side-lobe suppression higher than 12 dB along E and H planes, except for 45° planes where this value is much lower (i.e. SSL ≥ 25 dB).



a)



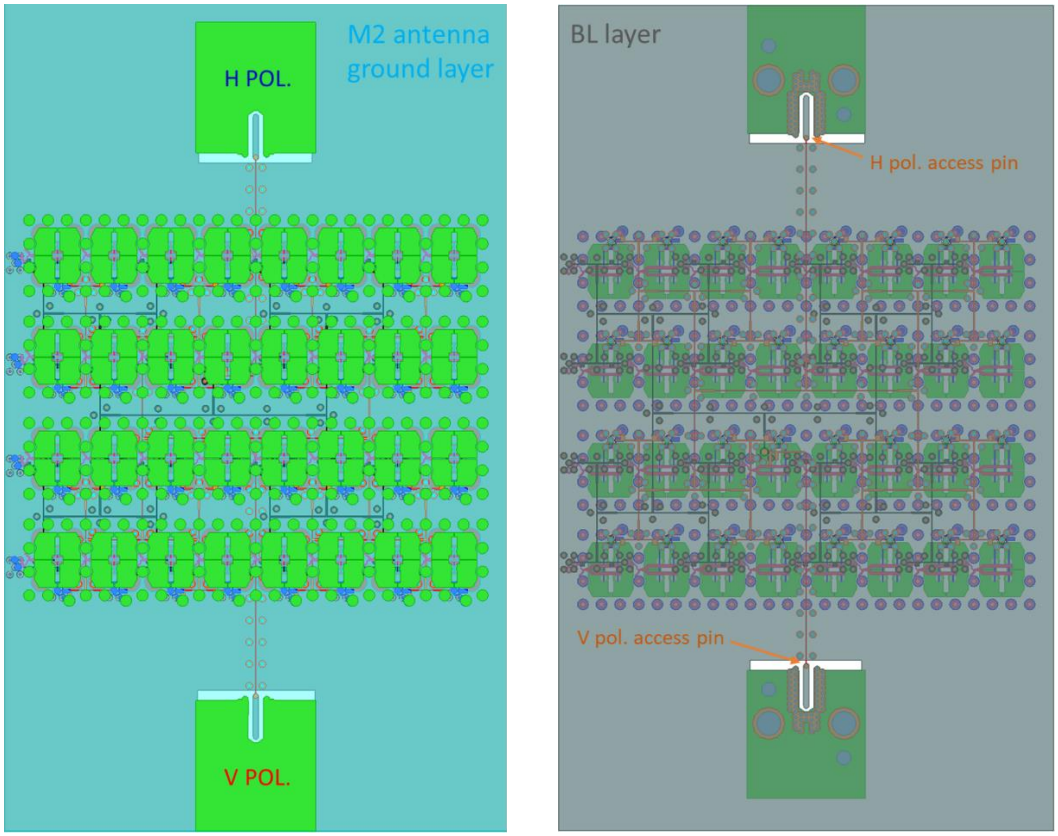
b)

Figure 4-31: Boresight radiation pattern at 28GHz. a) H polarization; b) V polarization.

4.5.3 Array prototype and measurements

As mentioned previously, a passive structure of the dual-polarized ME dipole array has been realized. In **Figure 4-32** is reported the complete layout of the array prototype that includes the footprints of two RPC-2.92 SMD connectors, which are mounted to have the access pins on the bottom layer of the stack-up. Although not clearly visible in the picture, the antenna ground layer with Jerusalem-shaped coupling slots are located on M2 layer (the light blue one), just like in the layout of the single ME dipole antenna. In this work, a stripline 1:32 power divider/combiner is used in the beam-forming (BFN) network to distribute, with the same phase difference, the signal coming from the connector towards the radiating elements of the array. In the beam-forming network for the H polarization shown in **Figure 4-33**, a 1:32 power divider/combiner is placed on M11 layer of the stack-up reported in **Figure 4-3**. Each branch of this component is connected to the input of the balanced stripline power divider located on M4 level by using M4 to M11 quasi-coaxial transitions. At this point, a single M11-M13 transition is used to connect a terminal of the long M13 stripline with the input of the power divider. The other terminal of the M13

stripline is connected to the CPW line on the bottom layer (**Figure 4-32 -b**) by an M13 to BL access via in the point *A*. Regarding the BFN network for the V polarization, the 1:32 stripline power divider/combiner has been located directly on M13 layer of the stack-up. Each arm of the latter is connected to the input of the balanced stripline power dividers, which are located on M3 level, by employing M3 to M13 quasi-coaxial transitions as indicated in **Figure 4-34**. In this case, the long M13 stripline is used to route the signal from point A' (i.e. input of the power divider/combiner) to point *A* thanks to the use of the aforementioned M13-BL access via.



a) b)

Figure 4-32: Layout of the array prototype. a) top view; b) bottom view.

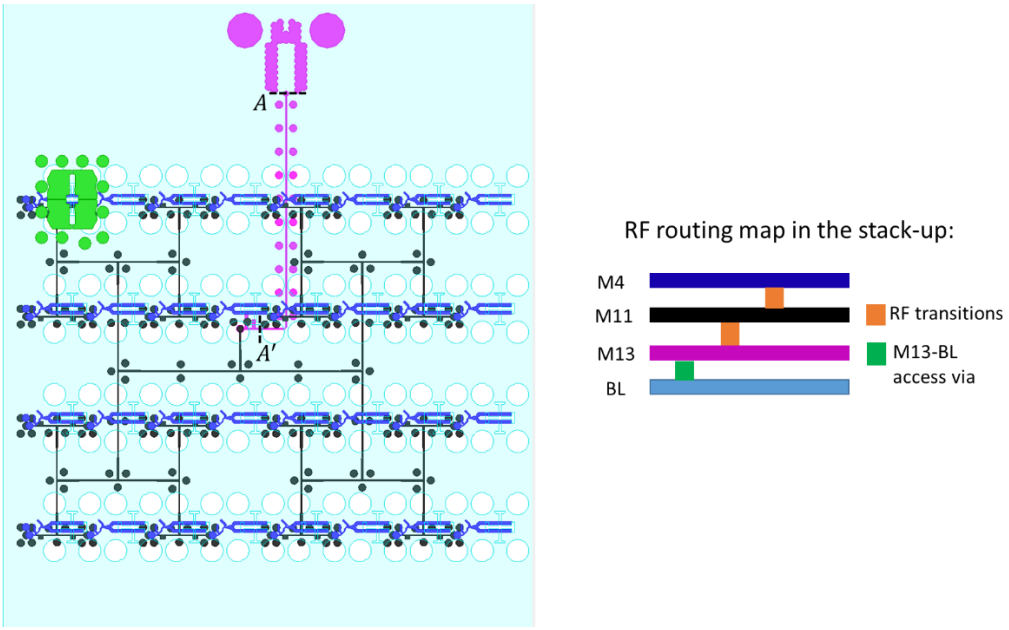


Figure 4-33: BFN network for H polarization.

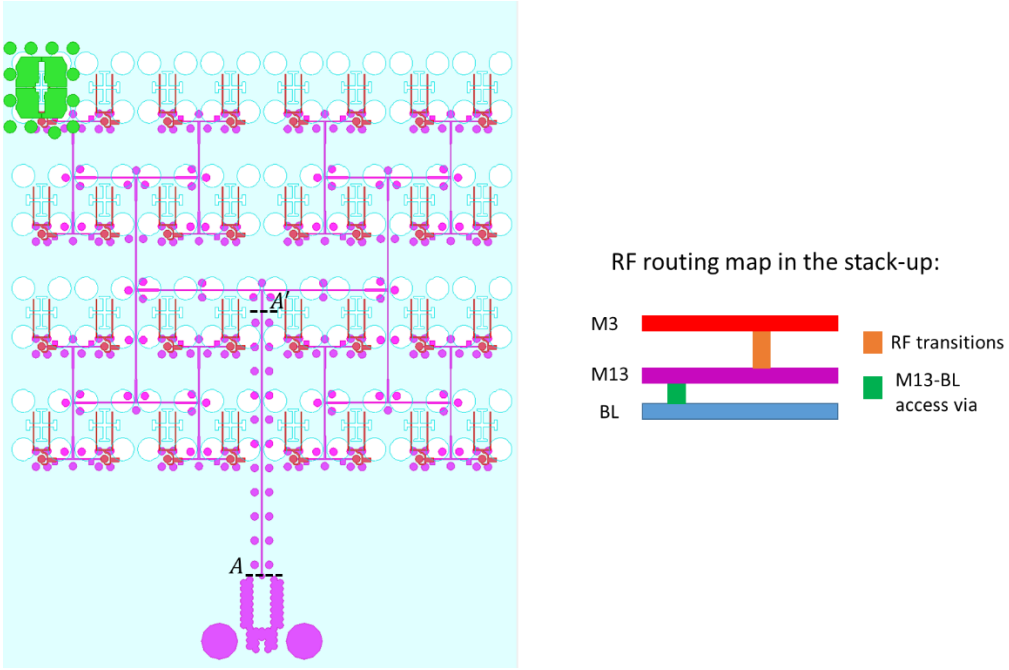


Figure 4-34: BFN network for V polarization.

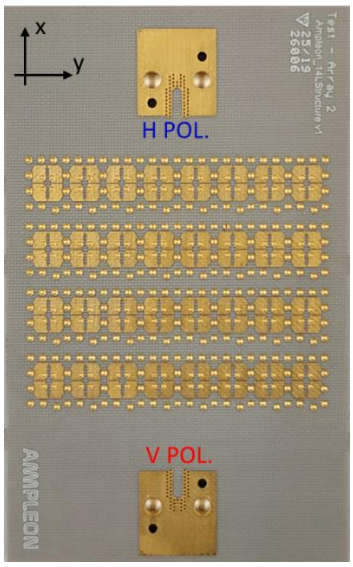


Figure 4-35: Top view of the passive array prototype (active area: 35.5 x 42.6 mm^2).

The realized prototype of the passive ME dipole array shown in **Figure 4-35** has been tested in the anechoic chamber considering the same setup used for the measurements of the single ME dipole (**Figure 4-18**). The normalized radiation patterns at 28 GHz shown in **Figure 4-31 -a** and **Figure 4-31 -b** have been compared with the measured ones at the same frequency on the polar diagrams in **Figure 4-36** and **Figure 4-37**. As it can be noticed, there is a good agreement between simulations and measurements along all the three radiation planes (E, H and 45°) for both polarizations. Some non-uniformities can only be observed between the amplitude of the radiation side lobes on all the radiation patterns.

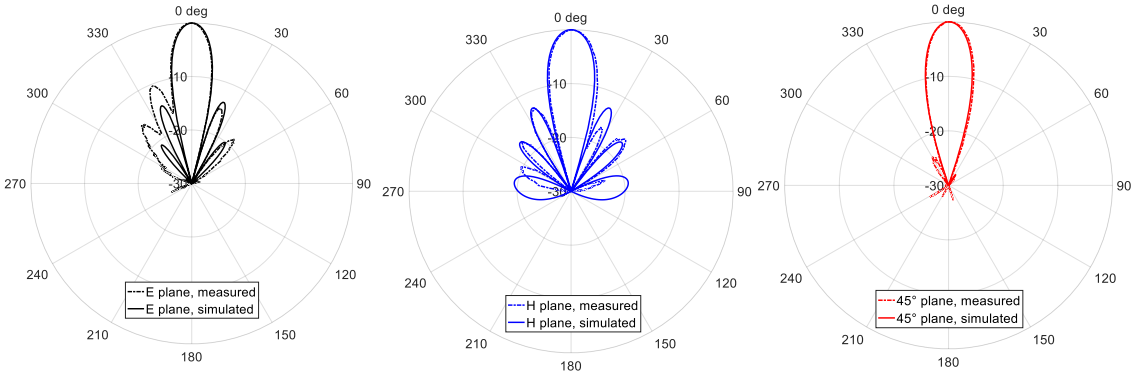


Figure 4-36: Comparison between radiation patterns at 28 GHz for H polarization.

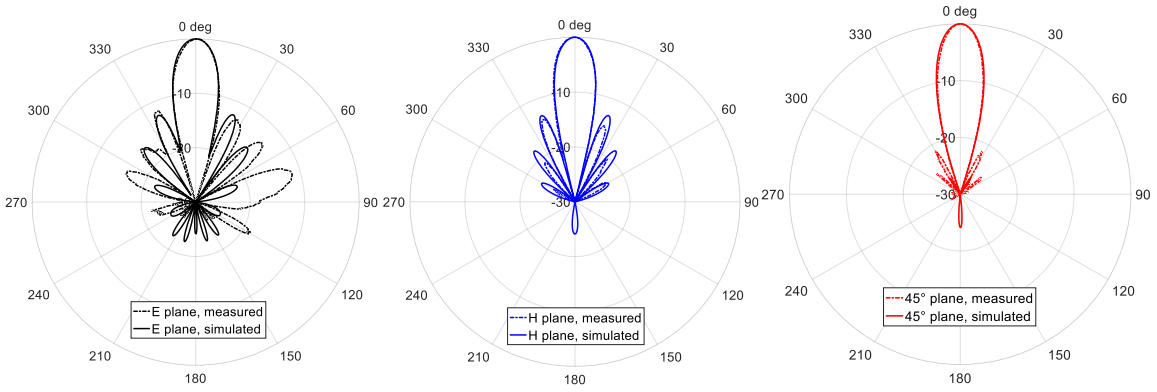
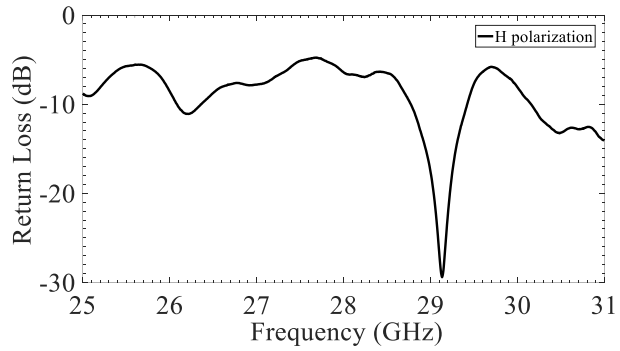
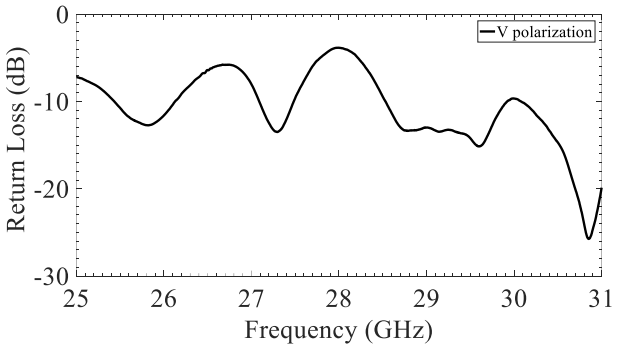


Figure 4-37: Comparison between radiation patterns at 28 GHz for V polarization.

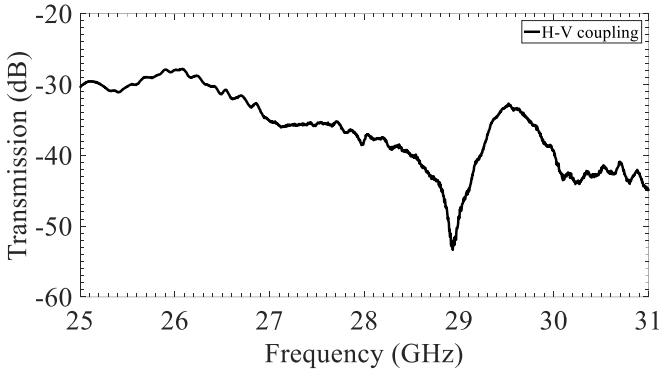
The measured S parameters of the passive array were plotted separately in **Figure 4-38 -a**, **Figure 4-38 -b** and **Figure 4-38 -c**. The impedance mismatch detected in the band of interest is because no TRL de-embedding procedure, used to mainly compensate the mismatch and losses introduced by the M13 stripline located between *A* and *A′* (see **Figure 4-33** and **Figure 4-34**), has been performed on the measured data yet. Therefore, the measured results were not compared with the simulated ones to avoid misunderstandings.



a)



b)



c)

Figure 4-38: Measured S parameters of the array. a) H polarization return loss; b) V polarization return loss; c) H-V coupling response.

5 Monolithically-integrated variable gain amplifiers for 5G transceivers

5.1 Introduction

The millimeter-wave spectrum is attracting great interest for the applications, such as 5G and satellite communications, respect to the traditional ones (e.g. military, scientific) in terms of investments, potential profits and technological challenges. The most attractive feature of mm-waves compared with the sub-6GHz band is the massive spectrum availability that leads a great advantage in terms of network capacity and data rate of the communication links. Other advantages of mm-wave systems are the compact size of the transceiver circuits and radiating structures, and an improved frequency reuse mechanism due to the high free-space attenuations [52][53]. On the other hand, this shift of frequency poses significant challenges to the systems design. Among building blocks in a wireless transmitter, one of the most critical components is the power amplifier (PA). This is

because one of the most important characteristics of a wireless transmitter is the Effective Isotropic Radiated Power (EIRP), which depends on the product of the antenna gain and the PA output power [53]. Although the total transmitter power can be incremented by combining several PAs, the output power (P_{out}) is still strictly related to the power density of the transistor technology adopted in the PA design [52]. For this reason, power density measured at the mm-wave frequency of interest is a crucial FoM about the technology comparison. The other key feature of a PA is its ability to amplify; thus, the gain of the transistors is another crucial FoM. This parameter is related to transistor characteristics, such as the transit or cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) whose values depend on both selected technology process and the transistor dimensions expressed respect to the emitter width (for bipolar devices) or gate length (for MOSFET devices). It is well known in the literature that as the scaling factor of a technology process increases, the f_t and f_{max} values grow up too [52]. This means that, for a fixed output power target, the transistor with better power density and lower capacitance value can be used for design of high frequency PA with good gain values because of greater maximum available gain (MAG) values [52]. Power efficiency and linearity, which are two other key parameters of the PA circuits, are mutually dependent. Basically, an amplifier with higher linearity will have a lower efficiency expressed as drain/collector efficiency and/or power added efficiency (PAE). Their tradeoff is usually optimized by some circuit-level solutions, such as Doherty PAs and/or outphasing PAs with digital pre-distortion (DPD) circuits [54][55], J-class and/or F/inverse-F PAs with multi-harmonic terminations [56] and some novel configurations as PAs with pMOS neutralization capacitors [57] and derivative superposition (DS) PAs [58][59]. However, if these parameters are considered separately, the linearity is deeply affected by the transistor characteristics, such as the variation of the

transconductance, the trapping phenomenon and the dynamic nonlinearities related to the presence of the parasitic components. At the same time, the efficiency is also dependent on some transistor characteristics, such as the ratio between drain bias and knee voltage. In light of the above, in **Figure 5-1** are reported the output power trends versus frequency obtained considering several published mm-wave PAs, which are extracted from the survey maintained at Georgia Tech [60]. The solid lines show that at Ka-band, for instance, the saturated output power arises from 20 – 27 dBm in the CMOS and/or BiCMOS PAs up to 35 – 45 dBm in the GaAs and/or GaN cases, thus confirming the superior performance in terms of power density over a broad frequency band of the III-V group technology processes (especially for GaN and GaAs) compared to the Si-based processes. Moreover, the first family overcomes the second one if the performance in terms of gain, efficiency and noise figure are taken into account for the PA design [52].

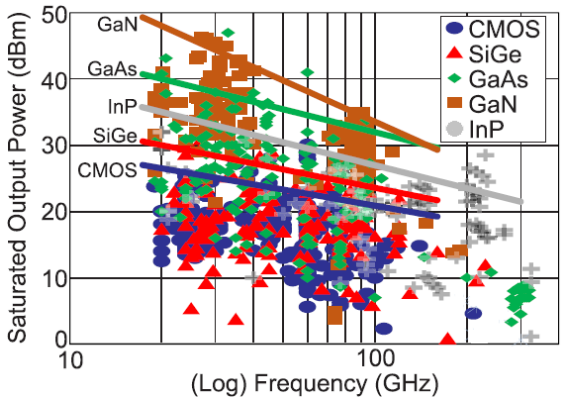


Figure 5-1: Survey of published PAs from K-band to over 300 GHz, extracted from [60].

Nowadays, with the increasing demand for smartphones to be used in future wireless networks (e.g. 5G), the III-V group technologies are achieving quite competitive production costs to meet the expected volume requirements of emerging mm-wave applications. On the other hand, Si-based PAs achieve lower output power levels compared

to the GaN-based or GaAs-based PAs counterpart, but they are unsurpassed in terms of cost (when mass-produced) and integration levels. Integration is, in fact, the main advantage of Si-based technologies. With up to ten metal levels in the back-end-of-line (BEOL) and the possibility to use, only for the BiCMOS technologies, bipolar and field-effect transistors on the same substrate, the capability of producing very complex heterogeneous circuits is outstanding. Moreover, the performance of passive elements such as inductors, capacitors in terms of losses or quality factors is quite competitive. Due to the latest advances in terms of process miniaturization, silicon technologies (CMOS and/or BiCMOS) are the right choice if high-frequency PAs to be designed. In this scenario, the technology nodes typically range from 250 nm with f_t around 220 GHz down to 90 nm with f_t of 300 GHz [52]. In conclusion, the selection of a Si-based technology can represent the right choice for the design of mm-wave PAs with medium/low output power levels.

Concerning the 5G systems, the latest services will use the portions of the mm-wave spectrum with the 5G new radio interfaces (5G-NR) [61]. Two distinct sets of bands have been designed in the frequency range 2 (FR2) of the 5G-NR (3GPP TS 38.101-2). The first one includes the n257, n258, and n261 bands (**Table 1-1**); if the total frequency band is used, it should include all the portions thus covering the 24-30 GHz portion corresponding to a 22% fractional bandwidth. In the highest part of the Ka spectrum, the n260 band, around 38.5 GHz, requiring an 8% fractional bandwidth. The biggest difference between 5G-NR and the previous radio technologies is related to the instantaneous bandwidths. In fact, the channel widths supported are, for FR2, up to 400 MHz per carrier, with the option of having the aggregation of multiple carriers at the base-station side thus achieving up to 1 GHz of channel bandwidth. Another key requirement of the transmitters is that PAs must operate in a more linear region to reduce the error vector magnitude (EVM) below 10% for

QAM constellations with M levels ≥ 64 on a large bandwidth. The 5G standard recommendations have specified that base-stations in the access networks should operate with EIRP values from 40 up to 75 dBm to guarantee data rate higher than 1Gbps with QAM modulation scheme up to 256 levels [13][24][25] in a coverage range of hundreds of meters. If the dimensions of the base station phased arrays is small and the beam-forming architecture is designed so that each radiating element is controlled by a single transceiver, the required transmit power at 1dB compression point for each chip should range from 10dBm up to 20dBm. For instance, the use of transceivers, which are usually realized in SiGe and CMOS technologies, with relatively low transmit powers (OP1dB =10-13 dBm) are suitable for phased-arrays with 64 to 128 elements that generate an EIRP of 55 dBm [13][25]. If very-large phased arrays are taken into account (i.e. $N \geq 256$ elements) and, thus, groups of many antennas (i.e. subarrays) will be fed by a single transceiver, the required output power of the PA should be $>$ 20 dBm for EIRP values up to 75 dBm. In this case, higher power technologies will be preferred, and GaN or GaAs could be regarded as the winning solution for the reasons listed above [25][52].

In the aforementioned 5G scenario, monolithically-integrated phased array transceivers use specific control algorithms to "shape" the patterns of the radiated beams depending on the network conditions. For instance, EIRP values of the mm-wave directional links established between MIMO base station (BS) and mobile users should be varied dynamically by changing the output power of the transmitter to reduce the mutual interference and, consequently, the bit error rate (BER) values and to optimize the power consumption of the TX circuit if the BS-user distance changes. Moreover, by applying an amplitude tapering function (e.g. Taylor, Chebyshev) on the array ports, it is possible to control the side lobe levels, thus reducing the inter-user and/or inter-cell interference. Variable Gain Amplifiers

(VGAs) and attenuators are the key components used in the phased array circuits to perform all these tasks (**Figure 5-2**). Also, they are employed in other systems or applications such as radar systems, test equipment, modulators [62]. The primary function of these circuits is to control the amplitude of the RF signal without ideally distorting its waveform [63]. From the literature, VGAs are circuits where the amplitude of RF signal is controlled by varying the bias voltages/currents or activating/deactivating amplification cells [64][65]. These circuits provide gain tunability on a broad control range, but they could suffer of large phase/amplitude variations and large DC power consumption. Depending on both system requirements and the use of some compensation circuits to reduce phase and amplitude variations, VGAs are often used as gain control elements in the phased array transceivers [64]. At the other hand, the attenuators are circuits where the amplitude of RF signal is controlled by activating/deactivating resistors by transistor switches or varying the resistance of transistor-based varistors [66][67]. From the phased array requirements perspective, attenuators could be more attractive compared to VGAs because of their higher linearity, wider bandwidth, lower temperature dependency, reduced control circuit complexity and easier compensation of phase imbalance [67][68]. A possible disadvantage of these structures is that they do not provide gain control by themselves, but only attenuation control.

Considering the beam amplitude shaping related to the phased array systems, the aim of this work is to design a 0.13um SiGe BiCMOS variable gain PA (VGA) operating in the 24-30 GHz 5G-NR band. This component should act directly as end-stage PA in a Si-based transmitter or as a driver circuit for a more powerful end-stage PA placed in an GaN/ GaAs analog front-end (AFE) circuit.

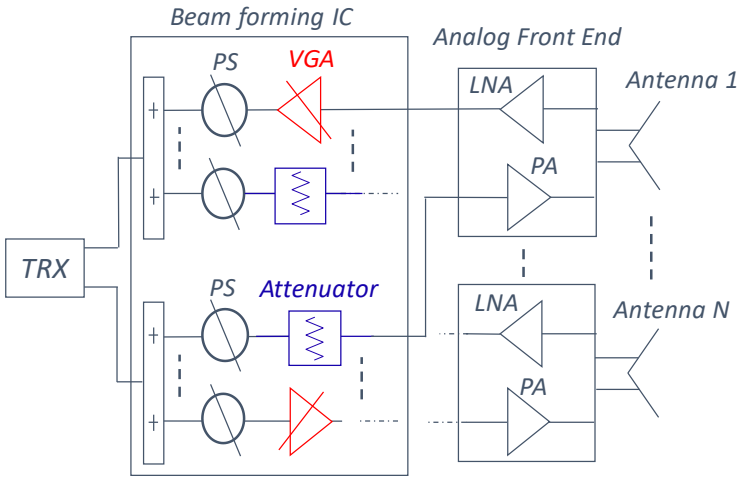


Figure 5-2: VGAs and attenuators as amplitude control blocks in phased array circuits.

5.2 State of the art on variable gain amplifiers

As explained previously, VGAs can be employed in the phased array systems to control both the EIRP of the wireless links and the side lobe levels of the array patterns by varying the amplitudes of the RF signals. Depending on the nature of the gain control mechanism, VGAs are classified into two groups, that are analog VGAs (AVGAs) and digital or step VGAs (DVGAs or SVGAs) [69]. In the first one (AVGA), the gain of the cell is controlled continuously by an analog voltage/current managed through DAC converters, while in the second one (DVGA) this parameter is changed by applying a specific digital word by external resistive/capacitive circuits or digital converters [69]. If wider gain control ranges are involved in the design, the resolution (or the number of bits) of the DVGAs should be augmented, thus leading to an increment of the occupied area comparing to AVGAs, which are generally more compact in size because of their intrinsic operating principle [69]. On the other hand, the digital VGA is preferred over AVGA circuit since it simplifies the interface with digital circuits and is less sensitive to noise in the DC control lines, mostly at higher frequencies [64]. Digital and analog VGA architectures can

be classified into four groups: transconductance-based VGAs, load-based VGAs, feedback-based VGAs and attenuator-based VGA [69] [70]. In the first family, the method used to change the amplifier gain A is to vary simply the transconductance value of the circuit (g_m). Basically, it is possible to modify the g_m values by varying the biasing values of the amplifier (as shown for a CS differential pair in **Figure 5-3**) by resistive/active current mirrors which can either activate / deactivate digitally the transistor cores of a digital VGA [65] or change continuously the biasing currents of an analog VGA [71]. Another solution, which can be only adopted in the digital structures, is to employ some switches to turn on /turn off the supply/biasing signals of the VGA stages, thus changing the total gain of the entire circuit [72][73].

$$A_v = g_{m1,2} \times R_L = \frac{2I_{tail}}{V_{GS} - V_t} \times R_L$$

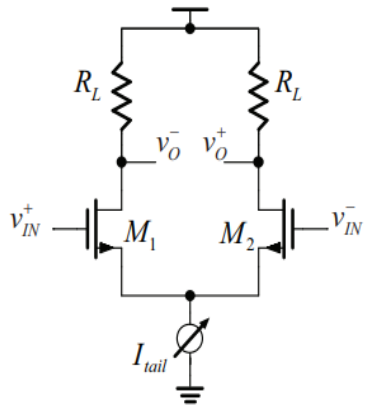


Figure 5-3: Example of CS differential circuit with a tunable current source (biasing is not shown).

The approach used in the second topology for adjusting circuit gain is to vary the load impedance R_L of a transistor amplifier [69] as depicted in **Figure 5-4 -a**. Several works found in literature employ this control mechanism, such as the well-known current steering/splitting method [64][70][74] where a control transistor acts as an additional

resistor to change the equivalent R_L value and, consequently, the amplifier output current by varying the voltage V_C (**Figure 5-4 -b**). Another circuit solution is to use switchable resistive load on differential amplifiers as reported in [75]. Although these architectures can achieve good performance in terms of phase imbalance, most of them have a gain-dependent bandwidth and, thus, these circuits could be not suitable for wideband applications.

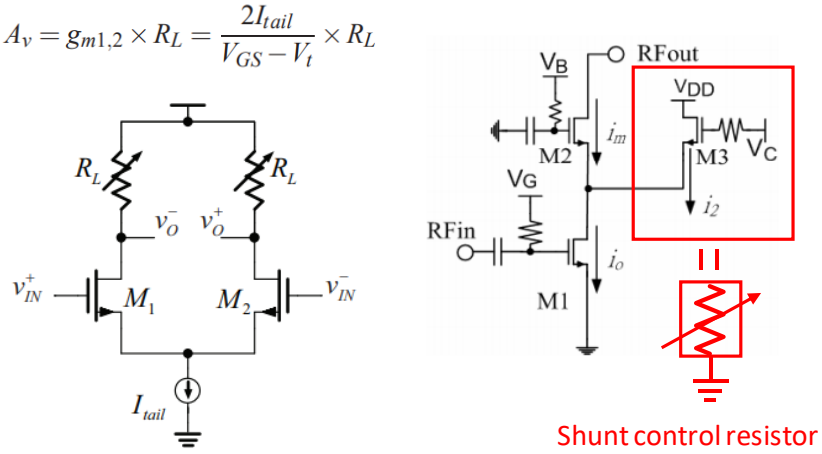
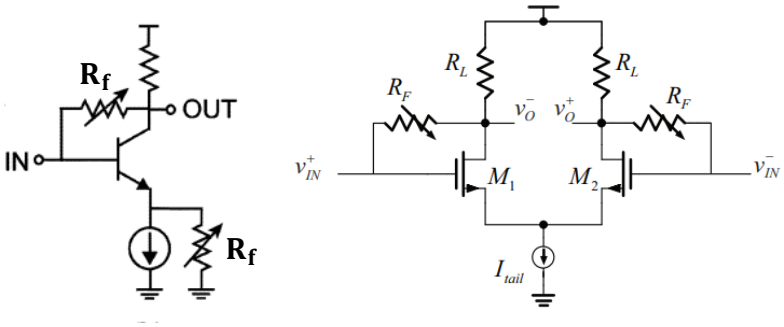


Figure 5-4: Load-based VGAs. a) simple circuit implementation [69]; b) example of current steering/splitting VGA [70].

In the third group, a resistor R_f employed to create a feedback network can regulate the gain of an amplifier if the feedback factor or resistance value is modified digitally, by using transistor-based switches, or continuously by exploiting transistor-based voltage-controlled resistors [69]. The feedback resistance in amplifier circuits is usually connected between the gate (or base) and drain (or collector) or between the source (or emitter) and the ground as depicted in **Figure 5-5** [64]. In the latter case, the degenerate resistor creates a negative feedback network, thus leading to an increment of both stability and phase imbalance [76].



a) b)

Figure 5-5: Example of feedback-based VGA. a) BJT-based circuit [64]; b) NMOS-based circuit [69].

In the last architecture shown in **Figure 5-6**, an attenuator circuit is used as the first block to vary the amplitude of the RF input signal and, consequently, the gain of the entire VGA circuit [77]. As mentioned in section 5.1, these control circuits usually exhibit good performance in terms of linearity, bandwidth, temperature dependency and energy efficiency. Therefore, the entire VGA circuit can take advantage from the latter to reduce the global power consumption and improve both linearity and bandwidth. In light of this, this VGA topology could be a potential candidate for 5G antenna array applications.

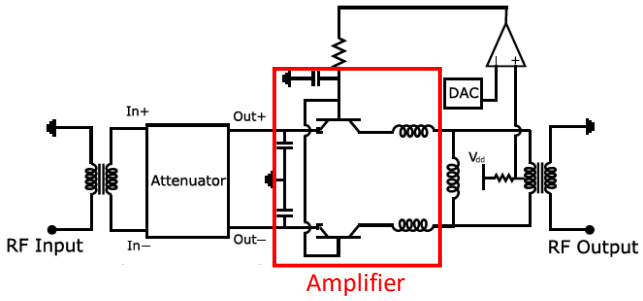


Figure 5-6: Example of attenuator-based VGA [77].

5.3 VGA requirements

As reported in section 5.1, the 5G mm-wave base stations should be able to work in multi-carrier aggregation mode to increase both the data rate per user and the network

capacity. Therefore, the PA circuits should cover all three designed bands in the 5G Ka spectrum, that is n257, n258 and n261, thus operating on the aggregate 24-30GHz band. Regarding the modulation quality or signal linearity, the 3GPP documentation (TS 38.104 version 15.2.0 [78]) indicates that EVM values of 64-QAM signals transmitted by 5G-NR base stations of type 1-C and 1-H should be lower than 8%, while this value drops below 3.5% if a 256-QAM constellation is employed. The efficiency (which can be express in terms of PAE or drain/collector efficiency) is another crucial parameter if power-efficient PAs are used in the base station transmitters in order to reduce the static power consumption and, consequently, the energy that must be dissipated out of the chips. CMOS/BiCMOS PA circuits, which are used in mm-wave low-power transceivers, show relatively high PAE around 30% or higher at 1dB compression point, but at the cost of poor linearity. Therefore, in the fifth-generation transceivers, it is necessary to relax the value of the efficiency to preserve the circuit linearity [13][79]. Considering the gain of the PAs employed in the 5G Ka-band transmitters, the peak values usually vary from 15 dB up to 25 dB while keeping good linearity performance of the entire array system [13][80][81]. Although a gain control range of 8-10 dB is enough to have a suppression of the side lobes up to 25 dB on the beam pattern [13][74], the most recent phased array systems could require a control range wider than 15 - 20 dB to further increase the channel amplitude selectivity and reduce the mutual interference between mobile users and base stations [79][80][82]. In light of this, the proposed VGA should satisfy the system requirements summarized in **Table 5-1**, focusing particular attention on the gain control capability, linearity and efficiency performance.

Table 5-1: VGA design requirements.

Parameters	Limits	Notes
Bandwidth	24 – 30 GHz	5G-NR aggregate bandwidth
Linearity	EVM < 3.5 % (up to 14 dBm)	256 QAM (5G-NR signal)
PAE	20% (@OP1dB = 16 dBm)	
OP1dB	16 dBm	
OP3dB	18 dBm	
Peak Gain	20 dB	
Gain range	30 dB	1dB tunability resolution
Gain flatness	0.5 dB (@ 1GHz of BW around f_0 = 27 GHz)	
Return loss	< 12 dB	

To accommodate the RF power requirements of the proposed circuit, a standard 0.13um SiGe BiCMOS MMIC technology from ST Microelectronics, namely BiCMOS9MW [83], has been employed in this work. The back-end-of-line (BEOL) of this process consists of six Cu-metal layers and an additional aluminum layer (ALUCAP) placed on the top of the stack-up which is mainly employed on the pads (**Figure 5-7**). The top metal layers M6T and M5T of the BEOL have a thickness of 3um, while the other layers, from M4B to M1, have smaller thicknesses. To increase both the quality factor Q and the power handling, transmission lines and inductors are designed in the last thick copper layers (M6T and M5T). In this case, it is possible to use the ALUCAP layer to further reduce the coil resistance because the equivalent thickness is increased. In this technology, metal-insulator-metal (MIM) capacitors are placed on the top of BEOL in a dielectric layer called PADOPEN. Regarding the active devices (**Figure 5-7**), this BiCMOS process includes two

families of NMOS and PMOS transistors, namely low leakage (LL) and high speed (HS), which can operate with two supply voltages equal to 1.2V (core) and 2.5V (IO), respectively [83]. High-speed SiGe heterojunction bipolar transistors (HBT) with f_t/f_{max} values up to 220GHz / 280GHz and two families of HBTs, denoted as medium voltage and high voltage, that have a collector-emitter (BVCEO) breakdown voltage of 7.5V and 13.5V, are embedded in the same silicon area. To optimize the performance of the proposed circuit in Ka-band, only high-speed NMOS and HBT transistors will be employed in this design.

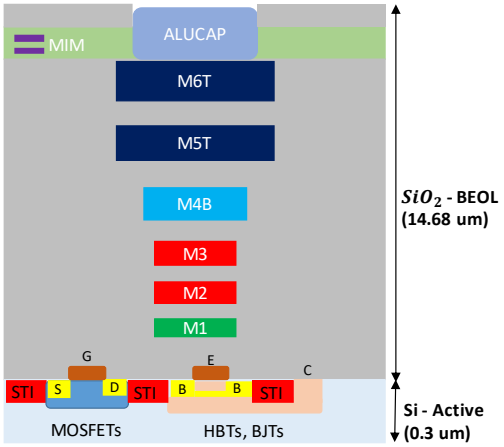


Figure 5-7: Stack-up of BiCMOS9MW technology.

5.4 VGA architecture

Considering the specifications indicated previously, the architecture reported in **Figure 5-8** has been chosen for the design of the VGA. It consists of a dual-stage amplifier whose gain is controlled continuously by a voltage variable attenuator (VVA) used as first block of the circuit. In this work, the design of the analog attenuator aims to minimize the occupied area and, thus, the number of DC control lines used to change the attenuation value, while maintaining good performance in terms of amplitude flatness, bandwidth and

power consumption on a wide control range. The dual-stage PA includes a differential end-stage unit that is connected to a single-ended driver cell. In the differential section, an on-chip balun transformer is employed to create both output matching network (OMNB) and inter-stage matching network (ISMB). The differential power combining brings several benefits such as an increment of 3dB in terms of P_{out}, an inherently high common-mode rejection ratio and, consequently, an increase of the circuit stability. Moreover, the intrinsic behavior of the balun transformer reduces significantly the power levels of the even-order harmonics thus increasing the circuit linearity [84][85]. The connection of the single-ended driver boosts the gain value of the entire dual-stage circuit thus relaxing the power capability of preceding stage [86][87].

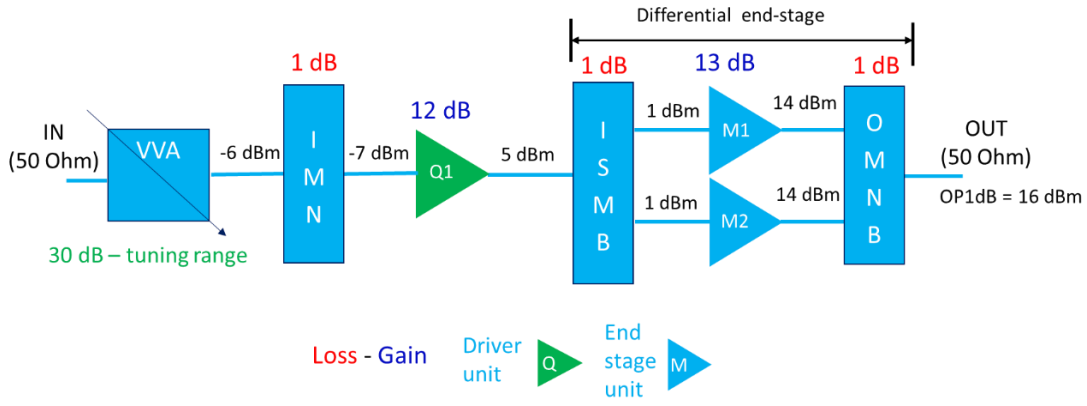
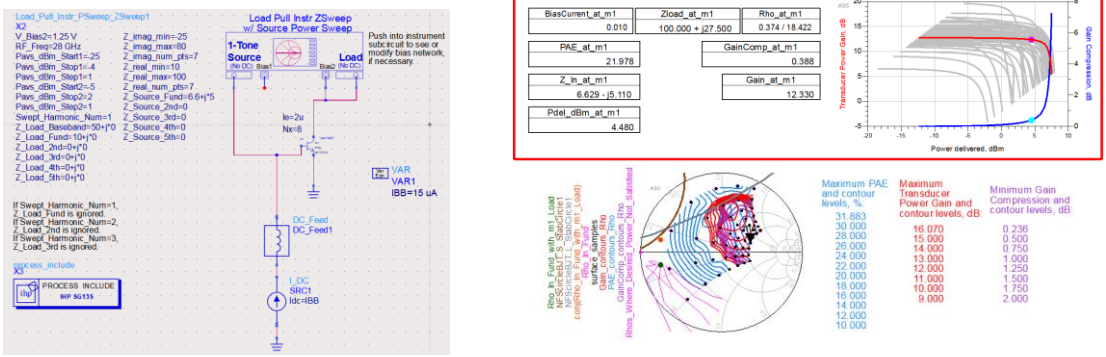


Figure 5-8: VGA architecture and circuit line-up.

The quiescent points were chosen so that both the end-stage unit and driver unit can operate in AB class. As it is well-known in the literature, this solution represents the right trade-off between output power, efficiency and linearity for power amplifiers operating in the mm-wave spectrum [86][88]. Concerning the selection of the circuit topology, the schematics of two conventional configurations, namely common emitter (CE) and common base (CB), have been simulated in Advanced Design System (ADS 2021 version) software

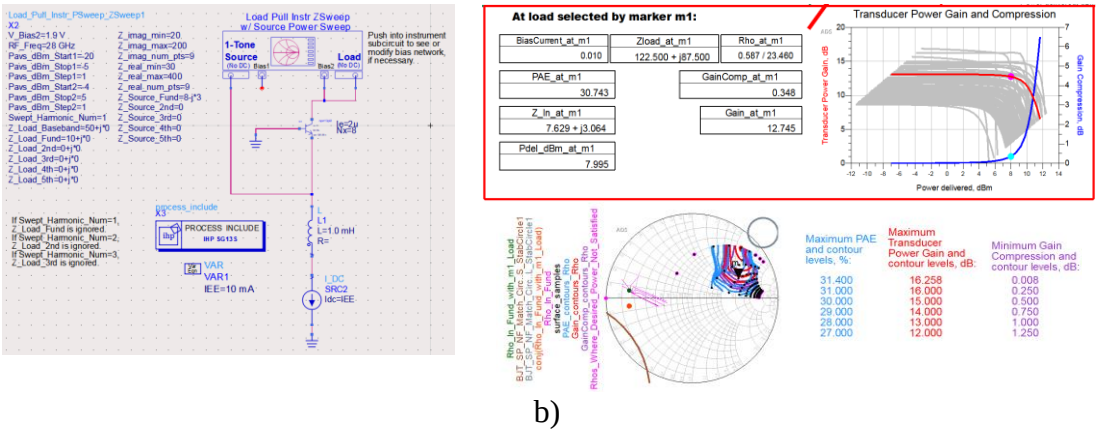
environment and their performance have been compared. In particular, the load-pull analysis was performed on both amplifiers operating in AB class and an optimal load has been selected (by marker M1) considering a gain compression value of $0.3 \div 0.4$ dB in a point where the power gains are similar as shown in **Figure 5-9 -a** and **Figure 5-9 -b**. The HBT transistors used in both configurations have dimensions $W_E \; x \; L_E \; x \; N$ equal to $0.12 \; x \; 2 \; x \; 8 \; um^2$ (where W_E = width emitter and L_E = length emitter) and they refer to a similar 0.13um BiCMOS process (SG13S technology from IHP Microelectronics [89]). The one-tone large signal performances obtained in the load-pull analysis (**Figure 5-9 -a** and **Figure 5-9 -b**) are reported in **Figure 5-10**. From these plots, it is worth noting that CB configuration has higher breakdown voltage and thus can use higher V_{dd}. In light of this, CB configuration outperforms the CE one in terms of output power at 1dB compression point and AM-PM linearity. Therefore, the CB configuration has been selected in this work as the most suitable topology for the implementation of both end-stage and driver units.

AB class Q point: $V_{bias2} = V_{dd} = 1.25V$
$I_{BBq} = 15 \; uA \rightarrow I_{CCq} = 20\%(Imax - Icutoff) = 9 \; mA$



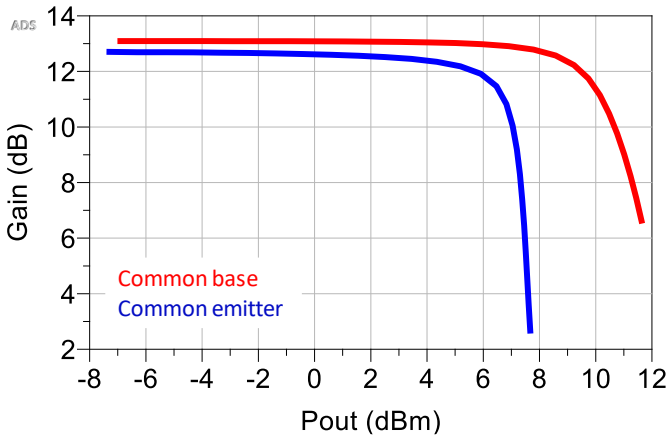
a)

AB class Q point: $V_{bias2} = V_{dd} = 1.9V$
$I_{CCq} = I_{EEq} = 20\%(Imax - Icutoff) = 10\ mA$

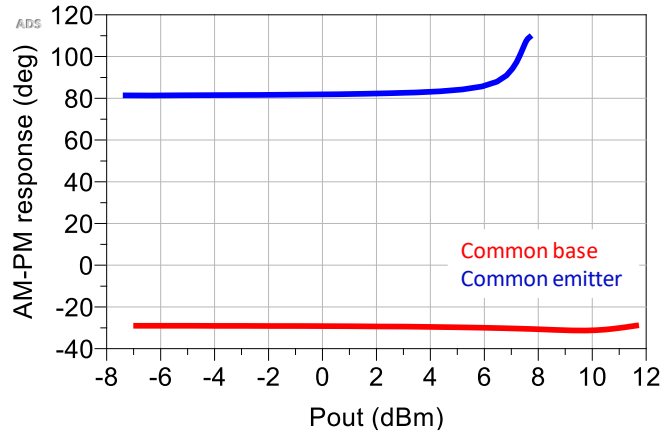


b)

Figure 5-9: Load pull analysis. a) AB-class CE circuit; b) AB-class CB circuit.



a)



b)

Figure 5-10: One-tone performance comparison at 28GHz. a) Gain vs Pout; b) AM-PM response vs Pout.

The description of the VGA building blocks in this thesis is organized as follows. At first, the design and simulation results of two different single-ended 50Ω-matched VVA structures will be presented in section 5.5. The entire TX-mode dual-stage PA, including the layout aspects and performance of each building block (i.e. amplifier cores, OMNB, ISMB, etc.), will be analyzed in section 5.6. Finally, the final schematic and the layout of the prototyped circuits (i.e. TX-mode dual-stage PA and the VGA circuit) will be reported in section 5.7, while the simulation results of both circuits will be reported in detail in section 5.8.

5.5 Ka-band Variable Voltage Attenuators

5.5.1 Introduction

As mentioned in section 5.1, variable gain amplifiers (VGAs) and analog/digital attenuators are one of the key components used in many communication systems and applications such as radar and cellular systems, test equipment, modulators, and phased array systems [62]. Due to the advances in MMIC technologies and their massive commercial use, monolithically-integrated attenuators and VGAs are demanded in the newer mm-wave array systems. These components must provide accurate tunability of the RF signal amplitude as required to control the radiation side lobes [62][67]. The use of attenuators and VGAs is particularly important for phased arrays to be employed in future mobile telecommunication systems, namely 5G systems. In these systems, especially in the Ka-band, each element of the array should be controlled both in amplitude and phase to reduce interferences between adjacent cells. VGA and attenuator requirements for such applications include high linearity and a wide dynamic range in view of its integration in

transceivers' core-chips. With respect to other applications, phased arrays require the signal amplitude of each radiating element to be controlled over a limited range, typically not higher than 15 dB, with a resolution of 1 dB [80]. On the other hand, the power consumption of these systems must be minimized to significantly increase both power efficiency and battery lifetime. For these applications, attenuators could be the best candidates because of their superior performance in terms of bandwidth, linearity and power consumption compared to the VGA counterpart [66][67][68]. In literature, most of the attenuator circuits rely on three basic topologies: T/Pi-type, T-bridge-type and switched-path [62][63]. These circuits can either be digital-based (also called switching or step attenuators) or analog-based (known as Voltage Variable Attenuators or VVA) [62][90]. Step attenuators typically outperform VVAs in terms of process/voltage/temperature (PVT) variations but they require a larger area especially when wider attenuation range requirements entail the use of a higher number of cells. On the other hand, VVAs exhibit smaller chip area and lower circuit complexity but they require a DAC circuit along the control path [62]. Typically, both analog and digital configurations rely on FET-based circuits to control the attenuation level. In step attenuators, FETs are employed in switches which enable or disable the different attenuation stages, while in VVAs they are used as varistors to continuously vary the channel resistances [66]. However, FET transistors have large parasitic source-to-drain and drain-to-substrate capacitances that could affect the performance of the attenuator in terms of insertion losses and power handling (IP1dB), especially at higher frequencies [91]. In the switches design, this drawback can be overcome by replacing the NMOS transistors with SiGe HBT transistors in Forward-Saturation (FS) mode [91]. As an alternative solution, switches can be also implemented using the Reverse-Saturated (RS) SiGe HBTs as their emitter capacitance is smaller than the collector capacitance in the forward-

saturation mode thus leading to a further decrease of the losses in the off-state without affecting its performance in terms of IP1dB [91]. The first example of 7-bit distributed step attenuator based on RS HBT transistors is reported in [68]. In this dissertation, a first example of single-stage hybrid Pi-type VVA using two shunt RS HBT varistors is proposed for 5G Ka-band antenna systems. In the following the performances of the proposed architecture are compared with the ones of a single-stage conventional NMOS Pi-type VVA. As it will be reported, results demonstrate an increase of 3 dB in the power handling capabilities and an improvement of 2 dB in terms of linearity (IIP3) of the hybrid VVA with respect to the FET-based configuration. For both circuits, the attenuation flatness is lower than 7.5 dB in all the Ka-band considering a wide attenuation range whose value is higher than 25dB.

5.5.2 Conventional NMOS Pi type VVA design

In order to validate the proposed hybrid approach, a conventional NMOS Pi-type VVA in ST BiCMOS9MW technology is first designed and taken as a reference (**Figure 5-11**). This topology includes a series NMOS-based varistor and two shunt NMOS-based varistors referred to as M_{S1} and M_{P2}, respectively.

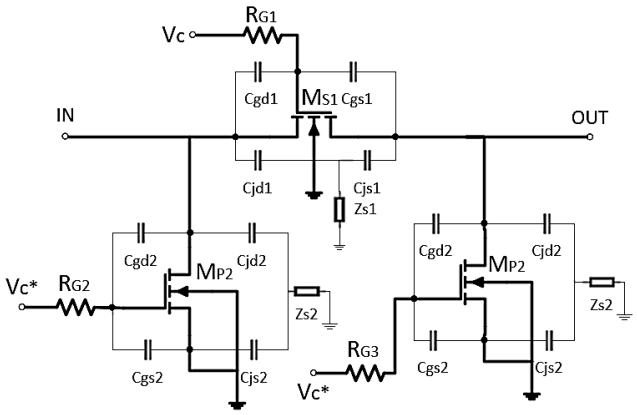


Figure 5-11: Conventional NMOS Pi-type VVA (the parasitic elements are included).

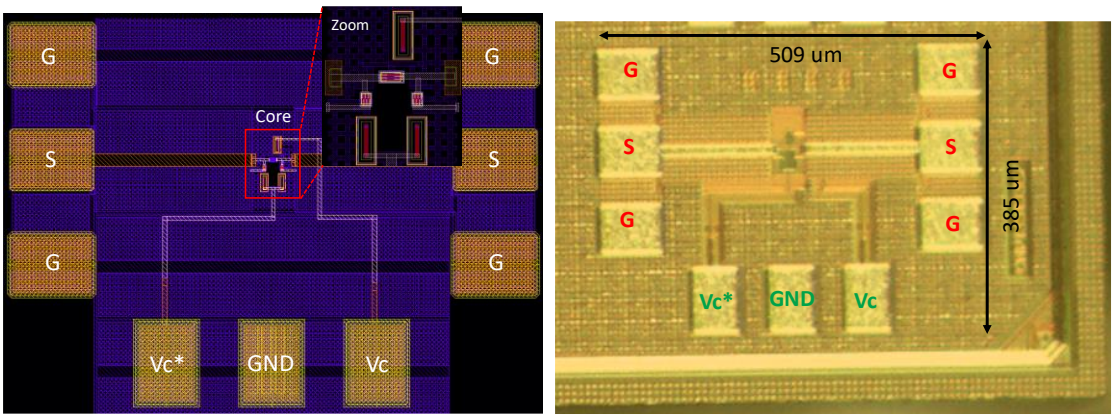
The minimum attenuation condition of the cell occurs when M_{S1} NMOS is turned on by high-value control voltage (V_c = 1 logic) and M_{P2} NMOSs are turned off by complementary control voltage (V_c^* = 0 logic). When the maximum attenuation condition is selected, the logic value of the control voltages is the opposite one [92]. As reported in **Figure 5-11**, these transistors can be modeled including some parasitic elements that affect the performance of the attenuator in terms of insertion loss, power and amplitude flatness [63]. The triode region of an NMOS transistor can be exploited so that the channel resistance R_{CH} can be varied by the gate voltage, V_{GS}, based on the following relationship:

$$R_{CH} = \frac{1 + \theta(V_{GS} - V_{th})}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th} - \eta V_{DS})} \qquad \textbf{Eq. 5-1}$$

where V_{th} represents the threshold voltage, $\frac{W}{L}$ is the NMOS aspect ratio while θ models the drain-to-source resistance, mobility variations and other short channel effects. The behavior of the drain current in the subthreshold region is modeled by the parameter η [66]. When V_{GS} exceeds the threshold V_{th}, the channel resistance value decreases until the gate voltage reaches its maximum value. If $V_{GS} < V_{th}$, the NMOS works in the cutoff area where the resistance tends asymptotically to its maximum value [92]. In the conventional VVA, two separate yet complementary gate control voltages, referred to as V_c and V_c^*, are typically used to dynamically change the channel resistance of both series and shunt NMOSs. Hence, the attenuation level of the VVA varies from the minimum to the maximum value and vice versa. The attenuation range depends on the aspect ratio of the transistors and the gate voltage swings of the NMOSs. In sight of this, the aspect ratio of the series MS1 is bigger than two shunt MP2 thus reducing the insertion loss (IL) at the minimum attenuation state.

To achieve a wider control range without scarifying the input/output matching level in the band of interest up to maximum attenuation state, the dimensions of shunt NMOSs were chosen to be as small as possible [63]. Therefore, the M_{S1} NMOS has a total width $W = W_{sngle\_finger} \times N_{finger}$ of 30 μm while the M_{P2} NMOSs have a total width of 15 μm (the finger number is set to 5 for all the transistors). The length for each high-speed transistor is set to the minimum value of the technology at hand, i.e. 0.13 μm. The gate terminal of each transistor is biased by a large resistors $R_{G1,2,3}$ equal to 10 kΩ to block the leakage of the RF signal through the control lines and oxide breakdown due to voltage fluctuations at the gate terminal [62].

In **Figure 5-12 -a** and **Figure 5-12 -b** are reported the layout and a microphotograph of the realized prototype, respectively. Input and output 50Ω GSG pads with 100 μm pitch are used for the RF measurements of the circuit. Two transmission lines placed on the M6T layer of the BEOL (**Figure 5-7**) are employed to drive the RF signals from pads to the VVA core. The control voltages V_c and V_c^*, applied through two DC pads, are employed to modify the channel resistance of the series/shunt transistors which in turn change the attenuation state of the VVA. The respective control lines are located on the M3 layer (the pink ones in **Figure 5-12 -a**) of the MMIC BEOL to avoid unintentional contacts with M6T RF transmission lines in the VVA core. The arrangement of series/shunt transistors, resistors, and DC control lines was conceived to reduce as much as possible the overall chip area. In fact, the overall circuit occupies an area of 508×385 um^2 while the core area of the attenuator (excluding pads and feeding lines) is 42×80 um^2 as shown in **Figure 5-12 -b**.



a) b)

Figure 5-12: Conventional NMOS Pi-type VVA. a) layout; b) IC microphotograph.

5.5.3 Hybrid Reverse-Saturated HBT Pi-type VVA design

The configuration reported in the previous section was taken as a reference to design the new VVA configuration. In particular, the proposed hybrid VVA is based on the use of reverse-saturated SiGe HBT transistors into the conventional Pi-type circuit. The theory behind the employment of reverse-saturated HBT transistors in the switches and attenuators design is treated in [68][91]. As mentioned in [68], the main constraint for utilizing CMOS transistors in switch design is the large parasitic junction diodes source-to-drain and source-to-substrate. The increased signal losses of the switch, due to finite substrate impedance of the shunt NMOS, lead to a decrease of the IP1dB. To overcome these issues and increase the power handling of the circuit, the shunt transistors can be replaced by SiGe HBT in a Forward-Saturation (FS) configuration where the emitter is connected to the ground. However, it is well-known that a shunt SiGe HBT in reverse saturation mode (RS) has improved off-state performance compared to a shunt FS SiGe HBT [91]. In this flipped transistor the RF signal flows into the emitter and the collector is connected to the ground. This configuration further improves the insertion loss performance of the switch for two

reasons. First, the emitter is physically well insulated from the conductive substrate thus resulting in smaller parasitic capacitances. Second, due to the higher doping concentration in the emitter and to the bandgap reduction in the base, the electrons have more difficulties to drift from the emitter to the base [91]. Since the energy gap in the conduction band is larger at the emitter than at the collector, the off-state impedance of RS HBT is larger compared to that one of the FS HBT. In order to prove the effectiveness of the RS HBT configuration with respect to the NMOS one taken as a reference, in the proposed hybrid VVA shown in **Figure 5-13** the series NMOS employed in both circuits has exactly the same size, while the shunt NMOS transistors of the conventional Pi-type VVA are replaced with two RS high-speed HBT transistors whose size is 0.27×6×1 um^2 (W_E×L_E× N_E). Since these elements act as varistors, the base terminals are biased by the same control voltage V_c^* (through big resistors $R_{G2,3}$ = 10kΩ) which is used to modify the resistance values in the triode region.

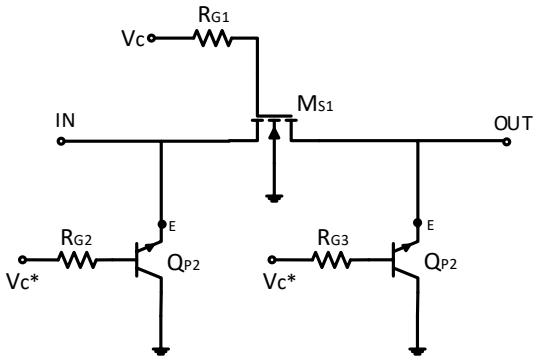
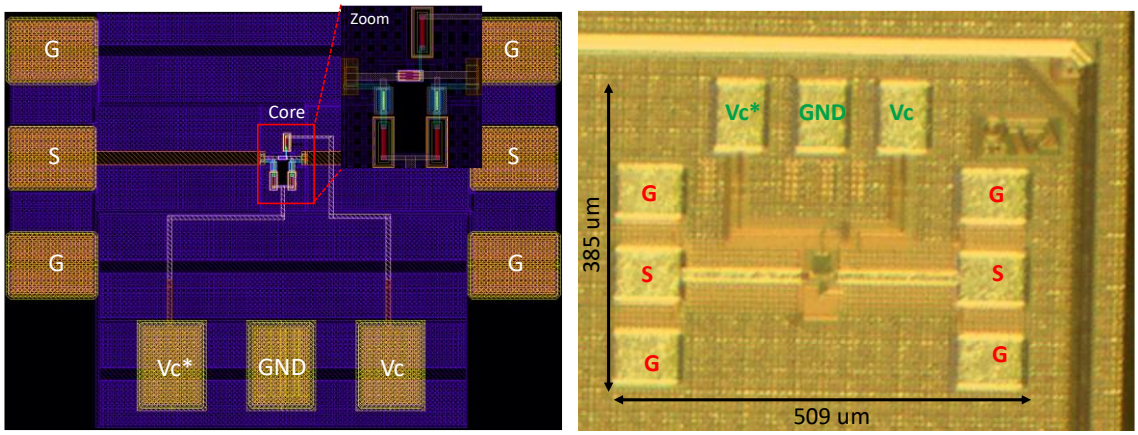


Figure 5-13: Hybrid RS HBT Pi-type VVA.

The same layout considerations regarding the RF GSG pads, RF/control lines arrangement in the MMIC stack-up reported for the conventional VVA are applied for the hybrid RS HBT VVA layout which is shown in **Figure 5-14 -a**. The entire hybrid circuit occupies the

same area as the conventional one (508×385 um^2) as well as the core area of the attenuator (42×80 um^2) as reported in **Figure 5-14 -b**.



a) b)

Figure 5-14: Hybrid RS HBT Pi-type VVA. a) layout; b) IC microphotograph.

5.5.4 Voltage variable attenuators results

The proposed structures have been validated using ADE-L schematic of Cadence software by taking into account the control parameters reported underneath. The control voltage for series NMOSs, V_c, is equal to $V_{cmax} - D_V$, where V_{cmax} = 1.2V, and D_V varies from 0 to 1.2V in steps of 50 mV. The control voltage V_c^*, whose value is initially set to 0V, is varied simultaneously following the complementary formula $V_c^* = 0 + D_V$. Given the reciprocity of the Pi-type topology, only the input return loss over frequency has been reported for both circuits in **Figure 5-15 -a** and **Figure 5-15 -b**. As it can be seen, this value is lower than 10 dB from DC to 40 GHz for all the attenuation states without employing any matching element such as $\frac{\lambda}{4}$ transmission lines or big inductors, thus reducing the occupied area of two circuits reported in **Figure 5-12** and **Figure 5-14**.

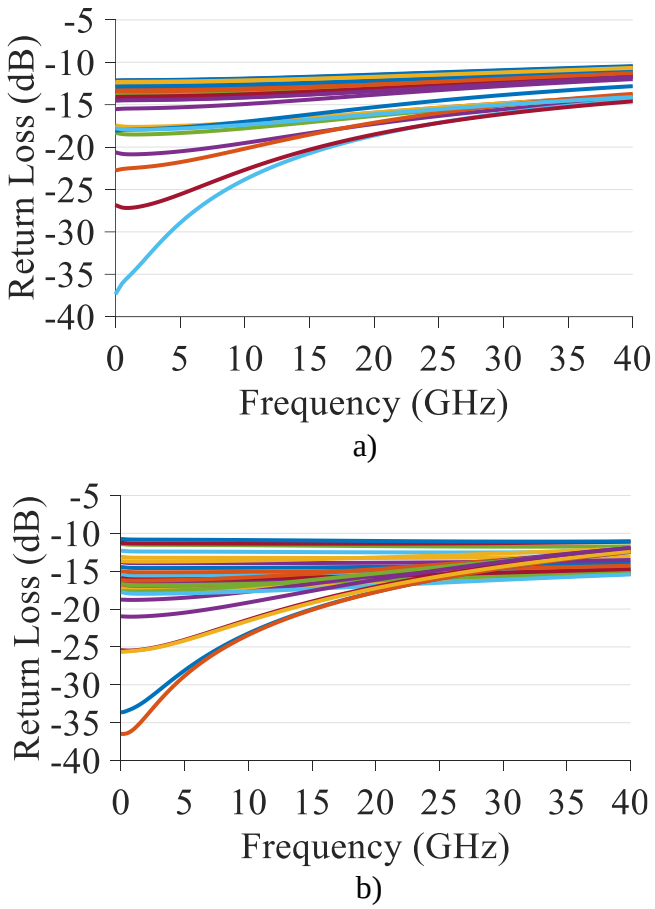


Figure 5-15: Simulated input return loss. a) conventional NMOS VVA; b) hybrid RS HBT VVA.

As depicted in **Figure 5-16 -a** and **Figure 5-16 -b**, both VVAs have similar performance in terms of attenuation response across the frequency band. At the center frequency (i.e. 27 GHz), the attenuation ranges for the reference and the proposed circuit are 31 and 27 dB, respectively. This small difference is because the area of two shunt HBT varistors equal to 1.62 μm^2 is smaller than the one of two shunt NMOS varistors that is 1.95 μm^2. This aspect makes the resistive ratio (or attenuation ratio) of the hybrid RS HBT Pi-type circuit smaller than the one of the conventional NMOS Pi-type circuit when it is evaluated at the maximum attenuation state [63].

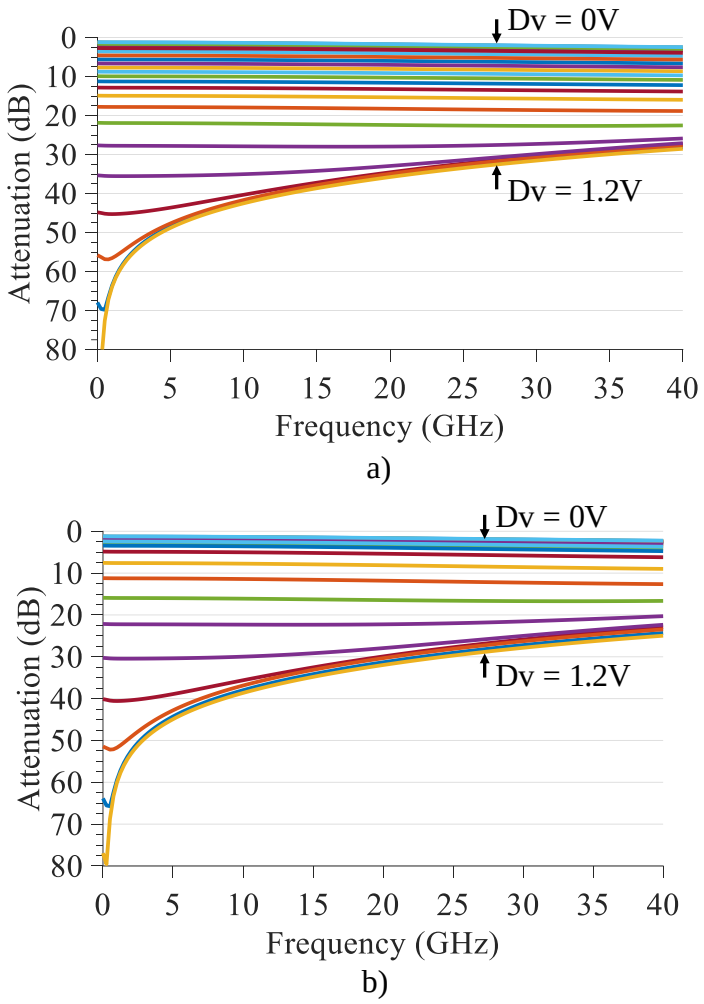


Figure 5-16: Simulated attenuation response: a) conventional NMOS VVA; b) hybrid RS HBT VVA.

The amplitude flatness, evaluated when the attenuation level is changed with a resolution D_V of 100 mV, is reported for both circuits in **Figure 5-17 -a** and **Figure 5-17 -b**. In the band of interest 24-30 GHz, both circuits exhibit an amplitude imbalance less than 1 dB until the attenuation state is evaluated for a D_V = 0.9V and lower than 2.5 dB at maximum attenuation state (D_V = 1.2V). If this analysis is performed in all the Ka-band, the amplitude deviation is greater than the previous case because of both the inherent behavior of the Pi-type attenuator and the high-frequency parasitic effects of the transistors that become

relevant mostly at higher attenuation states. Therefore, the maximum imbalance is lower than 7.5 dB at maximum attenuation state (D_V = 1.2V) for both circuits.

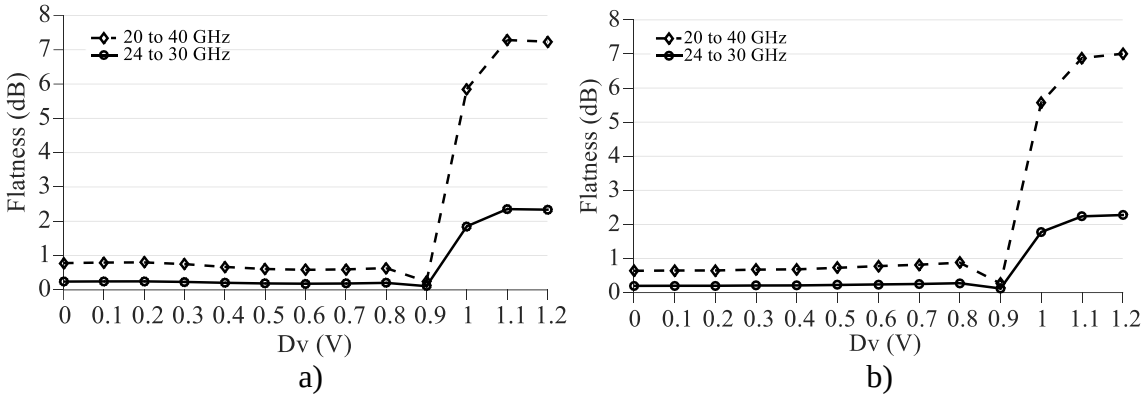


Figure 5-17: Simulated flatness across attenuation states: (a) conventional NMOS VVA; (b) hybrid RS HBT VVA.

One tone large-signal analysis was performed for the two proposed VVAs. **Figure 5-18** shows the simulated IP1dB vs. frequency at the minimum attenuation state for both circuits. As it can be seen, the values obtained for the hybrid RS HBT VVA are 3 dB higher than the ones of the conventional NMOS circuit over the entire frequency band. As expected, this is due to the higher off-state impedances and lower substrate losses distinctive of the shunt RS HBT transistors in the hybrid VVA with respect to the conventional configuration.

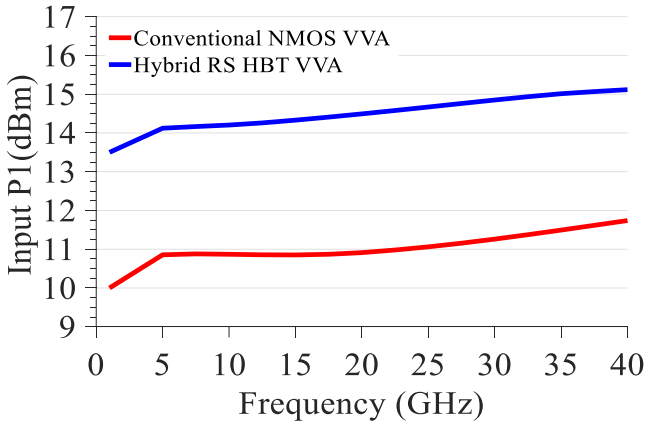


Figure 5-18: Input P1dB across frequency at minimum attenuation state.

Two tones analysis considering a carrier spacing of 10 MHz and an input power of -5dBm was performed for both VVA circuits at the minimum attenuation state. **Figure 5-19** reveals that the IIP3 values for the hybrid RS HBT VVAs are 2.2 dB higher than those of the conventional NMOS VVA, thus showing an improved linearity with respect to the reference case.

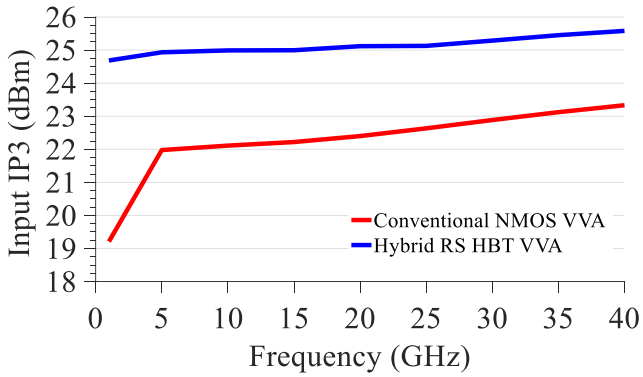


Figure 5-19: Input IP3 across frequency at minimum attenuation state.

The effectiveness of the hybrid configuration has not been validated experimentally as the two prototypes have not been measured by probe-station system yet.

5.6 Ka-band dual-stage power amplifier

The description of the dual-stage PA is organized in steps considering the architecture of the circuit reported in **Figure 5-8**. The design of the end-stage section which includes both the differential common-base (CB) HBT amplifier and the output matching network balun (OMNB) (**Figure 5-8**) will be presented at the beginning. The analysis of the driver section containing both the single-ended common-base (CB) HBT amplifier and the inter-stage matching network balun (ISMB) (**Figure 5-8**) and a description of the input section which incorporates the input matching network (IMN) will be shown at the end.

5.6.1 End-stage section

As mentioned in section 5.4, the selected circuit topology for the differential end-stage amplifier is the common-base (CB) configuration because of superior performance in terms of P_{out} and AM-PM linearity compared to the common-emitter (CE) configuration (as shown in **Figure 5-10**). Moreover, the end-stage PA should operate in AB class for the reasons indicated in section 5.4. The ideal schematic of the differential end-stage PA is depicted in **Figure 5-20**; the high-speed HBT transistors of the selected 0.13um BiCMOS process (ST BiCMOS9MW) have an area $W_E \times L_E \times N_E$ equal to 0.27 x 10 x 5 um^2. Both the biasing voltage $V_{bb} = 0.89V$ and the supply voltage $V_{cc} = 1.8V$ are applied to the circuit by ideal DC feeding network.

Load-pull analysis is performed on this circuit at the center frequency of 27 GHz to find the optimal impedance load. In particular, the load impedance $Z_{L\_diff} = 60 + j40\ \Omega$ was selected to achieve the gain target reported in the circuit line-up in **Figure 5-8** and to maximize the performance in terms of P_{out} and PAE. Regarding Z_{S_diff}, , its value equal to $3 - j1.5\ \Omega$ was chosen to realize the conjugate matching in the input section. As it can be seen by plots in **Figure 5-21**, the ideal end-stage differential PA fully satisfy the line-up requirements in terms of P_{out}, PAE and gain for the selected Z_{L_diff} and Z_{S_diff} impedance values.

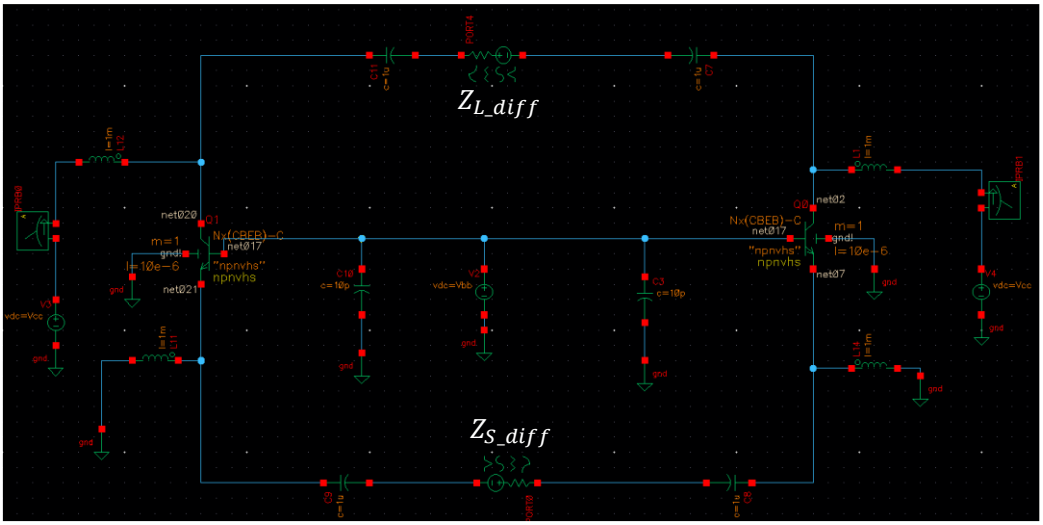
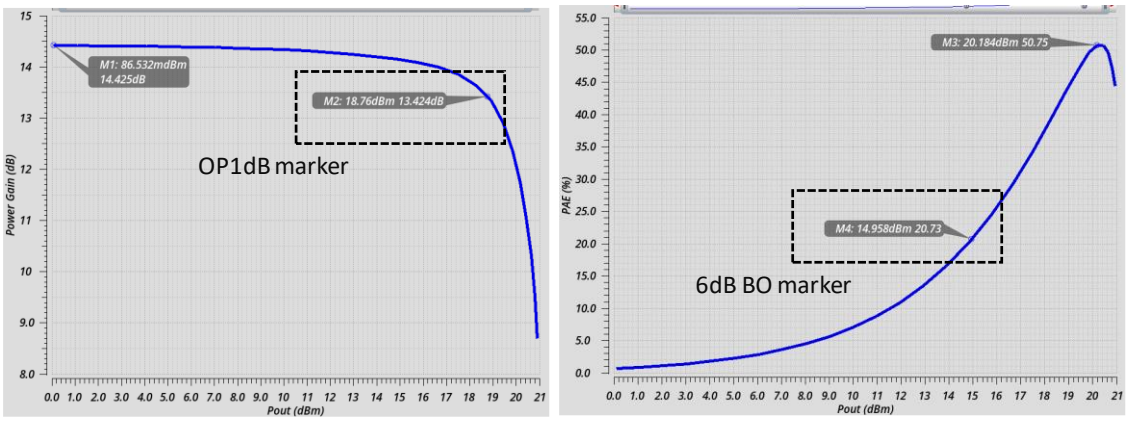


Figure 5-20: Ideal differential CB end-stage amplifier.

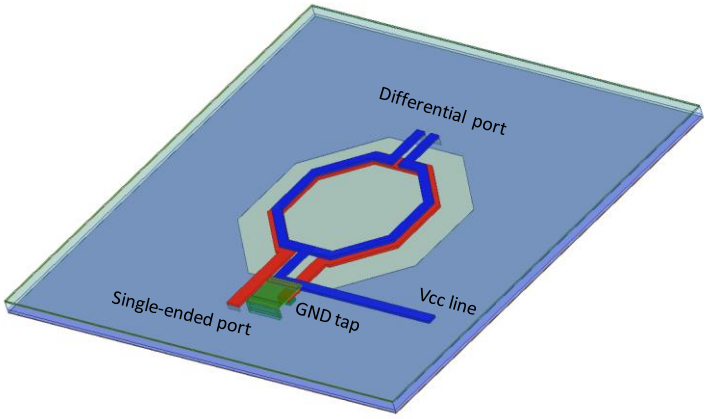


a) b)

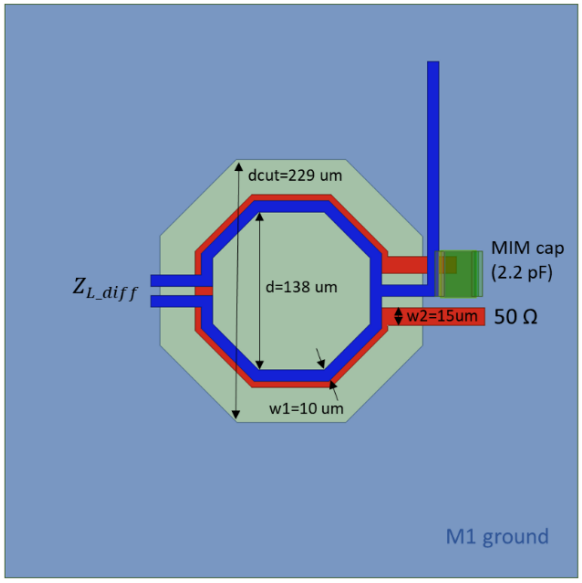
Figure 5-21: Large signal results at 27GHz. a) Power gain vs Pout; b) PAE vs Pout.

The OMN balun (OMNB) is used to combine the RF current signals coming from the collectors of the CB units to the single-ended 50 Ω output port. This component was designed in Ansys HFSS software environment and its layout is reported in **Figure 5-22**. It consists of two octagonal spirals, the differential one in blue is placed on the M6T layer of the BEOL (**Figure 5-7**), while the single-ended one in red is aligned vertically on the underlying M5T layer. By this arrangement, two stacked spirals generate the magnetic coupling mechanism while keeping smaller the occupied area of the transformer. The

diameter d of both spirals has been chosen to have a return loss below -10 dB in the band of interest 24-30 GHz and to avoid that the self-resonant frequency (SRF) is within the same band. The values of the widths w_1 and w_2 have been optimized directly by HFSS simulations to reduce the ohmic losses and to fine tune the inductance value of both spirals. The termination 2.2pF MIM capacitor (green one in **Figure 5-22**), which is connected between M6T and M1 ground, is used for a dual purpose: the first one is to reduce the spiral area of the inductors [93]; the second one is to decrease the amplitude imbalance between two ports on the differential side [94] and to increase the decoupling between RF signal and V_{cc} supply voltage because it acts as a RF filtering component. An octagonal cut has been realized on the M1 ground layer underneath the transformer (**Figure 5-22**) to reduce the losses due to the substrate eddy currents and increase the Q factor of the structure [94][95]. The balun was simulated both as a two-port device in differential mode, where the differential impedance is set to the end-stage PA impedance load Z_{L_diff}, and as a three-port device where the single-ended impedances on the differential side are equal to $\frac{Z_{L\_diff}}{2}$. As it can be seen from the plots in **Figure 5-23**, the insertion loss evaluated in differential mode is less than 1dB from 26 GHz to 30 GHz, while its maximum value of 1.18 dB is achieved at 24 GHz. From the results in **Figure 5-24** obtained considering the three-port device in single-ended mode, the amplitude imbalance is lower than 0.3 dB and the phase imbalance is lower than 6° in the band of interest (24 - 30) GHz.



a)



b)

Figure 5-22: Layout of the OMN balun. a) 3D view; b) top view.

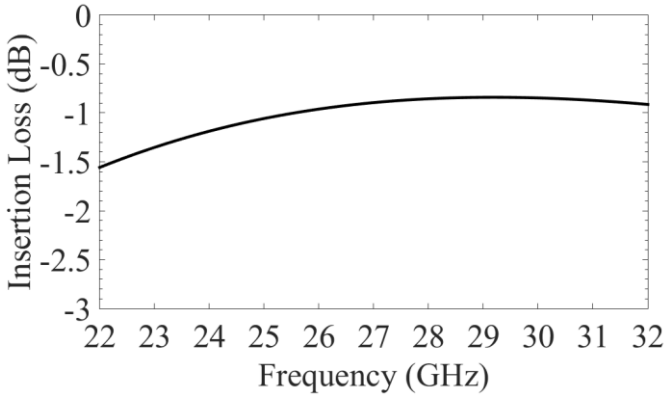


Figure 5-23: Insertion loss over frequency (two-port simulation).

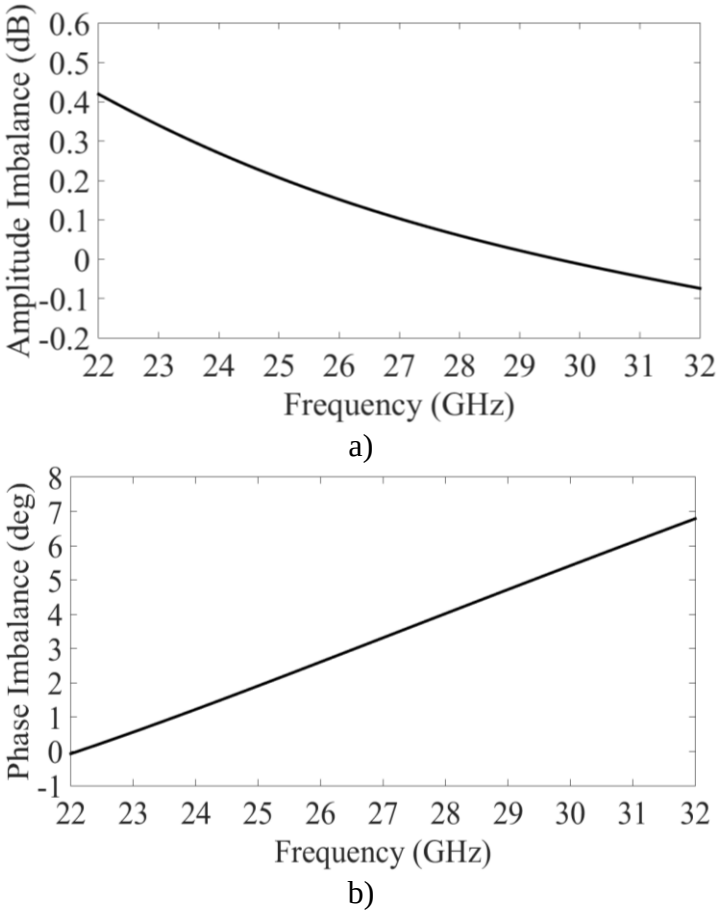


Figure 5-24: Three-port simulation. a) Amplitude Imbalance; b) Phase Imbalance.

In **Figure 5-25** is shown a portion of the final schematic that includes the end-stage section (OMNB + end-stage PA core) and the supply/biasing feeding networks. In addition to high-speed HBT transistors, only PDK passive components such as poly resistors, MIM and MOS capacitors, etc. are taken into account to make the simulations more accurate. Furthermore, the SnP blocks of OMN balun and 50Ω GSG output pad have been considered in the schematic. In the real case, the DC pads used for the supply (V_{cc}) and biasing (V_{bb}) voltages should be wire-bonded so that these signals can be applied from the outside of the chip. Therefore, in the final schematic, each wire-bonding connection is emulated by an inductance as depicted in **Figure 5-25**.

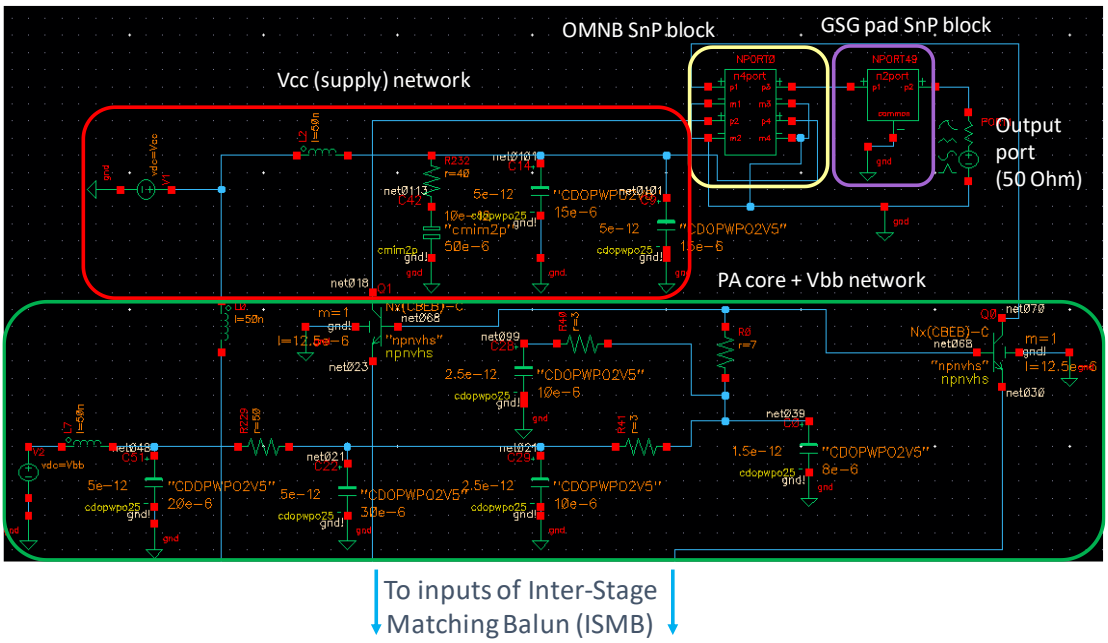
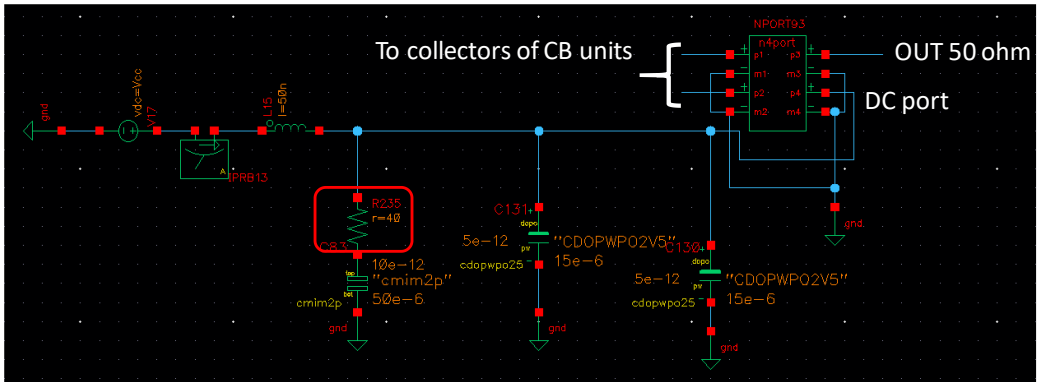
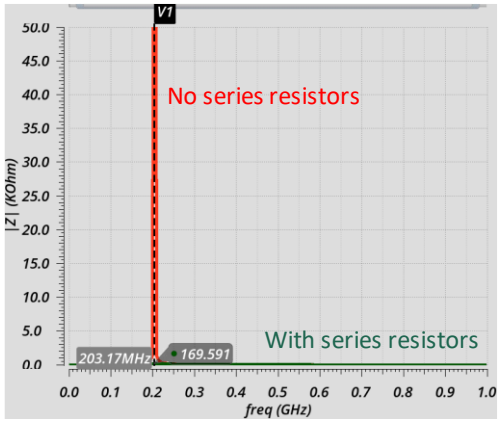


Figure 5-25: End-stage section of the dual-stage PA final schematic.

Some considerations were made regarding the design of the DC feeding networks for the end-stage differential amplifier. For instance, three shunt capacitors (total capacitance = 20 pF) were employed to increase the RF filtering capability of the V_{cc} feeding network depicted in **Figure 5-26 -a**. Two 5pF capacitors (namely, C130 and C131) were chosen as MOS capacitors, which are embedded in the active zone of the MMIC stack-up, to make both the design rule checking (DRC) and the tiling procedure on the PA layout easier. An inconvenience that could occur on the PA circuit is the presence of resonance effects at very low frequencies due to large time constants of the supply/biasing feeding networks (long-term memory effects) [96]. This causes a strong alteration of the 3rd-order intermodulation product (IMD3) of the PA and, thus, a reduction of the video-bandwidth. To attenuate the memory effect at very low frequencies (**Figure 5-26 -b**), a 40 Ω resistor (marked in red) is added in series with the 10 pF MIM capacitor of V_{cc} feeding network as reported in **Figure 5-26 -a**.



a)

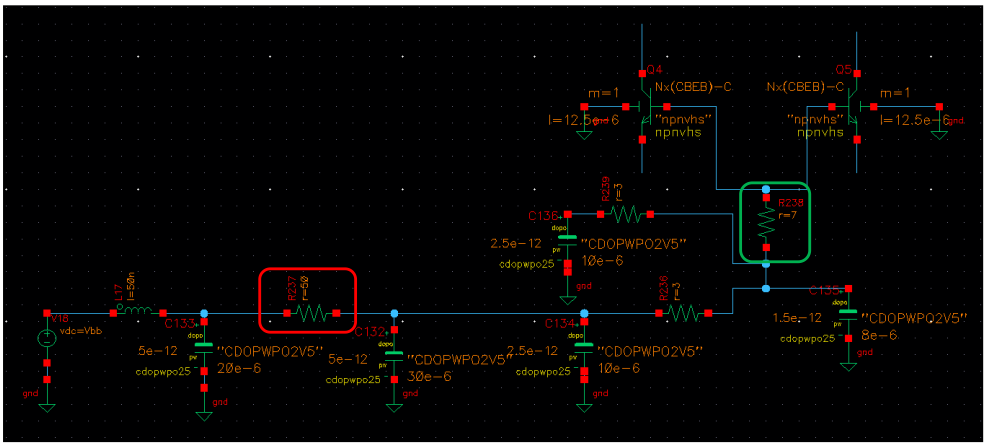


b)

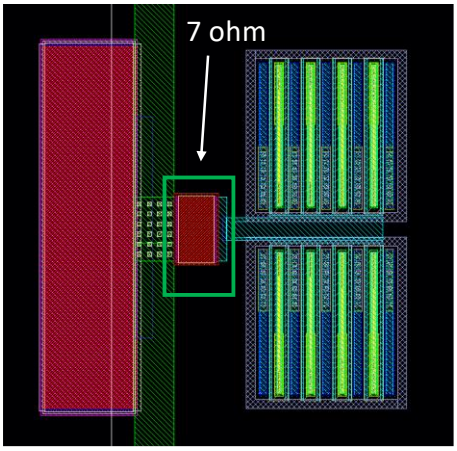
Figure 5-26: End-stage supply feeding network. a) circuit view; b) Memory-effect attenuation by adding a 40Ω resistor.

Similar to the supply (V_{cc}) network, the RF filtering capability of the biasing (V_{bb}) network in **Figure 5-27 -a** was improved by adding more shunt MOS capacitors in parallel for a total capacitance of 16.5 pF. In the end-stage PA core, two multi-finger HBTs are placed close to each other (**Figure 5-27 -b**) to reduce the inductive effect that could increase the PA instability. The form factor of these transistor has been changed with respect to the one used in the ideal circuit (**Figure 5-20**) but the equivalent area is the same (before: 0.27 x 10 x 5 um^2 = now: 0.27 x 12.5 x 4 um^2).Therefore, the actual large signal results remains unchanged as the ones in **Figure 5-21**.

A 7 Ω resistor has been added close to the base connection (**Figure 5-27 -b**) to further increase the stability condition and, consequently, the K factor of the circuit.



a)



b)

Figure 5-27: Biasing network in the end-stage section. a) circuit view. b) arrangement of the HBT transistors and connection of the base resistor (7 Ω).

The value of the resistor connected in series along V_{bb} line (marked in red in **Figure 5-27 -a**) was increased from 10Ω up to 50Ω to reduce the long-term memory effect of the feeding network and attenuate the impedance resonance seen at the input of V_{bb} network as shown in **Figure 5-28** without sacrificing too much the output power performance of the PA.

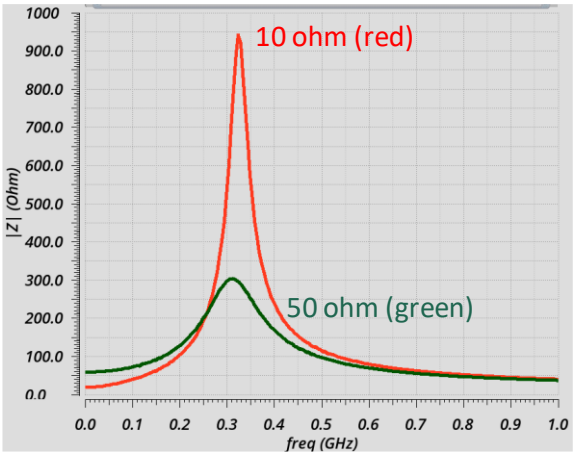


Figure 5-28: Memory-effect reduction by increasing the value of series resistance.

5.6.2 Driver and input sections

To boost the total gain of the PA circuit, a single-ended common-base driver has been designed. The ideal schematic of the PA driver is depicted in **Figure 5-29**; the high-speed HBT transistor has an area equal to half the one of the transistors used for PA end-stage (i.e. $W_E \times L_E \times N_E$ = 0.27 x 5 x 5 um^2) to avoid that the PA end-stage can operate in a higher power compression zone. The same biasing V_{bb} and the supply V_{cc} voltages equal to 0.89V and 1.8V are used in the PA driver to operate in AB class. The load-pull analysis is performed on this circuit at the center frequency of 27 GHz to find the optimal impedance load. In particular, the load impedance Z_L = 50+j20 Ω was selected to achieve the gain target reported in the circuit line-up in **Figure 5-8** and to maximize the performance in terms of P_{out} and PAE. Regarding Z_S, its value equal to 3-j2 Ω was chosen to realize the conjugate matching in the input section. As it can be observed in **Figure 5-30**, the ideal end-stage differential PA fully satisfy the line-up requirements in terms of P_{out} and gain of single CB unit.

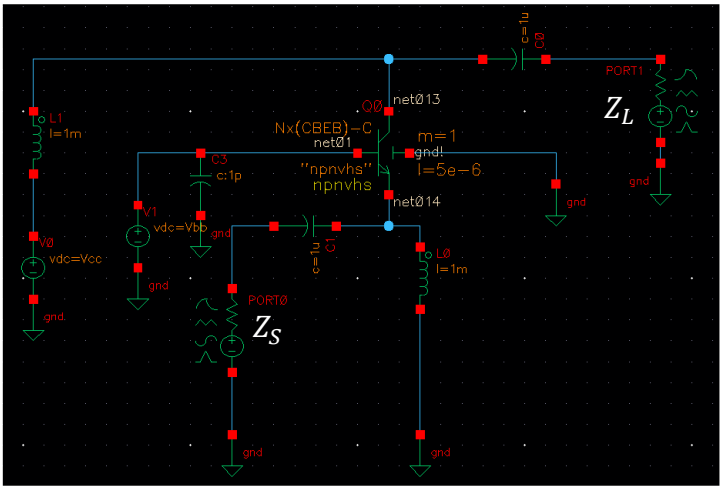
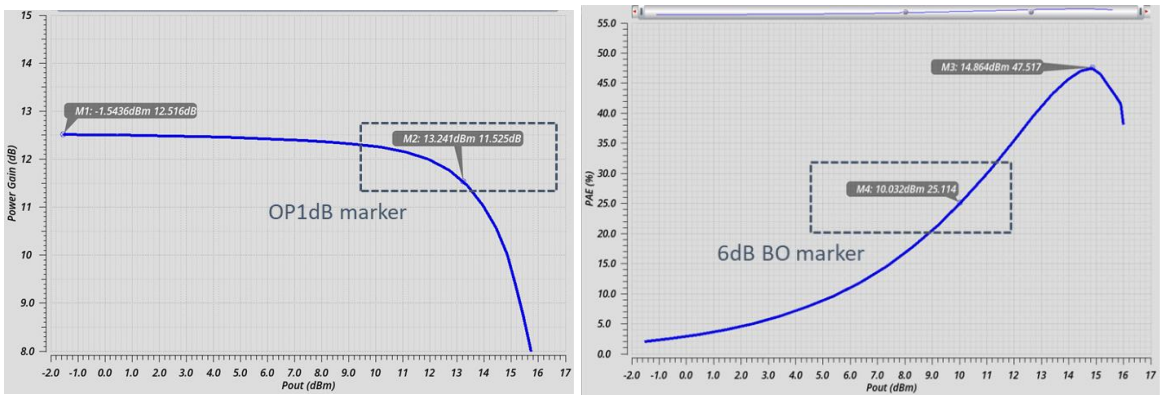


Figure 5-29: Driver common-base amplifier circuit.

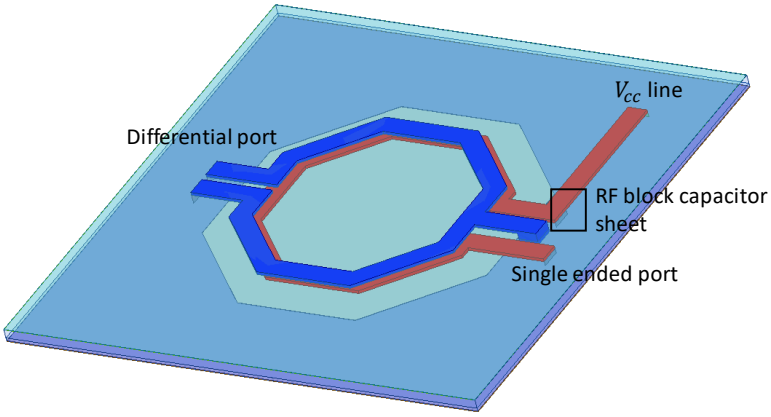


a) b)

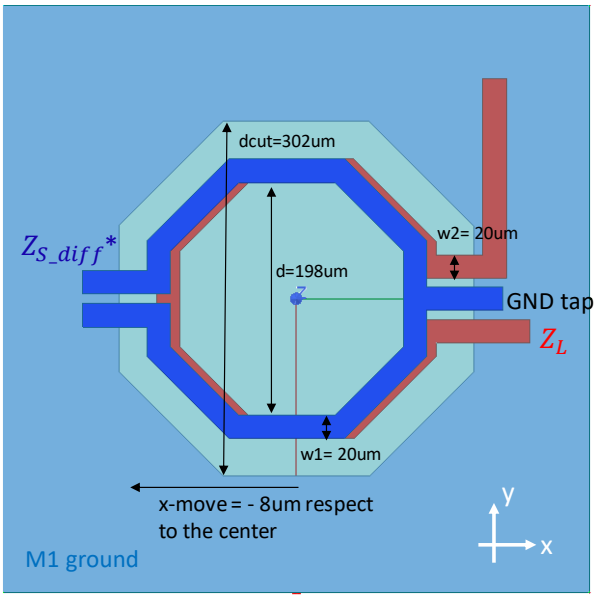
Figure 5-30: Large signal results at 27GHz. a) power gain vs Pout; b) PAE vs Pout.

To connect the single-ended output of the PA driver to the differential input of the PA end-stage, an inter-stage matching balun (ISMB) is employed in the PA circuit. Since this component is used to transform the driver load impedance $Z_L = 50 + j20\Omega$ to the differential end-stage input impedance $Z_S^* = 3 - \mathrm{j}1.5\Omega$, the impedance ratio or transformation ratio is higher than the one of OMN balun. To simplify the layout process and reduce the design efforts, a single-turn balun transformer, whose HFSS layout is reported in **Figure 5-31**, is used as an alternative to the multi-turn configuration. Similar to the OMN balun in **Figure 5-22**, the inter-stage balun consists of two octagonal spirals, the

differential one in blue is placed on the M6T layer of the BEOL (**Figure 5-7**), while the single-ended one in red is aligned vertically on the underlying M5T layer. The differential inductor with GND tap is used to close to the M1 ground the DC emitter currents of the end-stage common-base units, without using additional inductors as was done in the ideal circuit in **Figure 5-20**.



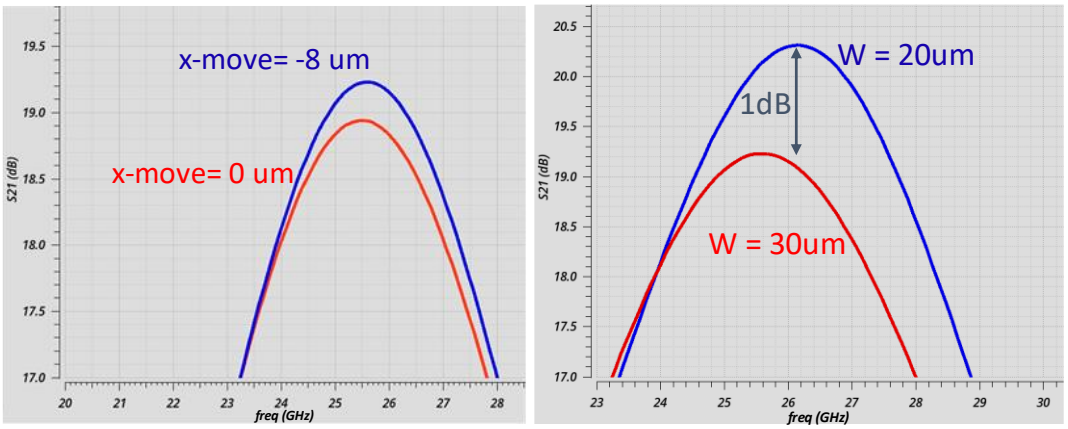
a)



b)

Figure 5-31: HFSS layout of ISM balun. a) 3D view; b) top view.

An RF block capacitor, which is emulated by a capacitive sheet of value equal to 21pF in the HFSS model, acts as a virtual ground in Ka-band for the single-ended spiral (the red one in **Figure 5-31 -a**). Furthermore, this capacitance is employed to enforce the RF filtering capability of the V_{cc} feeding line. The shift along x-axis of the differential spiral out of the center (**Figure 5-31 -b**) improves the peak value of the small-signal gain around the center frequency $f_0 = 27GHz$ as reported in **Figure 5-32 -a**. The widths w_1 and w_2 of both spirals has been optimized to further increase the peak value of the small-signal gain of the entire PA circuit. As it can be seen in **Figure 5-32 -b**, if the widths are reduced from the maximum value of the technology, 30um for both M5T and M6T layers, up to 20um the peak gain value increase of 1dB because the coupling factor varies between the spirals [97].



a) b)

Figure 5-32: Effects of the geometry variations over the small-signal gain: a) shifting of the differential spiral; b) decrement of the width of the spirals.

The performances of the stand-alone inter-stage matching balun are reported in **Figure 5-33** and **Figure 5-34**. The obtained results by simulating the structure in differential mode show that the insertion loss is a critical parameter when considering a high impedance ratio; in fact, its value drops up to 4 dB at $f_0 = 27GHz$ while the worst-case value is 4.5dB at

24GHz (**Figure 5-33**). Regarding the single-ended simulation results of the balun reported in **Figure 5-34 -a** and **Figure 5-34 -b**, the amplitude imbalance is $\leq 1\ dB$ while the phase imbalance is $\leq 2°$ in the frequency band $(24 \div 30)$ GHz.

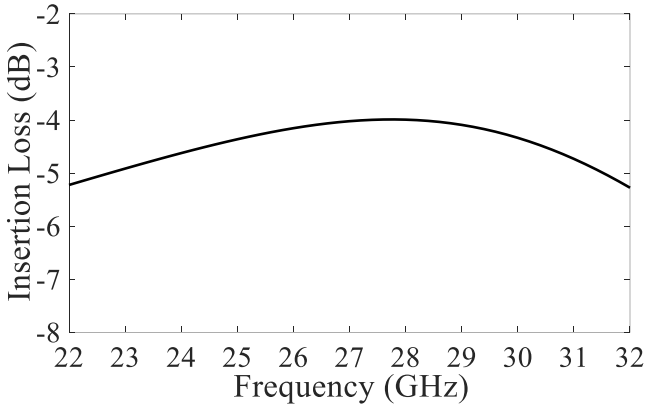


Figure 5-33: Insertion loss over frequency (differential simulation).

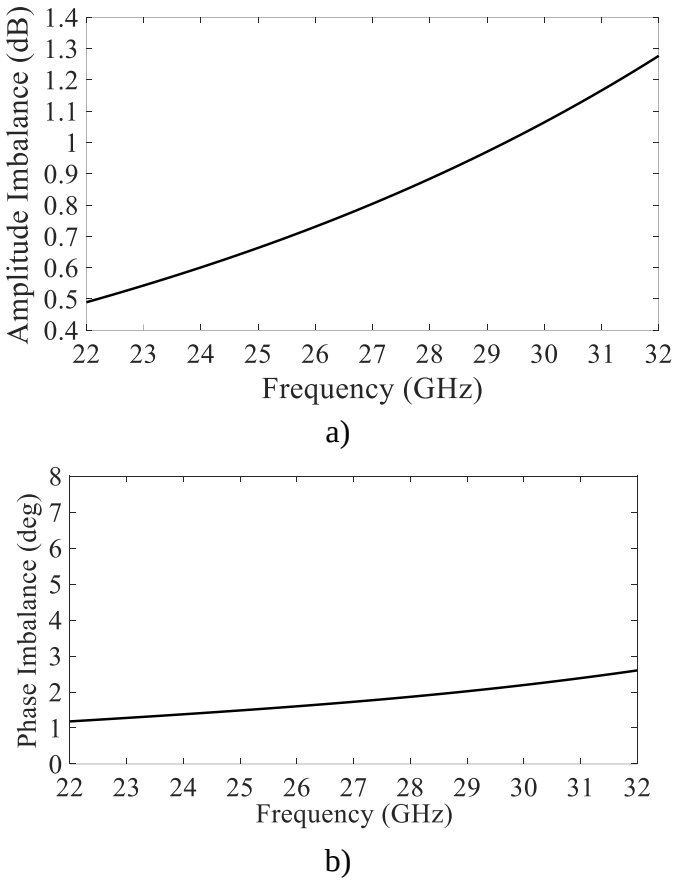
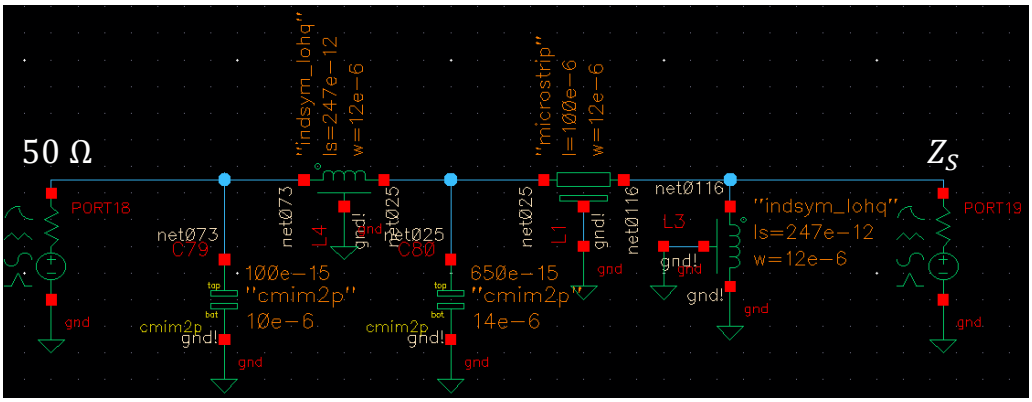
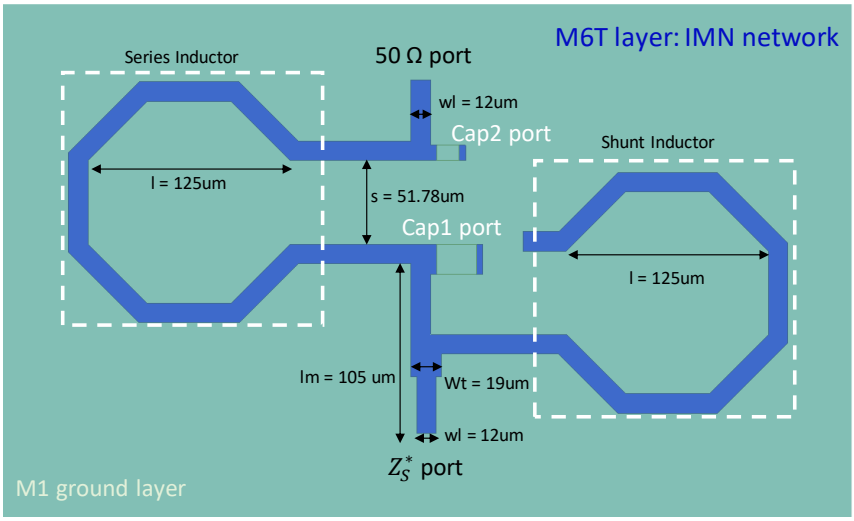


Figure 5-34: Three-port simulation. a) Amplitude Imbalance; b) Phase Imbalance.

In the input section, a matching network (IMN) is used to adapt the source impedance of the PA driver (Z_S^*) with the 50Ω single-ended input impedance (**Figure 5-35**). In the VGA circuit, a terminal of the VVA circuit will be connected at 50Ω port and the other one to the input GSG pad. This network consists of two shunt capacitors Cap_1 and Cap_2, represented through two ports in HFSS, of value equal to 650 fF and 100 fF as shown in **Figure 5-35**. In the SnP file of this network, two real MIM capacitors of equal value will be connected to the two grounded ports as shown in **Figure 5-37**. Moreover, a one-turn inductor placed on M6T metal layer whose inductance is 250 pH is connected in series between two capacitors, while another inductor of the same value is grounded to M1 layer. This shunt inductor is employed to direct the emitter current of the PA CB driver that comes into the network by Z_S port to the ground. The S-parameter results of the stand-alone network are depicted in **Figure 5-36**. These plots show that amplitude variation in the band of interest (24 ÷ 30) GHz is less than 1 dB and the insertion loss is equal to 1.5 dB at $f_0 = 27\ GHz$, while the $-10\ dB$ impedance bandwidth covers the entire band of interest.



a)



b)

Figure 5-35: Input Matching Network. a) schematic view; b) top view of HFSS layout.

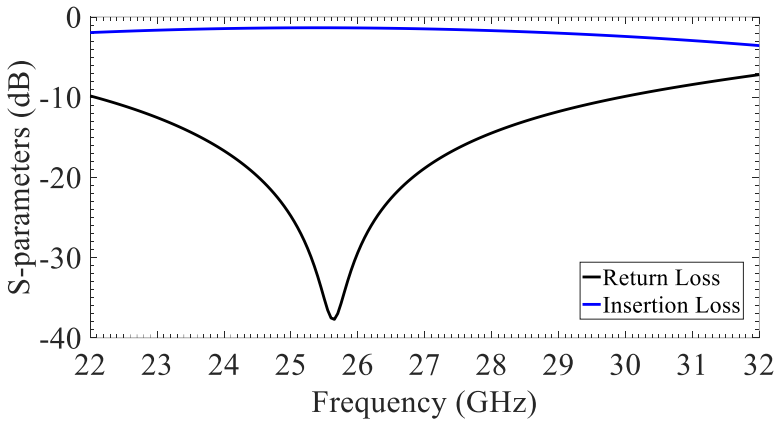


Figure 5-36: S-parameter results of Input Matching Network.

The portion of the PA schematic containing both driver and input sections is reported in **Figure 5-37**. The SnP blocks of the aforementioned elements (ISMB, PA driver core, IMN and input GSG pad) are taken into account to make more realistic the simulation of the entire PA circuit by considering the EM effects of the latter. Only PDK passive components as poly resistors, MOS and MIM capacitors are used in this design. The MIM and MOS capacitors (tot. capacitance = 21 pF) are connected, by RF block capacitor port of the inter-stage matching SnP block, to the supply (V_{cc}) network (yellow area in **Figure 5-37**).

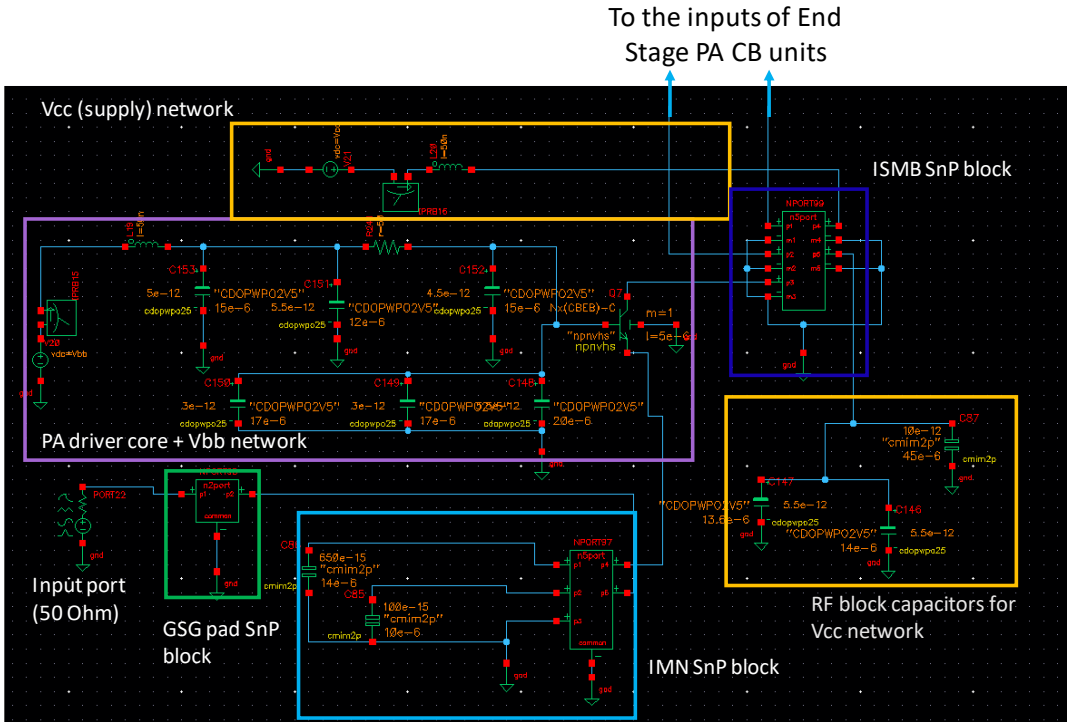


Figure 5-37: Driver/input circuit section.

To attenuate the impedance resonance due to the long-term memory effect along the biasing (V_{bb}) line of the PA driver (**Figure 5-39**), the value of series resistor marked in red in **Figure 5-38** is changed from 10Ω up to 50Ω, without sacrificing too much the output power performance of the PA.

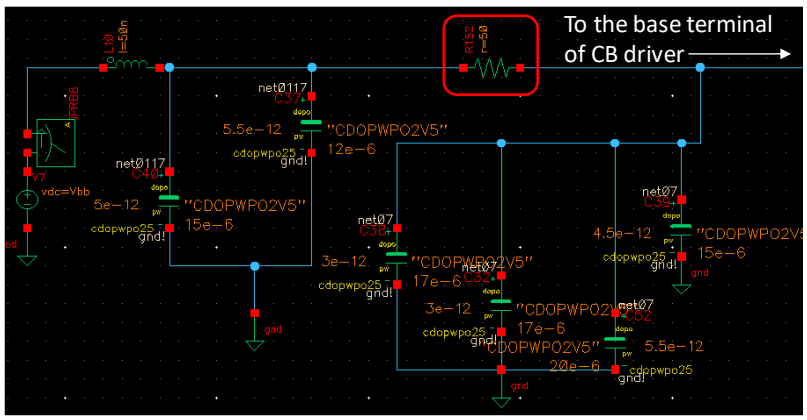


Figure 5-38: Biasing network of PA driver amplifier.

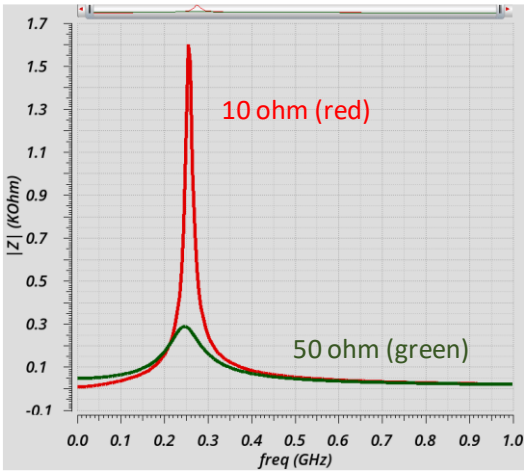


Figure 5-39: Memory-effect reduction by increasing the value of series resistance.

5.7 Layout and circuit prototype

The final schematic of the entire VGA circuit comprises of the two sections treated previously and the circuit of the conventional NMOS VVA described in section 5.5 is shown in **Figure 5-40**.

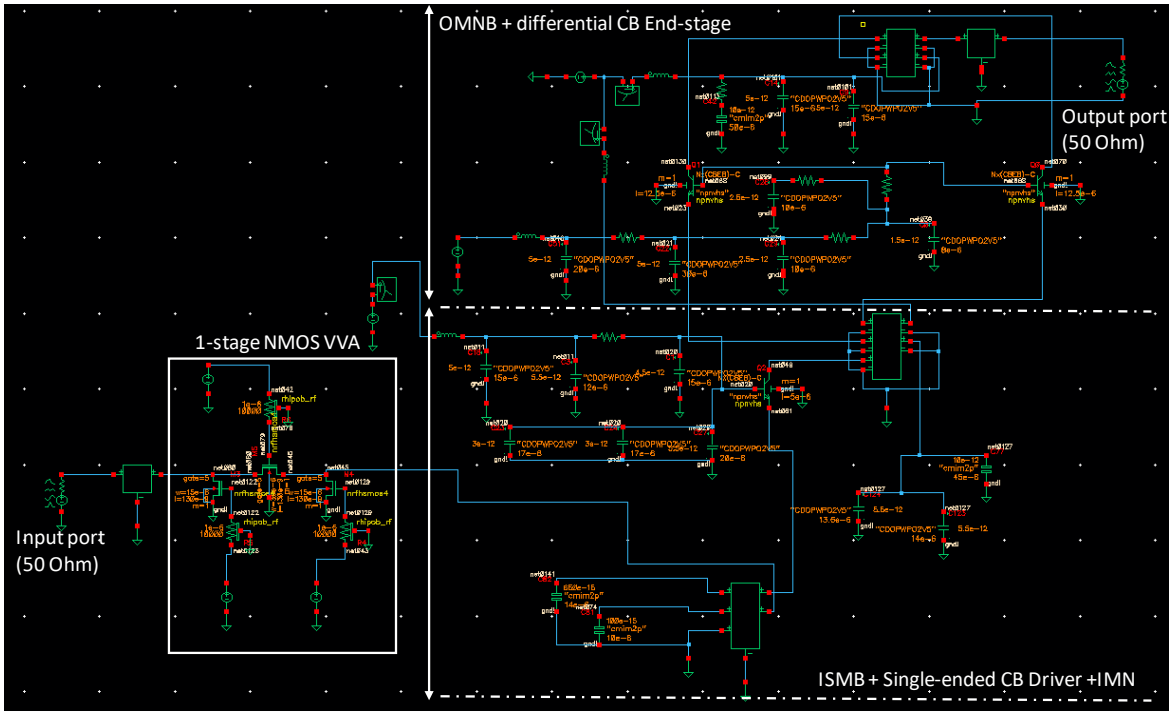
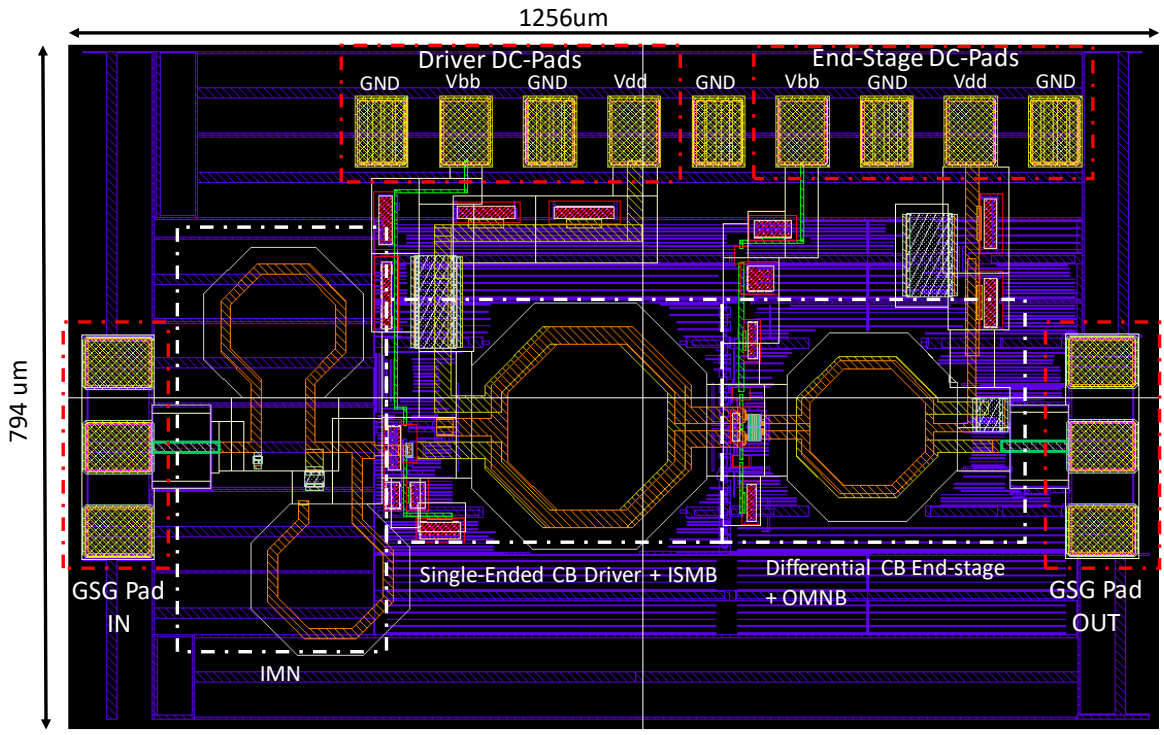
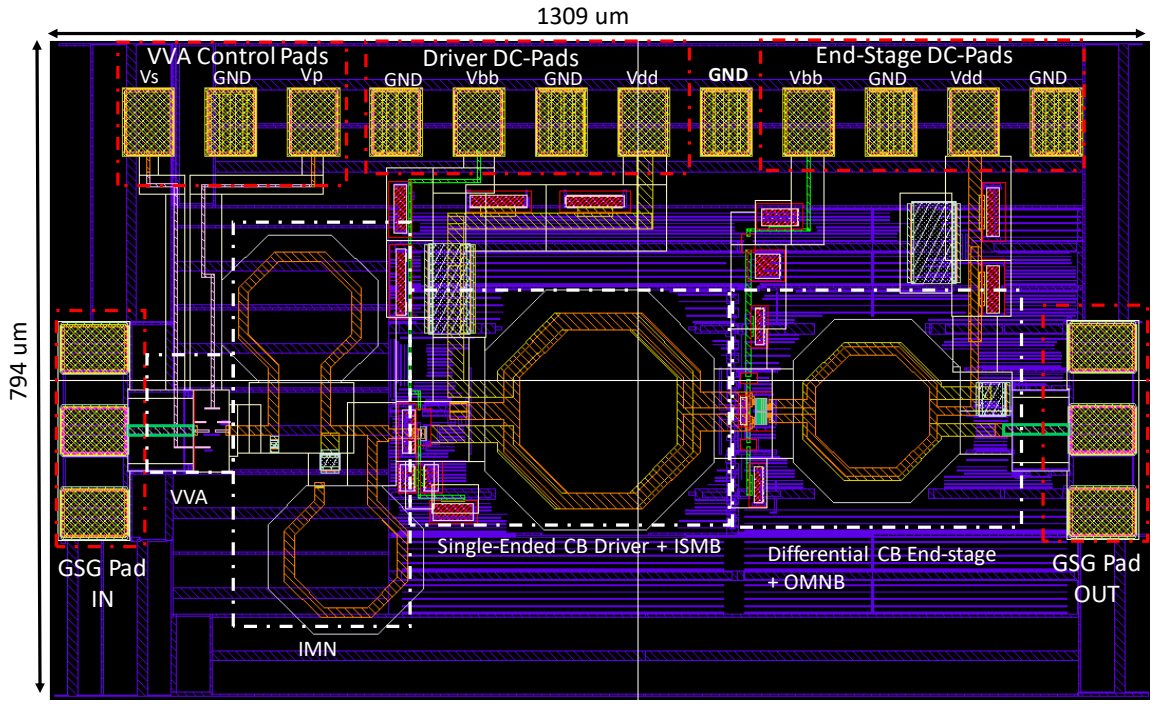


Figure 5-40: Final schematic of VGA circuit.

Figure 5-41 -a and **Figure 5-41 -b** show the layouts in Cadence of both TX-mode dual-stage power amplifier and the attenuator-based VGA prototypes. As mentioned above, only MOS capacitors are used as filtering elements along the biasing (V_{bb}) lines (the green ones placed on the M4 layer of the BEOL) of both end-stage and driver amplifiers. The use of these capacitors is because the voltage swing of RF signal along V_{bb} lines should be lower than the one of output RF signal that flows inside V_{dd} lines. For similar reasons, the first filtering capacitors connected on the V_{dd} lines are chosen as MIM capacitor since they support a higher voltage swing without compromise their physical integrity. The position of GSG pads and DC pads in both circuits have been chosen to reduce the die dimensions along x and y directions. A microphotograph of both circuits is reported in **Figure 5-42**.



a)



b)

Figure 5-41: Layout of two prototypes. a) Dual-stage PA; b) Attenuator-based VGA.

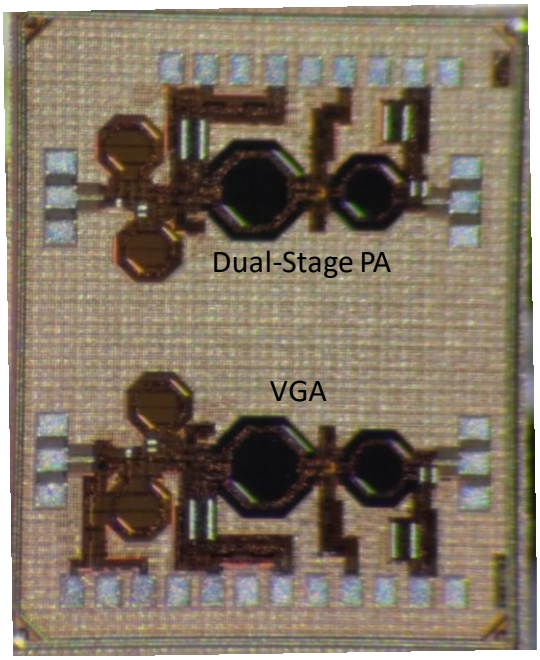
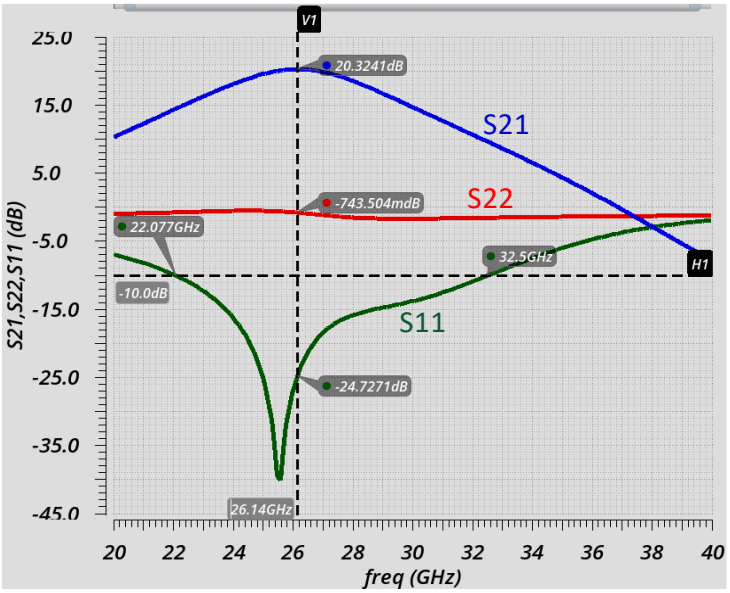


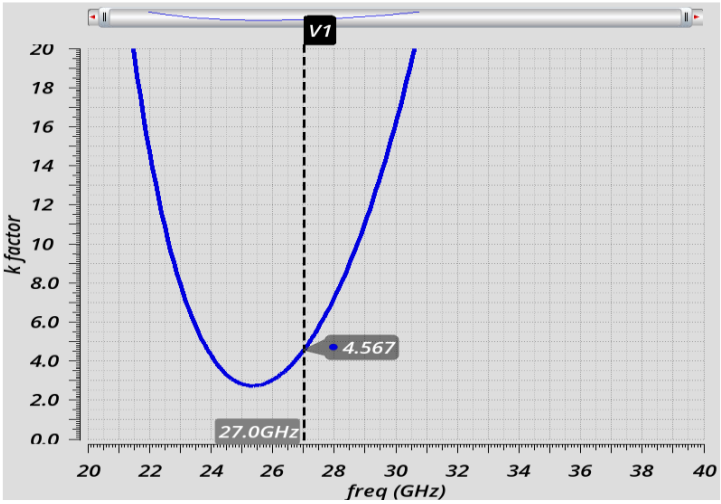
Figure 5-42: Microphotograph of both dual-stage PA and VGA circuits.

5.8 Simulation results

The small-signal analysis was performed on the stand-alone dual-stage PA final schematic in **Figure 5-40** (excluding the VVA circuit connection). **Figure 5-43 -a** show that the peak gain is higher than 20dB and the gain variation around 27GHz in 1GHz of bandwidth is lower than 0.6dB, while the input return loss (S_{11} parameter) is $\leq -12dB$ in all the band of interest (24 ÷ 30) GHz. As it can be seen, the output return loss (S_{22} parameter) is worst respect to the input return loss, but this result is not unusual for the common-base amplifier due to the inherent behavior of this configuration [98]. Regarding the small-signal stability, the K factor of the PA circuit is higher than 4 at $f_0 = 27GHz$ while its minimum value is 2.8 at 25 GHz as shown in **Figure 5-43 -b**. Globally. the PA device is unconditionally stable in the band of interest (24 ÷ 30) GHz since $K > 1$ (Rollet's stability condition).



a)



b)

Figure 5-43: Dual-stage PA small-signal results. a) S-parameter response; b) K-factor.

One-tone large-signal simulation at the center frequency $f_0 = 27GHz$ was accomplished on the stand-alone dual-stage PA. The simulated output power at 1dB compression point is equal to 14.3 dBm (**Figure 5-44 -a**), while the power-added efficiency (PAE) is almost 18% at OP1dB point and exceeds 30% at P_{SAT} (**Figure 5-44 -b**). These results confirm that the proposed power amplifier could be employed as end-stage PA in low-power SiGe transmitters for 5G phased array systems [13][24].

Considering the plot reported in **Figure 5-44 -c**, the circuit has a high degree of AM-PM linearity up to OP1dB point due to the use of common-base units that operate in AB class. This is a crucial result as the AM-PM linearity affects the performance of the PA in terms of error vector magnitude (EVM) when a specific modulation (e.g. 64-QAM and 256-QAM for 5G-NR applications) is considered in the multi-tone harmonic-balance measurements. The overall static power consumption of the entire circuit is equal to $150mW$ at 1dB compression point (**Figure 5-44 -d**).

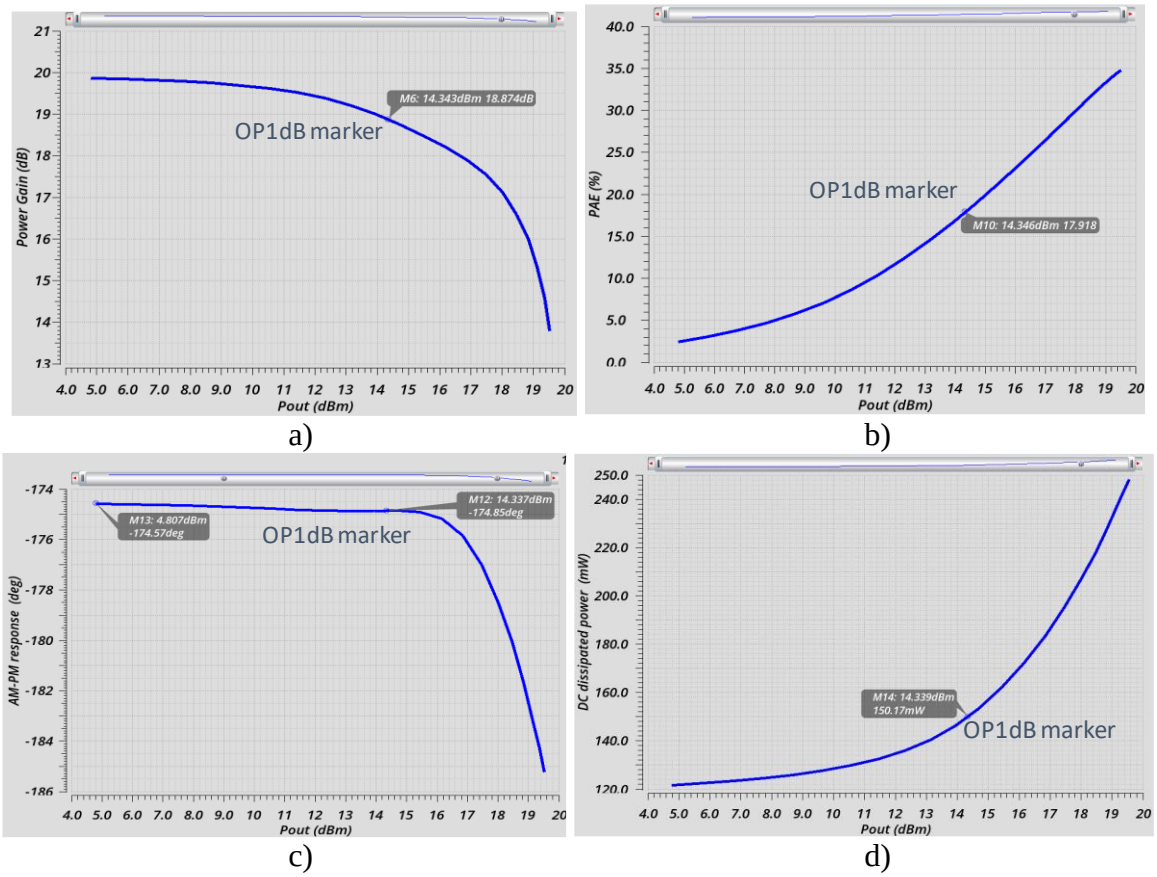
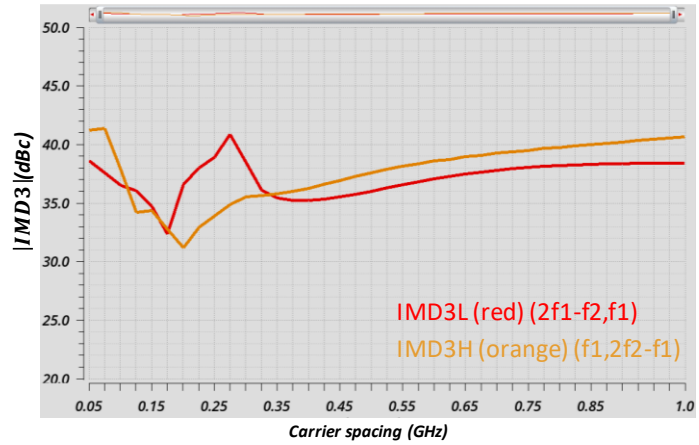
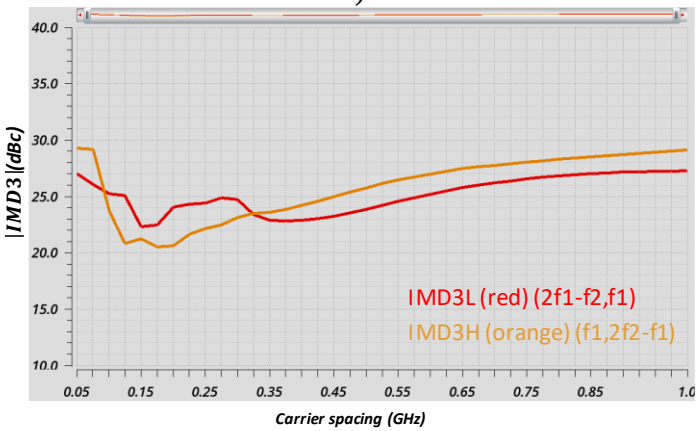


Figure 5-44: Dual-stage PA large-signal results at 27GHz. a) Power gain vs Pout; b) PAE vs Pout; c) AM-PM vs Pout; d) DC power vs Pout.

Two-tones harmonic balance analysis was performed on the dual-stage PA circuit considering the following testbench parameters: $f1 = 27GHz$; $f2 = f1 + s$; carrier spacing interval = $[50MHz, 1GHz]$. **Figure 5-45 -a** shows that for a typical channel bandwidth equal to 400MHz (specification for 5G small cells operating in the FR2 bands [52]) the 3rd-order intermodulation distortion at 10 dB of back-off is close to 35 dBc, while at 6dB of back-off this value drops up to 23 dBc (**Figure 5-45 -b**).



a)

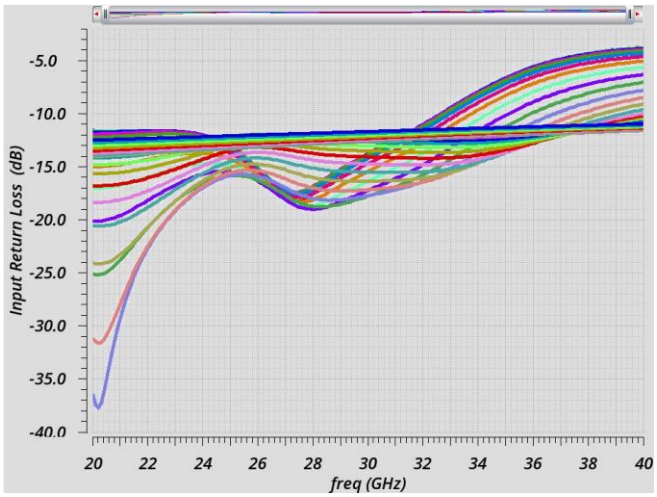


b)

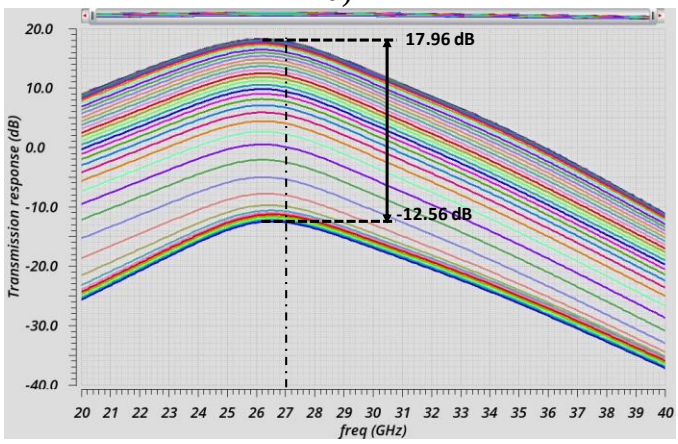
Figure 5-45: Dual-stage PA two-tone harmonic balance analysis. a) IMD3 vs carrier spacing at 10dB BO; a) IMD3 vs carrier spacing at 6dB BO

By placing the conventional NMOS Pi-type VVA described in section 5.5 as the first block inside the VGA circuit shown in **Figure 5-40**, it is possible to modify the gain of the entire VGA circuit by changing the amplitude of RF signal in input to the dual-stage PA. In particular, the gain is varied by changing the control voltage V_p for the shunt NMOSs from 0V to 1.2V and the control voltage V_s for series NMOS from 1.2V to 0V with a resolution of 30mV. The small-signal performances of the VGA are reported in **Figure 5-46**. **Figure 5-46 -a** shows that, for all the gain states of the circuit, the -10dB impedance bandwidth covers the entire band of interest. **Figure 5-46 -b** confirms that the gain control range is

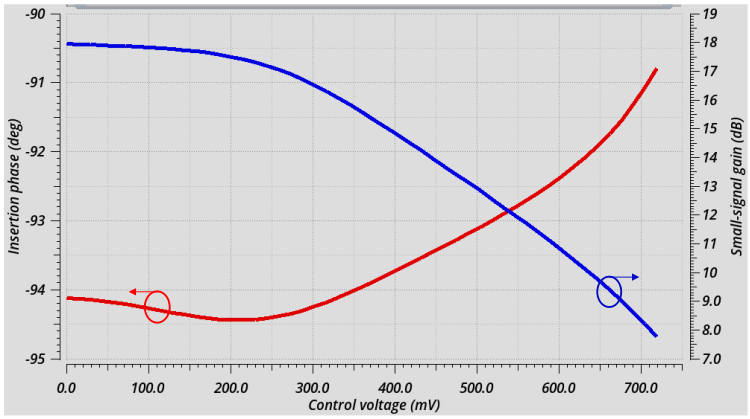
higher than 30dB just like the attenuation range of the VVA attenuator reported in **Figure 5-16 -a**. As reported in **Figure 5-46 -c**, the maximum phase imbalance evaluated in a 10dB control range at 27 GHz is almost 5°. Therefore, if the VGA with this gain control range is employed in a phased array transceiver to control the sidelobe level up to 25dB of suppression value [13], external phase compensation circuits could be avoided, thus reducing the complexity of the entire system. One-tone large signal analysis at $f_0 = 27GHz$ was performed on the VGA circuit when the VVA circuit is in its lowest state of attenuation (that is, the maximum gain state of the VGA). The performance discrepancy between stand-alone dual-stage PA (**Figure 5-44**) and VGA circuit (**Figure 5-47**) in terms of OP1dB, PAE and AM-PM response at 1dB compression point is very small.



a)

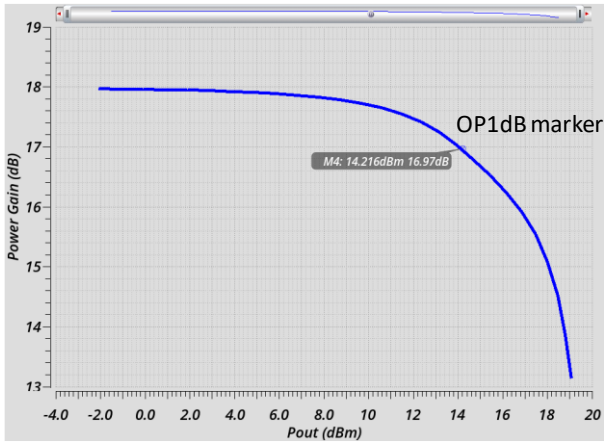


b)

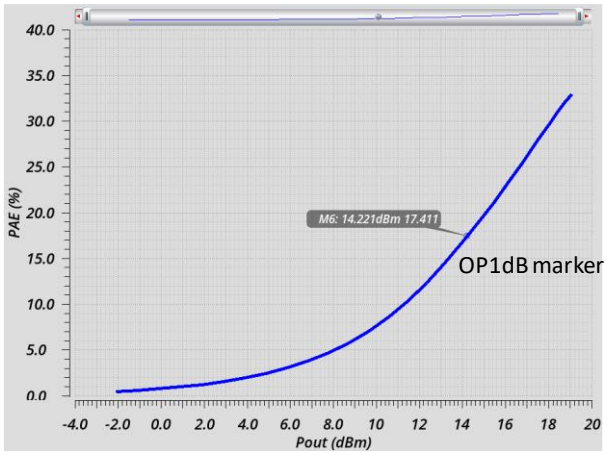


c)

Figure 5-46: VGA circuit S-parameter results for all the gain states. a) input return loss; b) small-signal gain; c) Insertion phase in 10dB gain control range.



a)



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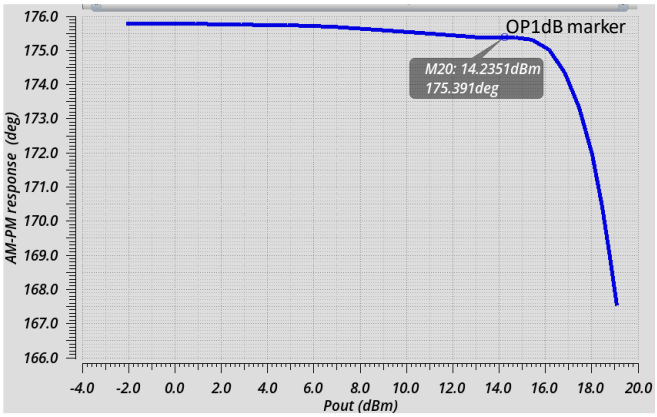

c)

Figure 5-47: VGA circuit large signal analysis at 27GHz. a) Power gain vs Pout; b) PAE vs Pout; c) AM-PM response vs Pout.

5.9 Conclusion and future works

The primary object of this study is to design and develop different building blocks of phased array systems for 5G Ka-band MIMO small cells. A 28 GHz 32-element dual-polarized array based on the use of ultra-low profile Magneto-Electric dipole has been proposed. This structure operating in the n257 frequency band (26.5 - 29.5 GHz) enables the pointing control of the radiated beam in a wide scan range ($\pm 55° AZ, \pm 20° EL$) while achieving a boresight gain higher than 18 dBi in the entire band of interest. The radiation patterns of both passive array structure and isolated ME dipole have been measured in the anechoic chamber and a good agreement between normalized measured and simulated data has been achieved. Compared to the conventional ME dipole array found in the literature which are realized in stack-ups with a core thickness of $\frac{\lambda_g}{4}$, the novelty introduced in this design is related to the implementation of the novel wideband capacitively-coupled dual-polarized ME dipole in a light multi-layer PCB stack-up with a very small profile (core thickness $= 0.074\lambda_g$ or $0.047\lambda_0$ at 28GHz). The adopted solution does not require complex

stack-ups with air cavities (to increase the impedance bandwidth performance) which could reduce the reliability over time of the radiator. Since the resonance length of the printed electric dipole is near to $\frac{\lambda_0}{2}$, the inter-element spacing cannot be too small. This leads to an increment of the impedance mismatch when the beam is steered along a large scan angle as reported in this thesis. Therefore, a possible future work could be the realization of phased arrays based on the use of miniaturized Magneto-Electric dipoles to decrease the coupling between antenna elements and improve the impedance matching when scanning. Finally, a 0.13um SiGe BiCMOS variable gain amplifier (VGA) for 5G phased array applications has been taken into account. At first, the performance of a Ka-band conventional NMOS single-stage Pi-type voltage variable attenuator (VVA) has been compared with a novel Ka-band hybrid single-stage Pi-type VVA where two shunt HBT transistors in reverse-saturation (RS) mode act as varistors to change the attenuation state of the cell continuously. Both circuits achieve a return loss lower than -10 dB from DC to 40 GHz without employing any external matching elements such as $\frac{\lambda}{4}$ transmission lines and/or inductors. The achieved attenuation range is higher than 25 dB, while the amplitude imbalance less than 7.5 dB in all the Ka-band (20 – 40 GHz) for both structures. The proposed hybrid RS-HBT VVA provides an IP1dB value which is 3.5 dB higher than the one achieved with conventional NMOS structure in all the Ka-band, while the linearity in terms of IIP3 is improved of 2 dB compared to the one obtained with conventional circuit in the same frequency band. Both circuits have been realized in a standard 0.13um SiGe BiCMOS process from ST Microelectronics and two prototypes are actually under test. If the simulation results will be validated by measurement ones, the proposed hybrid Pi-type VVA will represent the first example of voltage variable attenuator employing two shunt

reverse-saturated HBTs as varistor to change continuously the attenuation state of the cell while providing an improved dynamic range.

At this point, a dual-stage VGA with higher power capability and wider gain tuning range has been developed considering the aforementioned 0.13um SiGe BiCMOS process from ST Microelectronics. In this design, it has been demonstrated that AB-class common-base (CB) configuration outperforms the AB-class common-emitter (CE) one in terms of power output and AM-PM deviation. The use of dual stage structure with a differential end- stage PA leads to an improvement in terms of P_{out}, common-mode noise rejection and gain. Furthermore, the mechanism of gain control by using the conventional NMOS VVA as first block of the VGA is very simple and does not require complex DC control circuits. The VGA circuit achieves more than 14 dBm of OP1dB, when the maximum gain of 18 dB is selected by VVA, while the power added efficiency is near to 20% at 1dB compression point in the same gain condition. Moreover, the AM-PM linearity is very high up to 1dB compression point. The input return loss of this circuit is lower than -10 dB in the entire 30-dB control range. The achieved performances confirm that this circuit could be employed directly as an end-stage variable gain PA in Si-based 5G transmitters or as a driver circuit in hybrid Si/GaN-based or Si/GaAs-based transceivers. Stand-alone dual-stage PA and the entire VGA have been prototyped and these circuits have to be measured. Future works could include the employ of a more efficient derivative superposition (DS) technique to design Si-based end-stage PAs with improved performances in terms of P_{out}, back-off efficiency and linearity.

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