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TITOLO TESI

A Defect-Centric Analysis of the Channel Hot Carrier Degradation

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Para Jeanina por todo su amor, apoyo y paciencia...

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Sommario

Durante l'ultimo decennio, il channel hot carrier (CHC) é stato considerato uno dei più importanti meccanismi di degrado della moderna tecnologia CMOS. La degradazione CHC si verifica quando un voltaggio superiore a quello di saturazione viene applicato sul terminale di *drain* e, contemporaneamente, un voltaggio superiore alla tensione di soglia (V_{TH}) viene applicato sul terminale di gate. Nel presente lavoro, abbiamo utilizzato la cosiddetta *defect-centric distribution* (DCD) per spiegare e descrivere il meccanismo di degradazione CHC. Il DCD si basa su due presupposti: il V_{TH} prodotto da una singola carica segue una distribuzione esponenziale (valore medio η) e il numero totale di difetti segue la distribuzione di Poisson (valore medio N_t). La combinazione di questi due presupposti da come risultato la DCD. Negli ultimi anni, la distribuzione DCD è stata usata per descrivere e spiegare la bias temperature instability (BTI) ed è in grado di predirre le code estreme della distribuzione ΔV_{TH} fino a 4σ . Il vantaggio di usare il DCD è che i suoi primi e secondi momenti sono direttamente correlati ai parametri fisici $\eta \in N_t$.

Nel presente lavoro, é stato dimostrato che il DCD è anche in grado di descrivere e spiegare il degrado della distribuzione ΔV_{TH} fino a 3σ . É stata studiata la dipendenza dei parametri deffect-centric, $\eta \in N_t$, in relazione alla geometria del dispositivo. É stato dimostrato che η è inversamente proporzionale all'area del dispositivo come in la degradazione BTI. Inoltre, il valore previsto della distribuzione ΔV_{TH} (< ΔV_{TH} >) si incrementa fortemente quando la lunghezza di canale (L) diminuisce e si incrementa debolmente con il decremento della larghezza del dispositivo (W). In la degradazione BTI, si riporta che non vi è alcuna dipendenza tra $\langle \Delta V_{TH} \rangle$ ed L. Pertanto, la forte dipendenza trovata è da atribuire alla degradazione CHC. Si é anche studiata la dipendenza della temperatura (T) dei parametri defect-centric e abbiamo trovato che η non dipende da T, al contrario degli esperimenti BTI, dove invece N_t aumenta con T, fatto che si spiega con l'attivazione del meccanismo di dispersione elettrone-elettrone. Inoltre, abbiamo estratto una energia di attivazione di ~ 56meV per N_t . Finalmente, abbiamo usato dispositivi matching-pair con la finalitá di studiare la variabilità tempo zero e la variabilità dipendente dal tempo. É stato dimostrato che il tempo di stress e la tensione di stress applicati sul terminale di *drain* non influenzano la variabilità.

Summary

During the last decade, channel hot carrier (CHC) has been considered one of the most important degradation mechanisms in modern CMOS technology. The CHC degradation occurs when a voltage higher than the saturation voltage is applied on the drain terminal and, simultaneously, a voltage higher than the threshold voltage (V_{TH}) is applied on the gate terminal. In the present work, we have used the so-called defect-centric distribution (DCD) in order to explain and describe the CHC degradation mechanism. The DCD is based in two assumptions: the V_{TH} produced by a single charge follows an exponential distribution (mean value η) and the total number of traps (or defects) is Poisson distributed (mean value N_t). The combination of these two assumptions gives us the DCD. During the last years, the DCD distribution has been used for describing and explaining the bias temperature instability (BTI) and it is able to predict the extreme tails of the V_{TH} shift distribution up to 4σ . The advantage of using the DCD is that its first and second moments are directly related to the physical parameters η and N_t .

In our work, we have shown that the DCD is also able to describe and explain the V_{TH} shift distribution of CHC degradation up to 3σ . We have studied the dependence of the defect-centric parameters, η and N_t , with respect to the device geometry. We have shown that η is inversely proportional to the device area as in BTI degradation. As well, the expected value of the V_{TH} shift distribution ($\langle \Delta V_{TH} \rangle$) strongly increases when the channel length (L) decreases and weakly increases with the decrement of the device width (W). In BTI degradation, it has been reported that there is no dependence between $\langle \Delta V_{TH} \rangle$ and L; therefore, the strong dependence we have found is the *signature of the* CHC degradation. As well, we have studied the temperature (T)dependence of the defect centric parameters and we have found that η does not depend on T, as in BTI experiments, whereas N_t increases with T, which is explained by the activation of the electron-electron scattering mechanism. Moreover, we have extracted an activation energy of ~ 56meV for N_t . Finally, we have used matching pair devices in order to study the time-zero variability and the time-dependent variability. We have shown that the stress time and the stress voltage applied on the drain terminal do not affect the time-dependent variability.

List of Publications

Journal Papers:

- L. M. Prócel, F. Crupi, J. Franco, L. Trojman, B. Kaczer. A Defect-Centric Analysis of the Temperature Dependence of the Channel Hot Carrier Degradation in nMOSFETs. submitted to IEEE Transactions on Device and Materials Reliability.
- L. M. Prócel, F. Crupi, J. Franco, L. Trojman, B. Kaczer, N. Wils, H. Tuinhout. A Defect-Centric perspective on channel hot carrier variability in nMOSFETs. Microelectronic Engineering, vol. 147, pp. 72-74, 2015.
- L. M. Prócel, F. Crupi, J. Franco, L. Trojman, B. Kaczer. Defect-Centric Distribution of Channel Hot Carrier Degradation in Nano-MOSFETs. IEEE Electron Device Letters, vol. 35, pp. 1167-1169, 2014.
- L. M. Prócel, L. Trojman, J. Moreno, F. Crupi, V. Maccaronio, R. Degraeve, L. Goux, E. Simoen. Experimental evidence of the Quantum Point Contact theory in the conduction mechanism of bipolar HfO2-based resistive Ran-

dom Access Memories. Journal of Applied Physics, vol. 114, pp. 074509, 2013.

- V. Maccaronio, F. Crupi, L. M. Prócel, L. Goux, E. Simoen, L. Trojman, E. Miranda. DC and low-frequency noise behavior of the conductive filament in bipolar HfO2based Resistive Random Access Memory. Microelectronic Engineering, vol. 107, pp.1-5, 2013.
- L. Villamagua, R. Barreto, L. M. Prócel, A. Stashans. Hydrogen impurity in SrTiO3: structure, electronic properties and migration. Physica Scripta, vol. 75, pp. 374-378, 2007.
- C. Zambrano, A. Sánchez, L. M. Prócel, A. Stashans. Structural and electronic properties of PbZrxTi1-xO3 (x=0.5, 0.375): a quantum-chemical study. Internacional Journal of quantum Chemistry, vol. 95, pp. 37, 2003.
- L. M. Prócel, F. Tipán, A. Stashans. Mott-Wannier excitons in the tetragonal BaTiO3 lattice. International Journal of Quantum Chemistry, vol. 91, pp. 586, 2003.
- Stashans, C. Zambrano, A. Sánchez, L. M. Prócel. Structural properties of PbTiO3 and PbZrxTi1-xO3: a quantum-

chemical study. International Journal of Quantum Chemistry, vol. 87, pp. 145-151, 2002.

Conference Papers:

- B. Kaczer, J. Franco, M. Cho, T. Grasser, Ph. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. De Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken, A. Thean. Origins and implications of increased channel hot carrier variability in nFinFETs, presented at IEEE International Reliability Physics Symposium (IRPS), pp. 3B.5.1 - 3B.5.6, 2015.
- R. Viteri, L. M. Prócel, F. Tipán, D. F. Ortiz, A. Stashans. Quantum-chemical study of excitons in tetragonal BaTiO3 and SrTiO3 crystals, presented at SPIE Proceedings, vol. 5122, pp. 295-302, 2003.
- A. Sánchez, C. Zambrano, L. M. Prócel, A. Stashans. Structural and electronic properties of PZT, presented at SPIE Proceedings, vol. 5122, pp. 310-316, 2003.

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Chapter 1

Introduction

1.1 Channel Hot Carrier degradation in long channel devices

During the 80's, the study of the Channel Hot Carrier (CHC) degradation had a lot of interest because of the high voltages $(\sim 5V)$ applied on the drain and gate terminals when the Metal-oxide-semiconductor field-effect transistor (MOSFET) was in on-state. The application of a gate voltage (V_{GS}) larger than the threshold voltage (V_{TH}) and, simultaneously, a drain voltage (V_{DS}) larger than the saturation voltage provokes the injec-

tion of high energetic electrons and holes (hot carriers) into the gate dielectric. The most accepted physical mechanism for CHC degradation in large devices is that hot carriers are generated by the impact ionization mechanism at the pinch-off region. This mechanism is supported by lucky-electron model developed by Chemin Hu [1, 2, 3]. In this model, a single particle (electron or hole) is accelerated by the lateral electric field (E_{lat}) in the channel, and then it collides with a valence electron of a static crystal atom. As result of this collision, an electron-hole pair with enough energy to cross the band gap of the dielectric oxide is generated [1, 2, 3, 4]. With this model, the field-driven paradigm began, since hot carrier are supposed to be generated and controlled by the E_{lat} .

Microscopically, this carrier injection provokes a degradation of the oxide-channel interface due to the increment of the interface traps (ΔN_{it}) [4, 5]. Macroscopically, this interface degradation causes a reduction of the drain current (I_{DS}) and an increment of V_{TH} . In addition, ΔN_{it} in function of the stress time (t_{stress}) follows a power law with a typical exponent of 0.5 [5].

In nMOSFETs, hot electrons are injected into the gate, whereas hot holes are injected into the bulk generating an increment of the bulk current (I_{BS}) , which is a measure of the CHC degradation severity [4, 5]. In pMOSFETs occurs the opposite: hot holes are injected into the gate and hot electrons into the bulk. The maximum of I_{BS} is the criterion for considering the maximum CHC degradation (worst-case) and it occurs when $V_{GS} = V_{DS}/2$ [4, 5, 6]. The typical criteria for calculating the transistor life-time are: a reduction of 10% of I_{DS} in the saturation region, a reduction of 10% of I_{DS} in the linear region or a V_{TH} shift of 30mV [6, 7, 8].

1.2 Channel Hot Carrier degradation in short channel devices

With the scalings of the channel length and the supply voltage, the CHC degradation was considered less relevant during the 90's, whereas the bias temperature instability degradation (which provokes a V_{TH} shift due to an application of a $V_{GS} > V_{TH}$ at high temperature) became more important [5, 6]. However, the supply voltage scaling slows down in comparison to the channel length scaling due to the non-scalability of the sub threshold slope [6, 7, 9, 10]. This has originated that, from the beginning of the last decade, CHC injection was again considered one of the most important degradation mechanisms.

When the channel length decreases below the 130nm, the maximum damage condition changes from the maximum impact ionization ($V_{GS} = V_{DS}/2$) to $V_{GS} = V_{DS}$, where a higher vertical electric filed is applied [4, 5, 6, 11]. The exponent of the power law of ΔN_{it} vs. t_{stress} is still found between 0.4~0.6 showing that the dominant damage is generated by the increment of ΔN_{it} [5]. However, in [11], it has been found exponents of the power law in the range 0.1~0.2 in CHC experiments done in short channel nFinFETS with high- κ dielectric, showing, in these cases, that the dominant degradation mechanism is the generation of oxide bulk defects. The peak of N_{it} in function of the channel length coordinate shows the maximum degradation region in the channel, which is located at the drain overlap [4, 5]. However, this peak does not coincide with the maximum of E_{lat} [4].

In short devices, the channel length is not enough to accelerate the charges in order to generate electron-hole pairs with enough energy to cross the dielectric band-gap [4, 5]. In addition, it has been found channel hot carrier degradation even at low stress voltages in short devices [4, 5]. All these evidences show that in short devices, the E_{lat} is not the only cause of damage to the device. In order to explain these changes, the energy-driven paradigm developed by Rauch and La Rosa was introduced. According to this new paradigm, the carrier energy plays the most important role to damage the oxide-channel interface [12].

It is well known that the increment of ΔN_{it} is caused by the rupture of the Si-H bond during CHC degradation [4, 5, 13, 15]. This rupture can be done by a single particle (SP, like in the lucky-electron model) or by a series of multiple particles (MP, cold carriers) that bombard the bond until its rupture [4, 5, 13, 14]. In ultra-scaled devices, the probability of having a SP mechanism is very low and the MP mechanism is dominant [4]. A good way to understand the CHC degradation mechanism is by computing the carrier energy density function (DF), which takes into account the majority of the energy exchange mechanisms like: impact ionization, surface scattering, scattering at ionized impurities, electron-phonon scattering, and electronelectron scattering (EES). As well, other important mechanisms like Auger recombination and electron-dipole interaction can be considered [4, 5, 13, 16]. In long devices, the scattering mechanisms depopulate the high energies of the carrier energy DF and then soften the CHC degradation in agreement to the decrement of this degradation with respect to the temperature (T) [17]. On the other hand, in short channel devices, the EES plays an important role and populates the tail of the carrier energy DF, and as result, the increment of T increases the CHC degradation [4, 5, 13, 18].

1.3 Aim of this work: A Defect-Centric Analysis

The purpose of this work is to understand the defect generation (microscopical property) from the extraction of the V_{TH} shift (macroscopical property) caused by the CHC degradation. In order to study the defect generation, we use the so-called Defect-Centric theory developed by Kaczer and Graser in [19, 20]. The result of this theory is the Defect-Centric distribution (DFD), which is based in two assumptions [19, 20]:

- i) the V_{TH} shift produced by a single charge follows an exponential distribution with mean value η , and
- ii) the total number of traps follows a Poisson distribution with mean value N_t .

The DCD has been used for describing and explaining the

BTI degradation behaviour, and it has been shown that it can predict very well the extreme tails of the V_{TH} shift distribution up to 4σ [22]. The DCD and its capacity of predicting the BTI behaviour has been tested in five generations of Intel technologies (from 90nm to 22nm) in different materials and architectures, showing very good results [23]. The model takes into account the traps located in the oxide as well as the interface traps without any distinction [21].

The average parameters used for estimating the life-time in long devices (see section 1.1) are not valid in short devices where the complete distribution is needed to understand and predict the degradation behaviour [19, 20]. The principal reason is that only few atomistic defects can affect the device operation behaviour in ultra-scaled devices. In addition, there is a limited number of studies on the statistical distribution of CHC-induced degradation in nanoscale devices [24, 25, 26, 27]. Taking into account all these considerations, the novelty of the present work is to use the Defect-Centric model (used and tested in BTI degradation) in order to explain the CHC degradation behaviour. This type of analysis is extremely useful to physically understand the CHC degradation of nanoscale MOSFETs in terms of individual defects.

1.4 Outline of the document

- Chapter 2: The principal physical models for explaining the CHC degradation are reviewed in this chapter. Here, we study the Hess model, the energy-driven paradigm, the Bravaix model and the Tyaginov model.
- Chapter 3: Here, we present the principal experimental measurement techniques. In addition, a complete description of the DCD is presented.
- Chapter 4: In this chapter, we show a defect-centric analysis of the CHC degradation for different geometries. As well, the principal defect-centric parameter dependences are studied.
- Chapter 5: Here, we present a Defect-Centric analysis of the temperature dependence in CHC degradation.
- Chapter 6: This chapter shows a defect-centric analysis of the timezero variability and the time-dependent variability.
- Chapter 7: Finally, conclusions and future works are presented in this chapter.

Chapter 2

Principal Channel Hot Carrier Degradation Models in Short Devices

The four principal models used for explaining the CHC degradation in short devices are described in this chapter. A very good review of these models can be found in [4]. All these models emerged from the necessity of explaining and understanding the CHC degradation in short devices, where the field-driven paradigm is not longer valid.

2.1 Hess model

Originally, this model was developed to understand and simulate the absorption and desorption processes of the hydrogen/deuterium from passivated Si interfaces [30, 31, 32]. The main contribution of this model is the introduction of the acceleration integral (AI). As we explained before, the peak of ΔN_{it} does not coincide with the $E_{lat,max}$, either with other macroscopical quantities, such as the average carrier density and dynamic temperature [4, 28, 29]. The behaviour of the ΔN_{it} peak is better explained by the AI, which represents the cumulative ability to dissociate bonds [4]. The Hess model introduces the use of the AI for representing the SP and MP mechanisms. The bond rupture process provoked by a single particle is caused by the excitation of bonding electrons to an antibonding state; therefore, a repulsive force is induced over the H atom, generating its release [4]. This mechanism is called AB process, whose AI has the form [4, 30, 31, 32] (see Fig. 2.1).

$$R_{SP} \sim \int_{E_{TH}}^{\infty} F(E) P(E) \sigma(E) dE, \qquad (2.1)$$

where R_{SP} is the SP rate, F(E) is the carrier flux, $\sigma(E)$ is the bond dissociation reaction cross section, P(E) is the probability of such reaction releases a H atom, and E_{TH} is the bondbreakage energy for this reaction. The carrier flux is the number of charges impinging the interface per unit area, per time, and per unit energy, and it is the result of:

$$F(E) = f(E)g(E)v(E) = DF(E)v(E),$$
 (2.2)

where f(E) is the carrier distribution probability, g(E) is the density-of-states (DOS), v(E) is the carrier velocity, and DF(E) is the carrier energy DF.

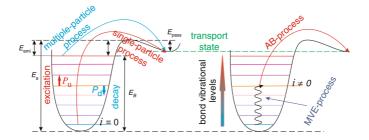


Figure 2.1: Left: SP and MP mechanisms, which are represented by the truncated harmonic oscillator. Right: schematic of the analogous AB and MVE processes. Figure taken from [4].

The Hess model also introduce the concept of the multiple vibrational excitation (MVE) of the bond associated to the MP mechanism (see Fig. 2.1). This process is triggered when a series of cold carriers excite the electron bond until its rupture. The AIs of the MVE process are related to the rates of excitation (P_u) and deexcitation (P_d) processes, which are explained by the truncated harmonic oscillator model for representing the Si-H bond (see Fig. 2.1). These AIs have the following expressions [4]:

$$P_d \sim \int_{E_{TH}}^{\infty} I(E) \sigma_{ab}(E) \left(1 - f_{ph}(E - \hbar\omega)\right) dE, \qquad (2.3)$$

$$P_u \sim \int_{E_{TH}}^{\infty} I(E) \sigma_{emi}(E) \left(1 - f_{ph}(E - \hbar\omega)\right) dE, \qquad (2.4)$$

where I(E) is the carrier flux bombarding the bond, σ_{ab} and σ_{emi} are the cross sections for the phonon absorption and emission reactions, and f_{ph} is the level occupation number, which follows the Bose-Einstein distribution. Note that $\hbar\omega$ is the distance between the levels of the oscillator (see Fig. 2.1). The ratio between P_d and P_u represents the MP process rate and has the following expression [4]:

$$R_{MP} = \left(\frac{E_B}{\hbar\omega}\right) \left[P_d + exp\left(\frac{-\hbar\omega}{k_BT}\right) \left(\frac{P_u + \omega_e}{p_d + exp\left(\frac{-\hbar\omega}{k_BT}\right)}\right) \right],\tag{2.5}$$

where E_B is the energy level of the last bonded state, ω_e is the inverse of the phonon life-time, and k_B is the Boltzmann constant [4].

One of the most important advantages of the Hess model is that it takes into account the multiple combinations of MVE and AB processes. For example, a bond electron can be excited by multiple cold carriers to a medium level, and then a SP with enough energy (and with less energy than a SP excited from the ground state) can break the bond. With this consideration, the total bond-breakage rate is [4]:

$$R = \sum_{i=0}^{N_l} \left(\frac{I_{DS} f_v + \omega_e exp\left(\frac{-\hbar\omega}{k_B T}\right)}{I_{DS} f_v + \omega_e} \right)^i A^i I_{DS} f_d, \qquad (2.6)$$

where f_v , f_d , and A^i are empirical parameters used to introduce the macroscopical parameter I_{DS} . This model has some shortcomings [4]:

- The life-time is computed as the time when ΔN_{it} achieves a threshold value, giving not correct estimations.
- The ΔN_{it} generation is not well connected to macroscopical quantities.

2.2 Rauch and La Rosa model (energy driven paradigm model)

Rauch and La Rosa changed the driven force paradigm of CHC degradation in short devices from the electric field to the carrier energy [4, 12, 33, 34, 35]. They showed that carrier energy plays an important role during CHC degradation. Following this paradigm, they suggested that the SP mechanism in short devices is due to the EES mechanism. In short channel devices, the probability of having a SP mechanism is close to zero, but according to this model, the EES mechanism changes this picture because it is able to provoke SP mechanisms [4, 33, 35]. In addition, the EES mechanism populates the tails of the carrier energy DF and enhances the CHC degradation when T increases.

The AI used in this model has the following form:

$$AI \sim \int DF(E)S(E)dE,$$
 (2.7)

where DF(E) is the carrier energy DF and S(E) is the cross section of the corresponding reaction. As DF(E) decreases rapidly and S(E) increases with a power law, the product of both functions shows two maxima (see Fig. 2.2), which can be related to empirical parameters such as stress voltages instead of carrier energies. In this way, the computational time decreases significantly.

The main shortcoming of this model is that it does not take into account the defect generation, which excludes the microscopic level of the CHC degradation.

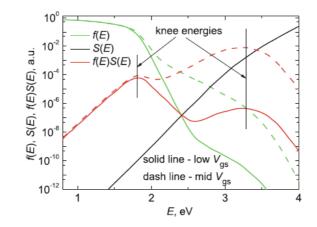


Figure 2.2: A sketch of the cross section function (S(E)), the carrier energy density function, (DF(E)), in the plot f(E), and the product of both function (DF(E)S(E)). Figure taken from [4].

2.3 Bravaix model

The Bravaix model divides the CHC degradation mechanism in three independent modes. For the formulation, the Bravaix group uses the concept of lifetime instead of computing the carrier energy DF. These life-times are related to macroscopical parameters through empirical factors [5, 37]. This model introduces the necessity of studying the carrier transport in order to correctly describe the physics of the three modes [5, 16, 36]. These modes are explained below.

1. The SP mechanism is activated when there are high average carrier energies. In this case the lifetime is [37, 38, 4]:

$$\frac{1}{\tau_{SP}} \sim \left(\frac{I_{DS}}{W}\right) \left(\frac{I_{BS}}{I_{DS}}\right)^m,\tag{2.8}$$

where W is the device width and $m \sim 2.7$ is an empirical factor.

2. The EES mechanism is activated when the flux and energy of the carriers are in an intermediate regime. The lifetime for this mode is [37, 38, 4]:

$$\frac{1}{\tau_{EES}} \sim \left(\frac{I_{DS}}{W}\right)^2 \left(\frac{I_{BS}}{I_{DS}}\right)^m,\tag{2.9}$$

3. The MP process is activated when the channel carrier flux is high and the average of the carrier energy is low. In this mode, the Si-H bond is described as a truncated harmonic oscillator as in the Hess model [5, 36]. Here, the lifetime is:

$$\frac{1}{\tau_{MP}} \sim \left[(qV_{DS} - \hbar\omega)^{1/2} \left(\frac{I_{BS}}{W} \right) \right]^{\frac{E_B}{\hbar\omega}} exp\left(\frac{-E_{emi}}{k_B T} \right)$$
$$\simeq \left[V_{DS}^{1/2} \left(\frac{I_{BS}}{W} \right) \right]^{\frac{E_B}{\hbar\omega}},$$
(2.10)

where E_{emi} is the emission energy.

The device lifetime is the weighted combination of the three lifetimes as follows:

$$\frac{1}{\tau_d} = \frac{K_{SP}}{\tau_{SP}} + \frac{K_{EES}}{\tau_{EES}} + \frac{K_{MP}}{\tau_{MP}},\tag{2.11}$$

where τ_d is the device lifetime and K_{SP} , K_{EES} , and K_{MP} are parameters related to the probability of having a SP, EES or MP mechanisms. Following the Hess model, the Bravaix group arrives to the following system of differential equations [5]:

$$\frac{dn_0}{dt} = P_d n_1 - P_u n_o, (2.12)$$

$$\frac{dn_i}{dt} = P_d(n_{i+1} - n_i) - P_u(n_i - n_{i-1}), \qquad (2.13)$$

$$\frac{dn_N}{dt} = P_u n_{N-1} - P_d \Delta N_{it} [H^*], \qquad (2.14)$$

where $[H^*]$ is the concentration of released hydrogen and n_0 , n_i , and n_N represent the occupation densities of the ground state, the *i*th level, and the last level, respectively. We can see that this model does not take into account combinations of MP and SP as the Hess model. The P_u and P_d rates are calculated with empirical parameters related to I_{DS} , reducing the computing time significantly. Another important advantage of this model is its ability to explain the temperature behaviour of the CHC degradation in short channel devices. In this case, the EES mechanism enhances the degradation process because it populates the tail of the carrier energy DF [5, 16].

Finally, the model has two important shortcomings [4]:

- The three modes are considered independent, which is not true because the carrier energy DF changes with respect to the stress time. In consequence, the weighted parameters must change. Therefore, a self-consistent model is necessary.
- In the newest version of the model [40], the authors say that the EES mechanism is overestimated but there is

some experimental evidence that shows the opposite [13].

2.4 Tyaginov and Bina model

The Tyaginov and Bina model solves the Boltzmann transport equation (BTE) in order to compute the carrier energy DF. In this way, the principal novelty of this model is the introduction of the transport perspective for the CHC degradation. The earlier version of the model uses the stochastic Boltzmann transport equation solver MONJU, which is based on Montecarlo methods [4, 13, 18]. The result of this simulation is the carrier energy DF for each discretized channel coordinate and for each stress time [4]. The DF is the input of the next module, which uses a simplified approach for solving the BTE. For this purpose, the MiniMOS simulator is used, which is based on the energy transport (ET) and drift-diffusion (DD) schemes [4]. The result of this step is the calculation of the principal characteristics of the degraded device. The AIs, used in the MONJU simulator, have the following form [4]:

$$AI_{SP/MP}^{(e/h)} = \int_{E_{TH}}^{\infty} f^{(e/h)}(E)g^{(e/h)}(E)\sigma_{SP/MP}^{(e/h)}(E)v(E)dE,$$
(2.15)

where $f^{(e/h)}(E)$ is the carrier DF for electrons/holes, $g^{(e/h)}(E)$ is the DOS, v(E) is the group velocity, and $\sigma_{SP/MP}^{(e/h)}(E)$ is the Keldysh-like reaction cross section for the SP/MP mechanism. The model takes into account all possible combinations between AB (SP mechanism) and MVE (MP mechanism) processes, as the Hess model [4, 13, 18]. For instance, a cold carrier can excite the Si-H bond to an intermediate state and then, a SP can break the bond through an AB process. All these combinations are considered independent and weighted by probability coefficients [4, 13]. With all these considerations, there were two shortcoming with respect to this earlier version [4]:

- This model considers the combinations of SP and MP mechanisms independent. It is necessary a self-consistent point of view of these mechanisms.
- It is not possible to simulate short channel devices (L < 100nm) due to some restrictions in the MiniMOS simulator. The simplified vision of the ET and DD schemes precludes a good accuracy between experimental and simulated data.

The new model version uses the deterministic Boltzmann transport equation solver ViennaSHE. Previously, the device

structure is simulated by using Sentaurus Process, which is coupled with the ViennaSHE simulator [4, 13, 18]. This simulator takes into account some energy exchange mechanisms like: surface scattering, scattering at ionized impurities, impact ionization, electron-phonon scattering and EES [4, 13, 18]. Moreover, the model is able to simulate dipole moment interactions with the oxide electric field [4, 13]. As in the Hess model, all possible combinations between AB and MVE processes are considered, but in a self-consisted way. This means that these mechanisms compete to release the H atom in order to obtain a Si dangling bond [4, 13, 18]. In this model the AI for the AB process is:

$$AI_{AB}^{(e/h)} = \int_{E_{TH}}^{\infty} f^{(e/h)}(E)g^{(e/h)}(E)\sigma(E)v(E)dE, \qquad (2.16)$$

where

$$\sigma(E) = \begin{cases} \sigma_0 (E - E_{th})^{11} & \text{if } E \ge E_{TH} \\ 0 & \text{if } E < E_{TH}, \end{cases}$$
(2.17)

where σ_0 is an attempt frequency. In the same way, the AI for the MVE process is:

$$AI_{AB}^{(e/h)} = \int_{E_{TH}}^{\infty} f^{(e/h)}(E) g^{(e/h)}(E) \sigma_0(E - \hbar\omega) v(E) dE, \quad (2.18)$$

Following the truncated harmonic oscillator model for representing the Si-H bond, a system of coupled differential equations (similar to equations (2.12), (2.13) and (2.14)) is obtained [4]. This system can be reduced to a single differential equation in order to compute N_{it} :

$$\frac{dN_{it}}{dt} = (N_0 - N_{it})\Re - N_{it}^2\beta,$$
(2.19)

where N_0 is the number of initial interface states, \Re is the cumulative bond breakage rate, and β is the Arrhenius term for the thermal activation, which has the form:

$$\beta = \nu_p exp\left(\frac{-E_{pass}}{K_B T}\right),\tag{2.20}$$

where ν_p is the attempt rate and E_{pass} is the pass energy (see Fig. 2.1). Eq. (2.19) shows that the CHC degradation increases the ΔN_{it} generation rate [4, 18].

This model is able to simulate, with very good accuracy with experimental data, the CHC degradation in long and short channel devices, as we can see in Ref. [4, 18]. As well, it is possible to analyse the contribution of each transport mechanism in the device degradation [13, 18]. Finally, the main shortcoming is related to the computing resources required for a single simulation [4].

Chapter 3

Experimental and Analytical Tools for Studying the Channel Hot Carrier Degradation under the Defect-Centric Point of View

The principal experimental and analytical tools, used in the present work, are studied in this chapter. First, we start with the principal CHC measurement techniques and then, we describe the defect-defect centric distribution.

3.1 Principal channel hot carrier measurement techniques

3.1.1 I-V stress

In this technique, the initial V_{TH0} is measured from a complete $I_{DS} - V_{GS}$ characteristic with a $V_{DS} = 50mV$. Then, the gate and drain terminals are stressed. This stress condition is interrupted several times in order to measure complete $I_{DS} - V_{GS}$ curves in order to extract a new V_{TH} (after stress) [41]. The V_{TH} shift is extracted as follows:

$$\Delta V_{TH} = V_{TH0} - V_{TH}. \tag{3.1}$$

We can see some typical $I_{DS} - V_{GS}$ characteristics for several stress times in Fig. 3.1. At the end, we obtain one ΔV_{TH} for each stress time. The principal shortcoming of this technique is that the recoverable degradation component is not well measured due to the time needed for taking a complete $I_{DS} - V_{GS}$ curve [41]. This effect is stronger in BTI measurements while is weak in CHC experiments due to the permanent nature of the degradation (the generated interface traps are permanent).

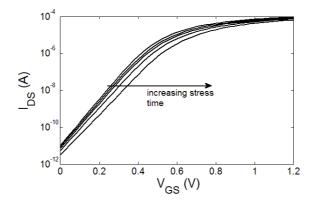


Figure 3.1: $I_{DS} - V_{GS}$ characteristics for several stress times. We can see that the characteristic curve moves to the right when the stress time increases, showing an increment of V_{TH} . In the I-V stress technique, the V_{TH} is extracted from the complete curve.

3.1.2 Measure-Stress-Measure (MSM) technique

Firstly, a complete $I_{DS} - V_{GS}$ characteristic is measured without any stress. Then, a logarithmic stress pulse is applied to the drain and gate terminals as we can see in Fig. 3.2 [41]. The part of the pulse related to the stress increases logarithmically while the time where the measurement is done (sense) is constant with $t_{sense} = 0.5s$ in our experiments. During the stress time, the drain and gate terminals are set to $V_{Gstress}$ and $V_{Dstress}$ (these values depend on the experiment). During the sense time, we apply $V_{Gsense} = 0.5V$ (close to V_{TH}) and $V_{Dsense} = 0.05V$ and we measure I_{DS} . These I_{DS} measurements are transformed into ΔV_{TH} values by projecting them into the initial $I_{DS} - V_{GS}$ curve (measured before applying the stress pulse) as we show in Fig. 3.3. This technique enables us to measure the recoverable component of the degradation [41].

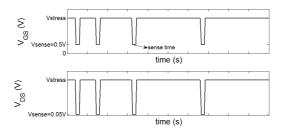


Figure 3.2: An example of a logarithmic stress pulse of the MSM technique. Top: the stress pulse for the gate terminal. Bottom: the stress pulse for the drain terminal. In this case, $V_{Gsense} = 0.5V$ and $V_{Dsense} = 0.05V$.

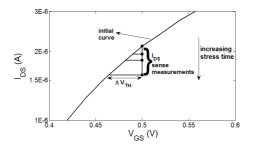


Figure 3.3: In the MSM technique, during the sense time, the I_{DS} current is measured several times according to the logarithmic pulse (square dots). These values are projected into the initial $I_{DS} - V_{GS}$ curve in order to extract the ΔV_{TH} value.

3.2 The defect-centric distribution

It is well known that the V_{TH} shift generated by a single charge follows an exponential distribution with mean value η [42, 43, 44]. The principal expressions for this distribution are: [20, 44]:

$$f_{\eta}(\Delta V_{TH}) = \frac{1}{\eta} exp\left(\frac{\Delta V_{TH}}{\eta}\right), \qquad (3.2)$$

$$F_{\eta}(\Delta V_{TH}) = 1 - exp\left(\frac{\Delta V_{TH}}{\eta}\right), \qquad (3.3)$$

where f_{η} and F_{η} are the probability density function and the cumulative function, respectively. If we consider *n* of these single defects in a device (*device level*), we have that the total ΔV_{TH} is equal to the convolution of the *n* individual exponential distributions [20, 44]. In this case, we have:

$$g_{\eta,n}(\Delta V_{TH}) = \frac{\Delta V_{TH}^{(n-1)}}{\eta^n (n-1)!} exp\left(\frac{\Delta V_{TH}}{\eta}\right), \qquad (3.4)$$

$$G_{\eta,n}(\Delta V_{TH}) = 1 - \frac{1}{(n-1)!} \Gamma(n, \Delta V_{TH}/\eta),$$
 (3.5)

where $g_{\eta,n}$ is the probability density function, $G_{\eta,n}$ is the cumulative function and Γ is the Gamma function. The total number of traps, in several devices (*chip level*), are Poisson distributed with mean value N_t [45, 46, 47]. In this case, the probability density function is:

$$P_{N_t}(n) = \frac{exp(-N_t)N_t^n}{n!}.$$
(3.6)

Hence, the total ΔV_{TH} in a chip is the sum of $G_{\eta,n}$ weighted by $P_{N_T}(n)$ [20, 44]:

$$H_{\eta,N_t}(\Delta V_{TH}) = \sum_{n=0}^{\infty} \frac{e^{-N_t} N_t^n}{n!} G_{\eta,n}(\Delta V_{TH})$$
(3.7)

or

$$H_{\eta,N_t}(\Delta V_{TH}) = \sum_{n=0}^{\infty} \frac{e^{-N_t} N_t^n}{n!} \left[1 - \frac{\Gamma(n, \Delta V_{TH}/\eta)}{(n-1)!} \right], \quad (3.8)$$

where H_{η,N_t} is the cumulative function of the defect-centric distribution. The advantage of using the DCD is that its first and second moments are related to physical parameters as follows [19, 20, 21, 53]:

$$\langle \Delta V_{TH} \rangle = N_t \eta, \qquad (3.9)$$

$$\sigma^2 = 2N_t \eta^2. \tag{3.10}$$

where $\langle \Delta V_{TH} \rangle$ is the expected value of ΔV_{TH} and σ^2 is the distribution variance. Finally, for computing the cumulative distribution of the experimental ΔV_{TH} data, it is necessary to sort them and then, apply a ranking algorithm. In our case, we have used the Benard approximation [48]:

$$H(i) = \frac{i - 0.3}{n + 0.4}.$$
(3.11)

where i is the position of a sorted experiment and n is the total number of experiments.

Chapter 4

Study of the Geometry Device Dependence of the Defect-Centric Parameters

In this chapter, we study the dependence of principal defectcentric parameters with respect to the device geometry. We show that the DCD explains very well the CHC degradation behaviour. As well, we demonstrate that the CHC degradation strongly depends on the channel length and weakly depends on the device width.

4.1 Defect-centric distribution of experimental data of CHC-induced ΔV_{TH}

Fig. 4.1 shows the experimental data and their fittings with the DCD of 50 CHC degradation experiments for several stress times. The MSM technique was used over bulk planar nMOS-FETS with an effective channel length (L_{eff}) of 100nm, W =85nm and a gate dielectric of 1.8nm of SiON [49]. The stress conditions were: $V_{Gstress} = V_{Dstress} = 2.0V$, which represents the most degrading CHC stress condition for short channel devices. The sense voltages were: $V_{Gsense} = 0.5V$ and $V_{Dstress} = 50mV$ (see Fig. 3.2) [49]. In the x - axis, we have the CHC-induced threshold voltage shift values for several times, and in the y - axis, we have the cumulative distribution, H(i), in probit scale. For computing H(i), we have used the Bernard ranking algorithm (see eq. 3.11). In these experiments, we can see that the DCD fits very well from -2σ to 2σ .

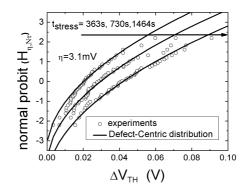


Figure 4.1: Distributions of the CHC-induced ΔV_{TH} for several stress times. We can see that η is constant and the variation of $\langle \Delta V_{TH} \rangle$ is only due to the increment of N_t . In this case: $V_{Gstress} = V_{Dstress} = 2V$.

In Fig. 4.1, we can see that the defect-centric parameter η (related to the second moment) is constant with respect to the stress time and the increment of $t < \Delta V_{TH} >$ is directly related to the increase of N_t , according to eq. (3.9). This can be seen in Fig. 4.2, where N_t and t_{stress} follow a power law with exponent 0.45, which agrees well with the typical values for CHC degradation (0.4 ~ 0.6) [5, 6, 11]. In addition, this value shows that the principal degradation mechanism is the generation of interface traps according to Ref. [11]. Note that

the DCD takes into account the traps formed at the interface and those generated in the oxide [21, 49].

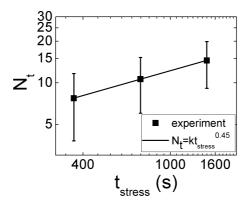


Figure 4.2: N_t increases with respect to t_{stress} . The exponent of the power law $N_t = t^n$ is 0.45.

Figures 4.3 and 4.4 show more fittings of CHC degradation experiments with the DCD for several stress times. In these cases, the tests were done on nMOSFETs processed in 45nmand 65nm bulk planar CMOS commercial technologies [50]. We have performed 160 experiments per technology. The channel width is $1\mu m$ for both processes and the effective channel lengths are 37nm and 50nm for the 45nm and 65nm technologies, respectively. The gate dielectric consists of 1.85nm of SiON. In this case, we use the I - V technique for the CHC degradation measurements. The stress conditions are: $V_{Gstress} = 1.1V$ and $V_{Dstress} = 1.8V$ for the 45nm technology, and $V_{Gstress} = 1.2V$ and $V_{Dstress} = 1.8V$ for the 65nm technology [50]. We can see that the DCD fits very well with the experimental data up to 3σ [50].

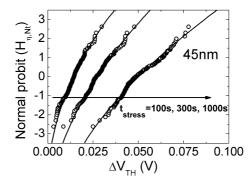


Figure 4.3: CHC-induced ΔV_{TH} follows a DCD in 45nm commercial technology. In this case: $V_{Gstress} = 1.1V$ and $V_{Dstress} = 1.8V$.

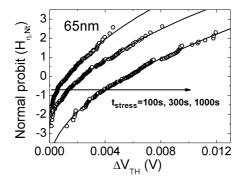


Figure 4.4: CHC-induced ΔV_{TH} follows a DCD in 65nm commercial technology. In this case: $V_{Gstress} = 1.2V$ and $V_{Dstress} = 1.8V$.

4.2 Length and width dependences of the defect-centric parameters

For studying the channel length dependence of the defect-centric parameters, we take into account the effective length (L_{eff} , which represents only the channel length of a device), instead of the total length (L, which takes into account the channel length and the overlaps). We have extracted the defect-centric parameters for three different L_{eff} : 120nm, 70nm and 40nm. For these cases, the device width is 90nm (constant). For the width dependence, we have chosen four different W: 70nm, 85nm, 100nm and 200nm with a constant $L_{eff} = 100nm$. For both groups of experiments, the gate stack consists of 1.8nm of SiON. We have used the MSM stress technique with the same stress conditions for both groups: $V_{Gstress} = V_{Dstress} = 2V$. The sense voltages were: $V_{Gsense} = 0.5V$ and $V_{Dsense} = 50mV$ with a $t_{sense} = 0.5s$. The defect centric parameters: η and N_t were extracted from the first and second moment of the DCD by applying eq. (3.9) and .eq. (3.10).

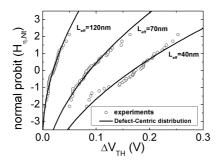


Figure 4.5: ΔV_{TH} for different L_{eff} and same W = 90nm. The first and second moments strongly decrease with L_{eff} .

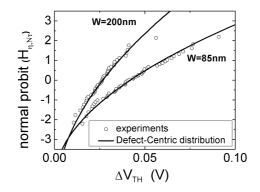


Figure 4.6: ΔV_{TH} for different W and same $L_{eff} = 100nm$. The first and second moments weakly decrease with W.

Figures 4.5 and 4.6 show the ΔV_{TH} distributions for different L_{eff} and W. We can see that the DCD has stronger dependence on L_{eff} than W. In both cases, η (second moment of the DCD) decreases with L_{eff} and W, whereas the first moment ($\langle \Delta V_{TH} \rangle$) strongly increases with L_{eff} and weakly increases with W; this can also be seen in Fig. 4.7. These tendencies are better explained in Fig. 4.8, where η is plotted in function of the effective area (A_{eff}), and in Fig. 4.9, where the number of traps is shown in function of the studied dimension. Fig. 4.8 shows that η is inversely proportional to A_{eff} and, therefore, to L_{eff} and W. The same result has been reported for BTI degradation in [21, 51]. Fig. 4.9 shows that N_t decreases with L_{eff} and increases with W. In one hand, we have that $\langle \Delta V_{TH} \rangle$ and σ strongly decrease with the increment of L_{eff} due to the diminution of η and N_t . On the other hand, we have that $\langle \Delta V_{TH} \rangle$ and σ weakly decrease with the increment of W because the diminution of η is partiality compensated by the increment of W.

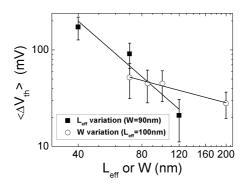


Figure 4.7: $\langle \Delta V_{TH} \rangle$ as function of L_{eff} or W. The expected value of ΔV_{TH} strongly decreases with L_{eff} and weakly decreases with W.

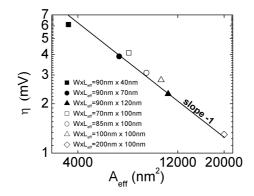


Figure 4.8: η scales as $1/A_{eff}$.

In Fig. 4.10, we plot the density of traps, $D_t = N_t/A_{eff}$, in function of L_{eff} or W. We can see that D_t strongly decreases with L_{eff} due to the higher lateral electrical field applied during the CHC degradation. The weak increment of D_t with respect to W can be attributed to some process related non-uniformities of the gate dielectrics along the shallow trench isolation edge [52] and it explains the soft decrement of $\langle \Delta V_{TH} \rangle$ when W increases. In BTI degradation, it has been reported that D_t is constant [21, 53]; therefore, the BTI-induced ΔV_{TH} does not change with respect to L_{eff} and W. Thus, this strong change

of $< \Delta V_{TH} >$ with respect to L_{eff} is the signature of the CHC mechanism.

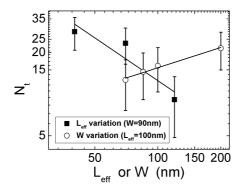


Figure 4.9: N_t as function of L_{eff} or W. N_t decreases with L_{eff} and increases with W.

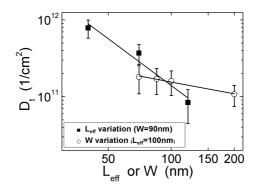


Figure 4.10: D_t as function of L_{eff} or W. D_t strongly decreases with L_{eff} and slightly decreases with W.

Chapter 5

A Defect-Centric Analysis of the Temperature Dependence of the Channel Hot Carrier Degradation

In this chapter, we study the temperature dependence of the defect-centric parameters, η and N_t . The experiments were carried out in bulk planar nMOSFETs with W = 90nm and $L_{eff} = 40nm$. The gate stack consists of 1.8nm of SiON. The temperature range varies from $25^{\circ}C$ to $150^{\circ}C$ in steps of $25^{\circ}C$. We performed 30 experiments per temperature, giving a total population of 180 devices. For generating the CHC stress, we have used the MSM technique with the following conditions:

 $V_{Dstress} = V_{Gstress} = 1.6V$ (maximum damage condition) and $V_{Dsense} = 50mV$ and $V_{Gsense} = 0.5V$. In order to compare results, we perform CHC stress measurements in wider devices $(W = 1\mu m, L_{eff} = 40nm)$ with the same stress conditions.

5.1 Temperature dependence of the defectcentric parameters

Fig. 5.1 shows the ΔV_{TH} distribution for several temperatures. We can see that experimental data fits well with the DCD. According to Fig. 5.1 and Fig. 5.2, $\langle \Delta V_{TH} \rangle$ increases with T in agreement with previous CHC experiments [5, 6, 7, 16]. This tendency can be explained by the activation of the EES mechanism which is dominant at high energies in the carrier energy DF, according to Bravaix model [5, 16]. In order to understand the physics of microscopic mechanisms for explaining these macroscopic results, we have extracted the defect centric parameters in function of the studied temperature range.

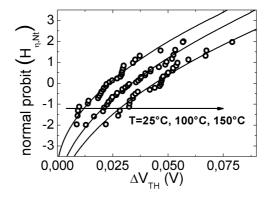


Figure 5.1: CHC-induced ΔV_{TH} distribution for several temperatures. All experiments agree well with the DCD. We can see that $\langle \Delta V_{TH} \rangle$ increases with T.

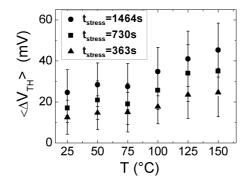
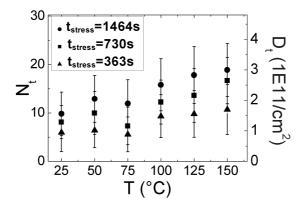


Figure 5.2: The expected value of the CHC induced V_{TH} shift increases with T in agreement to the activation of the EES mechanism.

On one hand, Fig. 5.3 shows that the total number of traps, N_t , and the density of traps D_t increase with T. On the other hand, Fig. 5.4 shows that η is independent of the temperature. It is important to mention that the temperature independence of η has also been reported for BTI degradation [54]. These two results show that the increment of the CHC degradation with respect to T (measured on the increase of $\langle \Delta V_{TH} \rangle$) is ascribed to the higher number of generated defects and not to the higher impact of defects on V_{TH} . This physical interpretation agrees well with the enhancement of the defect generation due



to the activation of the EES mechanism [16, 18].

Figure 5.3: N_t increases as function of T. On the right axis, D_t is plotted.

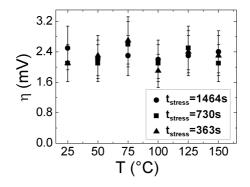


Figure 5.4: η is independent of *T*.

During the the CHC stress, the oxide close to the drain terminal is affected by CHC degradation mechanisms, whereas the oxide close to the source terminal experiences the cold carrier injection due to the high oxide electric field, resulting in a positive bias temperature instability (PBTI) degradation. In order to study the contribution of the PBTI component in the total device degradation, we have performed PBTI measurements in the short devices with the same stress condition on the gate terminal. We have obtained a $\Delta V_{TH} \simeq 1.25mV$ for a $t_{stress} = 1464s$ at $T = 125^{\circ}C$; therefore, the PBTI contribution can be neglected in comparison with the CHC component. Thus, the observed temperature dependence is only ascribed to CHC degradation.

5.2 Extraction of the activation energy

Fig. 5.5 shows the Arrhenius plot of N_t for several stress times. We have extracted an average value of $\simeq 58meV$ for the E_{ACT} , which is similar to that obtained in BTI degradation ($E_{ACT} \simeq 60meV$) [54]. The extracted E_{ACT} is related to the following empirical expression [54]:

$$N_t \propto exp\left(\frac{-E_{ACT}}{k_BT}\right) \left(\frac{V_{GS} - V_{TH0}}{t_{ox}}\right) t_{stress}^n, \tag{5.1}$$

where t_{ox} is the oxide thickness, and V_{TH0} is the initial threshold voltage measured before applying the stress. According to the DCD and our experimental results, we have that: $\langle V_{TH} \rangle = \eta N_t$ and η is constant; therefore, $\langle V_{TH} \rangle$ also follows an empirical rule like eq. (5.1). In Fig. 5.6, we show the Arrhenius plot of $\langle \Delta V_{TH} \rangle$ for small devices (90nm x 40nm) and wider devices (1 μ m x 40nm). The activation energies (E_{ACT}) are very similar for both geometries and close to the value calculated for N_t (small devices: $E_{ACT} \simeq 53meV$ and wider devices: $E_{ACT} \simeq 56 meV$).

Finally, in order to calculate the activation energy related to the failure time, in Appendix A, we have shown that both activation energies are related by:

$$\langle E_{A_{capture}} \rangle = \frac{1}{n} E_{ACT},$$
 (5.2)

where $\langle E_{A_{capture}} \rangle$ is the activation energy related to the failure time, and n is the exponent of the power law: $N_t = Kt^n$ (which is in the range 0.4 \sim 0.6 for CHC degradation). In our experiments, we have found that $\langle E_{A_{capture}} \rangle = 0.117 eV$, where an extracted n = 0.45 was used.

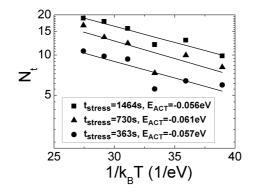


Figure 5.5: Arrhenius plot of $\langle \Delta V_{TH} \rangle$ for small and large devices. For both geometries, similar values of E_{ACT} are obtained.

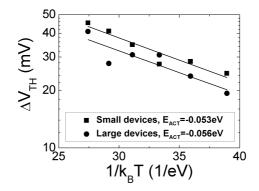


Figure 5.6: Arrhenius plot of N_t for several stress times. E_{ACT} values are similar to those obtained for BTI degradation.

Chapter 6

A Defect-Centric Study of the Channel Hot Carrier Variability

In this chapter, we begin studying the principal variability concepts. Then, we perform an analysis, based on the DCD, in order to study the dependence of $\langle \Delta V_{TH} \rangle$ with respect to the drain voltage and stress time. Finally, the time-zero variability and the time-dependent variability of the CHC degradation are studied.

6.1 Variability concepts

The mismatch of a parameter X measured in a pair of matching devices is defined by [9]:

$$\delta X = X_A - X_B,\tag{6.1}$$

where δX is the mismatch of the parameter X, and X_A and X_B are measurements of the X parameter on devices A and B, respectively. In this chapter, we study the mismatch of:

- i) the initial threshold voltage measured before applying the stress or time-zero mismatch: $\delta V_{TH0} = V_{TH0_A} V_{TH0_B}$, and
- ii) the threshold voltage shift measured after applying the CHC stress or time-dependent mismatch: $\delta \Delta V_{TH} = \Delta V_{TH_A} \Delta V_{TH_B}$.

We use the following nomenclature: δ denotes the difference between paired devices and Δ denotes a CHC-induced shift in one device. The total mismatch of V_{TH} after stress is the sum of the time-zero mismatch and the time-dependent mismatch [9]:

$$\delta V_{TH} = \delta V_{TH0} + \delta \Delta V_{TH}. \tag{6.2}$$

Thus, there are two sources of fluctuations for computing δV_{TH} : fluctuations related to V_{TH0} (pristine devices or timezero) and fluctuations due to CHC (time-dependent) [9]. The variance of δV_{TH} can be computed by [9]:

$$\sigma_{\delta V_{TH}}^2 = \sigma_{\delta V_{TH0}}^2 + \sigma_{\delta \Delta V_{TH}}^2 + 2\rho \sigma_{\delta V_{TH0}} \sigma_{\delta \Delta V_{TH}}, \qquad (6.3)$$

where $\sigma_{\delta V_{TH}}^2$ is the variance of the total V_{TH} mismatch, $\sigma_{\delta V_{TH0}}^2$ is the variance of the time-zero mismatch, $\sigma_{\delta \Delta V_{TH}}^2$ is the variance of the time-dependent mismatch and ρ is the correlation factor between time-zero fluctuations and time-dependent fluctuations. Note that the variability is defined as the standard deviation of the mismatch [9].

In addition, there are two kind of sources of variability: systematic (or extrinsic) and random (or intrinsic) [55, 56]. Systematic sources are process related and affect the real values of the extracted parameters. In this perspective, the time-zero variability has been well-studied in deeply-scaled very-large-scale integration (VLSI) technologies. For example, in Ref. [57] the timezero threshold voltage (V_{TH0}) distribution has been studied up to 5.4 σ on 11 billions of transistors. As result, this distribution is assumed to be normal with mean value $\langle V_{TH0} \rangle$ and variance $\sigma_{V_{TH0}}$ [57]. The random component of $\sigma_{V_{TH0}}$ scales with respect to the area, as follows [58, 59, 60]:

$$\sigma_{V_{TH0},int}^2 = \frac{K_{V_{TH0}}^2}{A},$$
(6.4)

where $K_{V_{TH0}}$ is a scaling parameter, A is the device area, and the sub-index *int* represents the intrinsic (random) component. The time-dependent variability has also been studied under the defect-centric framework in Ref. [55, 56], where the use of matching pair devices (MPD) enables to extract the random component of the time-dependent variability as follows (see Appendix B for the demonstration) [50, 55, 56]:

$$\sigma_{\Delta V_{TH},int}^2 = \frac{\sigma_{\delta \Delta V_{TH}}^2}{2}.$$
(6.5)

The same approach can be applied to the time-zero variability [55, 56]:

$$\sigma_{V_{TH0},int}^2 = \frac{\sigma_{\delta V_{TH0}}^2}{2},$$
(6.6)

Thus, the total variance of the CHC-induced ΔV_{TH} is:

$$\sigma_{\Delta V_{TH}}^2 = \sigma_{\Delta V_{TH},int}^2 + \sigma_{\Delta V_{TH},ext}^2, \tag{6.7}$$

where the sub-index *ext* is used for representing the extrinsic variability component. In the defect-centric framework, we have that η^2 is directly proportional to the variance of the CHCinduced ΔV_{TH} distribution: $\sigma^2_{\Delta V_{TH}} = 2N_t \eta^2$. Therefore, the total η also has two components:

$$\eta = \eta_{int} + \eta_{ext},\tag{6.8}$$

where η_{int} is considered the *correct* value. In this context, for studying the time-dependent variability, we use the defectcentric parameter, η , instead of $\sigma_{\Delta V_{TH}}$.

6.2 Experimental results

The experiments were carried on two groups of nMOSFETs processed in 45nm and 65nm bulk planar commercial technologies. For both technologies, the width is $1\mu m$ and the effective channel lengths are estimated to be 37nm and 50nm for the technologies of 45nm and 65nm, respectively. The gate stack consists of 1.85nm of SiON. The I - V technique was used for generating the CHC stress with the following conditions:

• 45*nm* technology: $V_{Dstress} = 1.7V$, 1.8V and 1.9V, $V_{Gstress} = 1.1V$

• 65nm technology: $V_{Dstress} = 1.8V$, 2.0V, 2.2V and 2.4V, $V_{Gstress} = 1.2V$

The measurements were done over 80 MPD for each stress configuration, giving an overall population of more than 1000 samples.

6.2.1 Drain voltage and stress time dependences

As we mentioned in previous sections, N_t follows a power law with respect to t_{stress} with an exponent in the range $0.4 \sim 0.6$. If we consider that η is constant with respect to t_{stress} (as we show in section 4.1), and by using the defect-centric expression: $\langle \Delta V_{TH} \rangle = N_t \eta$, we have that $\langle \Delta V_{TH} \rangle$ should also follow a power law with respect to t_{stress} with an exponent in the same range as N_t . This tendency can be seen in Figs. 6.1 and 6.2. In these plots, the average slope is ~ 0.55 [50]. Moreover, we have also found the same tendency for the $V_{Dstress}$ dependence, where $\langle \Delta V_{TH} \rangle$ follows a power law with respect to $V_{Dstress}$ with a slope of ~ 12.5 , as we can see in Figs. 6.3 and 6.4 [50].

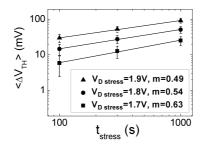


Figure 6.1: The expected value of the CHC-induced ΔV_{TH} follows a power law with respect to t_{stress} with an average slope of ~ 0.55 for the 45nm technology.

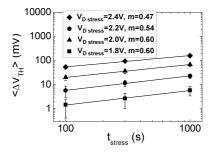


Figure 6.2: The expected value of the CHC-induced ΔV_{TH} follows a power law with respect to t_{stress} with an average slope of ~ 0.55 for the 65nm technology.

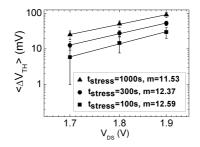


Figure 6.3: The expected value of the CHC-induced ΔV_{TH} follows a power law with respect to $V_{Dstress}$ with an average slope of ~ 0.12 for the 45nm technology.

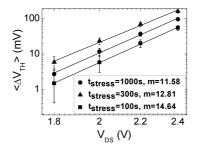


Figure 6.4: The expected value of the CHC-induced ΔV_{TH} follows a power law with respect to $V_{Dstress}$ with an average slope of ~ 0.13 for the 65nm technology.

6.2.2 Time-zero variability

Fig. 6.5 shows the distribution of V_{TH0} in a normal probit scale (NP) for both technologies. We can see that V_{TH0} follows a normal distribution up to 3σ in pristine devices in agreement with Ref. [57]. Fig. 6.6 shows the distribution of the mismatch of V_{TH0} for both technologies. We can see that the variability of the 45nm technology is higher than the 65nm technology, in agreement with the scaling rule $1/A_{eff}$ (see equation (6.4)) [56]. As well, the δV_{TH0} data follows a normal distribution up to 3σ . Fig. 6.7 shows the total and the intrinsic time-zero variabilities. We have extracted the intrinsic variability by applying equation (6.6). As we expected, the intrinsic (random) variability is lower than the total one.

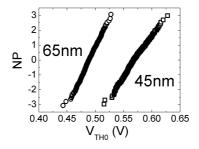


Figure 6.5: The time-zero V_{TH0} follows a normal distribution up to 3σ for both technologies.

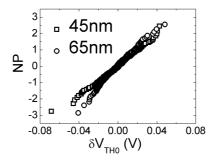


Figure 6.6: The time-zero mismatch follows a normal distribution up to 3σ for both technologies.

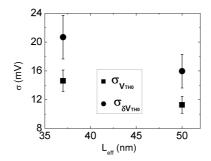


Figure 6.7: Total and intrinsic time-zero variabilities in function of the effective channel length for both technologies.

6.2.3 Time-dependent variability

Figs. 6.8 and 6.9 show the ΔV_{TH} mismatch for both technologies. We can see that the variability increases with t_{stress} due to the increment of $\langle \Delta V_{TH} \rangle$ (see Fig. 6.1 and Fig. 6.2). In addition, these mismatch data follow a normal distribution up to 3σ .

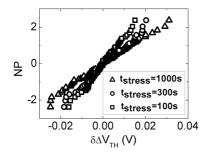


Figure 6.8: The time-dependent mismatch follows a normal distribution up to 3σ for several stress times in 45nm technology.

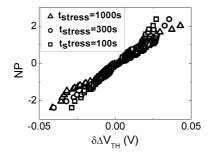


Figure 6.9: The time-dependent mismatch follows a normal distribution up to 3σ for several stress times in 65nm technology.

In Figs. 6.10 and 6.11 we can see that η is practically independent of the stress time in single devices (total η) and in MPD (intrinsic or correct η); whereas in Figs. 6.12 and 6.13, we can see the independence of η (total and intrinsic) with respect to $V_{Dstress}$. Here, we have used equation (6.5) for extracting the intrinsic values of η . As we expected, a lower time-dependent variability is obtained in MPD in function of t_{stress} and $V_{Dstress}$.

We can observe that the 45nm technology exhibits a higher time-dependent variability than the 65nm technology. This is ascribed to the scaling rule $\eta \propto 1/A_{eff}$ reported in section 4.2. In BTI degradation η is in the range: $\eta_0 \leq \eta \leq 2\eta_0$ with:

$$\eta_0 = \frac{q}{C_{ox}},\tag{6.9}$$

where q is the elementary charge and C_{ox} is the oxide capacitance. We can see in figures 6.10, 6.11, 6.12 and 6.13 that the extracted values of η are higher than the BTI range. This occurs because of the *non uniform* degradation region formed during CHC stress [50, 55]. Thus, the value of η can increase or decrease with respect to stress parameters, depending on the *lateral extend* and the *magnitude* of the degraded region [50, 55].

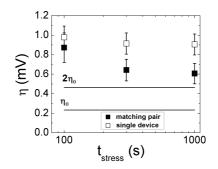


Figure 6.10: The time-dependent variability is practically independent of the stress time in 45nm technology.

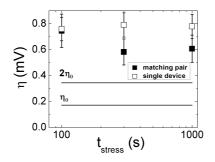


Figure 6.11: The time-dependent variability is practically independent of the stress time in 65nm technology.

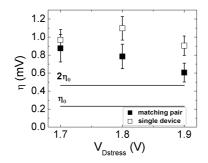


Figure 6.12: The time-dependent variability is practically independent of the drain voltage in 45nm technology.

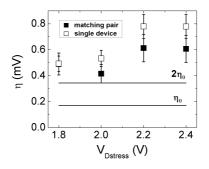


Figure 6.13: The time-dependent variability is practically independent of the drain voltage in 65nm technology.

Chapter 7

General Conclusions and Future Work

7.1 Conclusions

The CHC degradation under the defect-centric point of view has been studied. Particularly, we have analysed the behaviour of the defect-centric parameters: η , N_t and $\langle V_{TH} \rangle$ under the variation of different parameters: L_{eff} , W, t_{stress} , $V_{Dstress}$ and T. In addition, we have studied the variability of the defectcentric parameters by using MPD. For generating the CHC stress, we have used the I - V and MSM techniques. In total we have performed more than 1400 experiments.

We have demonstrated that the DCD is able to describe well the experimental data of the CHC degradation up-to 3σ . We have showed that $\langle V_{TH} \rangle$ and N_t follow a power law with respect to t_{stress} with an exponent in the range of $0.45 \sim 0.55$, which coincide with typical values for CHC degradation. One of the most important results we have found, is the following scaling rule: $\eta \propto 1/A_{eff}$, which coincides with BTI degradation. As well, $\langle V_{TH} \rangle$ strongly increases with the diminution of L_{eff} and weakly increases with the diminution of W. In addition, N_t decreases with L_{eff} and increases with W; whereas D_t (normalized N_t) strongly decreases with L_{eff} and weakly decreases with W. Below, we can find the explanations for these tendencies:

- For the W dependence: when W increases, the decrement of η is partially compensated by the increment of N_t , given a weakly decrement of $\langle V_{TH} \rangle$ with respect to W.
- For the L_{eff} dependence: when L_{eff} increases, the decrement of η is strengthened by the decrement of N_t , given a strong decrement of $\langle V_{TH} \rangle$ with respect to W. Note that this L_{eff} dependence is the most important difference between CHC and BTI degradations.

In the temperature experiments, we have found that η is independent of T as in BTI degradation. As well, N_t and $\langle V_{TH} \rangle$ increase with respect to T in agreement with the activation of the electron-electron scattering mechanism, which populates the tails of the carrier energy density function and enhances the defect generation. This increment of defects exhibits an activation energy of about 60mV, which coincides with BTI experiments.

Finally, we have studied the time-zero variability and the timedependent variability. For the time-zero variability, we have showed that V_{TH} and δV_{TH0} follow a normal distribution up to 3σ . As well, the 45nm technology exhibits more time-zero variability than the 65nm technology in agreement with the scaling rule $\sigma^2_{V_{TH0}} \propto 1/A_{eff}$. In the time-dependent variability experiments, we have shown that the total η and the intrinsic η are independent of t_{stress} and $V_{Dstress}$. As well, we have found that the 45nm technology has more variability than the 65nmtechnology in concordance with the scaling rule $\eta \propto 1/A_{eff}$.

7.2 Future work

• In order to determine the percentage of interface traps, charge pumping experiments could be performed after each

stress time. This will enable us to confirm the basic theory that the interface states are predominant in CHC degradation.

- It would be very interesting to perform CHC experiments in high- κ metal gate devices. In these devices, it would be necessary to separate the natural high density of oxide traps from those generated at the interface by the CHC stress.
- As well, It would be interesting to implement CHC experiments at high T in high-κ metal gate devices. In these devices the BTI component cannot be neglected and both degradations (CHC and BTI) will be present.

Appendix A

Activation Energy Conversion

According to experimental results, $\langle \Delta V_{TH} \rangle$ follows a power law in function of t_{stress} . If we consider the temperature, the empirical rule can be written as:

$$<\Delta V_{TH}> = Kexp\left(\frac{-E_{ACT}}{k_BT}\right)t_{stress}^n,$$
 (A.1)

where K is a constant, n is an exponent in the range $0.4 \sim 0.5$ for CHC experiments, and E_{ACT} is the activation energy extracted from the typical curve $\langle \Delta V_{TH} \rangle$ vs. T. With this equation, the stress time can be calculated by:

$$t_{stress} = \left(\frac{\langle \Delta V_{TH} \rangle}{Kexp\left(\frac{-E_{ACT}}{k_BT}\right)}\right)^{\frac{1}{n}}.$$
 (A.2)

One of the typical criterion for computing the failure time in CHC degradation is when a $\langle \Delta V_{TH} \rangle = 30mV$ is obtained. If we replace this criterion in eq. (A.2), we have:

$$t_{failure} = \left(\frac{K_1}{Kexp\left(\frac{-E_{ACT}}{k_BT}\right)}\right)^{\frac{1}{n}}.$$
 (A.3)

where $K_1 = 30mV$ and $t_{failure}$ is the failure time. Finally, we obtain:

$$t_{failure} = \left(\frac{K_1}{Kexp\left(\frac{-E_{ACT}}{k_BT}\right)}\right)^{\frac{1}{n}} = \left(\frac{K_1}{K}\right)^{\frac{1}{n}}exp\left(\frac{E_{ACT}}{k_BT}\right)^{\frac{1}{n}},$$
(A.4)

$$log\left(t_{failure}\right) = \frac{1}{n}log\left(\frac{K_1}{K}\right) + \frac{E_{ACT}}{n}\frac{1}{k_BT}.$$
 (A.5)

Therefore, $E_{A_{capture}} = \frac{E_{ACT}}{n}$. The relation of both activa-

tion energies is also explained in Fig. A.1.

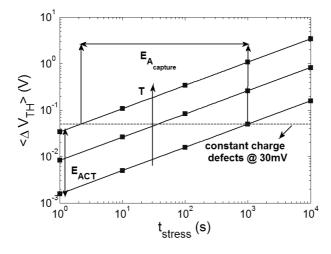


Figure A.1: In this simulated plot of $\langle \Delta V_{TH} \rangle$ vs. t_{stress} , we can see the difference between both activation energies. In this case the exponent of the power law is 0.5.

Appendix B

Conversion between the Variances of Single Device Experiments and Matching Pairs Experiments

The mismatch of a parameter X, measured in MPD, is:

$$\delta X = X_A - X_B. \tag{B.1}$$

Then, the variance of δX is:

$$var(\delta X) = var(X_A - X_B) = var(X_A) + var(X_B) - 2cov(X_A, X_B).$$
(B.2)

By considering that X_A and X_B are statistically independent dent and equally distributed, we have: $cov(X_A, X_B) = 0$ and $var(X_A) = var(X_B)$, therefore:

$$var(\delta X) = 2var(X_A) = 2var(X).$$
(B.3)

Finally,

$$var(X) = \frac{var(\delta X)}{2}.$$
 (B.4)

Bibliography

- C. Hu, Lucky electron model for channel hot electron emission, presented at IEEE Proceedings of the International Electron Devices Meeting (IEDM), pp. 22 - 25, 1979.
- [2] S. Tam, P. K. Ko, and C. Hu, Lucky-electron model of channel hot electron rejection in MOSFET'S, IEEE Transactions on Electron Devices, vol. 31, pp. 1116 - 1125, 1984.
- [3] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, K. W. Terril, *Hot-electron-induced MOSFET degradation-Model*, *monitor, and improvement*, IEEE Transactions on Electron Devices, vol. 32, pp. 375 - 385, 1985.
- [4] S. Tyaginov, Physics-Based Modeling of Hot-Carrier Degradation, in Hot Carrier Degradation in Semiconductor Devices, 1st. ed. Switzerland.

- [5] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. M. Roux, E. Vincent, *Hot-Carrier acceleration factors for low power* management in DC-AC stressed 40nm NMOS node at high temperature, presented at IEEE International Reliability Physics Symposium (IRPS), pp. 531 - 548, 2009.
- [6] E. Amat, T. Kauerauf, R. Degraeve, R. Rodriguez, M. Nafria, X. Aymerich, G. Groeseneken, A comprehensive study of Channel Hot-Carrier degradation in short channel MOSFETs with high-k dielectrics, Microelectronic Engineering, vol. 103, pp. 144 149, 2013.
- [7] E. Amat, T. Kauerauf, R. Degraeve, R. Rodriguez, M. Nafria, X. Aymerich, G. Groeseneken, *Channel hot-carrier degradation in pMOS and nMOS short channel transistors with high-k dielectric stack*, Microelectronic Engineering, vol. 87, pp. 47 50, 2010.
- [8] E. Amat, R. Rodríguez, M.B. González, J. Martín-Martínez, M. Nafría, X. Aymerich, P. Verheyen, E. Simoen, *CHC degradation of strained devices based on SiON and high-k gate dielectric materials*, Microelectronic Engineering, vol. 88, pp. 1408 - 1411, 2011.

- [9] P. Magnone, F. Crupi, N. Wils, R. Jain, H. Tuinhout, P. Andricciola, G. Giusi, C. Fiegna, *Impact of Hot Carriers on nMOSFET Variability in 45 nm and 65 nm CMOS Technologies*, IEEE Transactions on Electron Devices, vol. 58, pp. 2347 2353, 2011.
- [10] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, C. Fiegna, *Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region*, IEEE Transactions on Electron Devices, vol. 59, pp. 2093 - 2099, 2012.
- [11] M. Cho, Ph. Roussel, B. Kaczer, R. Degraeve, J. Franco, M. Aoulaiche, T. Chiarella, T. Kauerauf, N. Horiguchi, G. Groeseneken, *Channel Hot Carrier Degradation Mechanism in Long/Short Channel n-FinFETs*, IEEE Transactions on Electron Devices, vol. 60, pp. 4002 - 4007, 2013.
- [12] S. E. Rauch, G. La Rosa, The energy-driven paradigm of NMOSFET hot-carrier effects, IEEE Transactions on Device and Materials Reliability, vol. 5, pp. 701 - 705, 2005.
- [13] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, B. Kaczer, T. Grasser, On the importance of electron-electron scattering for hot-carrier degradation, Japanese Journal of Applied Physics, vol. 54, pp. 04DC18-1 - 04DC18-5, 2015.

- [14] J. H. Sim, B. H. Lee, R. Choi, S.-C. Song, G. Bersuker, *Hot Carrier Degradation of HfSiON Gate Dielectrics With TiN Electrode*, IEEE Transactions on Device and Materials Reliability, vol. 5, pp 177 - 182, 2005.
- [15] A. Tallarico, M. Cho, J. Franco, R. Ritzenthaler, M. Togo, N. Horiguchi, G. Groeseneken, F. Crupi, Impact of the Substrate Orientation on CHC Reliability in n-FinFETs-Separation of the Various Contributions, IEEE Transactions on Device and Materials Reliability, vol. 14, pp. 52 -56, 2014.
- [16] A. Bravaix, V. Huard, D. Goguenheim, E. Vincent, Hotcarrier to cold-carrier device lifetime modeling with temperature for low power 40nm Si-bulk NMOS and PMOS FETs, presented at IEEE International Electron Devices Meeting (IEDM), pp. 27.5.1 - 25.7.4, 2011.
- [17] F. C. Hsu and K.-Y. Chu, Temperature Dependence of Hot-Electron Induced Degradation in MOSFETs, IEEE Electron Device Letters, vol. 5, pp. 148 - 150, 1984.
- M. Bina, S. Tyaginov, J. Franco, Y. Wimmer, D. Osinstev,
 B. Kaczer, T. Grasser, *Predictive Hot-Carrier Modeling of*

n-channel MOSFETs, IEEE Transactions on Electron Devices, vol. 61, pp. 3103 - 3110, 2014.

- [19] B. Kaczer, T. Grasser, Ph. J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, H. Reisinger, Origin of BTI Variability in Deeply Scaled pFETs, presented at IEEE International Reliability Physics Symposium (IRPS), pp. 26 - 32, 2010.
- [20] B. Kaczer, Ph. J. Roussel, T. Grasser, G. Groeseneken, Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices-Application to BTI, IEEE Electron Device Letters, vol. 31, pp. 411 - 413, 2010.
- [21] M. Toledano-Luque, B. Kaczer, J. Franco, Ph.J. Roussel, M. Bina, T. Grasser, M. Cho, P. Weckx, and G. Groeseneken, *Degradation of time dependent variability due to interface state generation*, presented at Symposium on VLSI Technology (VLSIT), pp. T190 T191, 2013.
- [22] D. Angot, V. Huard, L. Rahhal, A. Cros, X. Federspiel, A. Bajolet, Y. Carminati, M. Saliva, E. Pion, F. Cacho, A. Bravaix, BTI variability Fundamental understandings and Impact on digital logic by the use of extensive dataset,

presented at IEEE International Electron Devices Meeting (IEDM), pp. 15.4.1 - 15.4.4, 2013.

- [23] C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post, S. Bodapati, M. Giles, S. Gupta, S. Mudanai, *Bias Temperature Instability* Variation on SiON/Poly, HK/MG and Trigate Architectures, presented at IEEE International Reliability Physics Symposium (IRPS), pp. 6A.5.1 - 6A.5.7, 2014.
- [24] E. R. Hsieh, Steve S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, C. W. Liang, New Observations on the Physical Mechanism of Vth-Variation in Nanoscale CMOS Devices After Long Term Stress, presented at IEEE International Reliability Physics Symposium (IRPS), pp. XT.9.1 - XT.9.2, 2011.
- [25] S. S. Chung, The Process and Stress-Induced Variability Issues of Trigate CMOS Devices, presented at IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp. 1 - 2, 2013.
- [26] C.H. Tu, S.Y. Chen, A.E. Chuang, H.S. Huang, Z.W. Jhou, C.J. Chang, S. Chou, J. Ko, *Transistor variability after*

CHC and BTI stress in 90 nm pMOSFET technology, Electronics Letters, vol. 45, pp. 854 - 856, 2009.

- [27] C. Liu, K. T. Lee, S. Pae, and J. Park, New Observations on Hot Carrier induced Dynamic Variation in Nano-scaled SiON/Poly, HK/MG and FinFET devices based on Onthe-fly HCI Technique: The Role of Single Trap induced Degradation, presented at IEEE International Electron Devices Meeting (IEDM), pp. 34.6.1 - 34.6.4, 2014.
- [28] I. A. Starkov, S.E. Tyaginov, H. Enichlmair, J. Cervenka, Ch. Jungemann, S. Carniello, J.M. Park, H. Ceric, T. Grasser, *Hot-carrier degradation caused interface state profile - simulations vs. experiment*, Journal of Vacuum Science & Technology B, vol. 29, pp. 01AB09-1 - 01AB09-8, 2011.
- [29] I. Starkov, H. Enichlmair, S. Tyaginov, T. Grasser, Analysis of the threshold voltage turnaround effect in high-voltage n-MOSFETs due to hot-carrier stress, presented at IEEE International Reliability Physics Symposium (IRPS), pp. XT.7.1 - XT.7.6, 2012.
- [30] W. McMahon, K. Matsuda, J. Lee, K. Hess, J. Lyding, *The* effects of a multiple carrier model of interface states gen-

eration of lifetime extraction for MOSFETs, presented at Proceedings of the International Conference on Modelling and Simulation Micro, vol. 1, pp. 576 - 579, 2002.

- [31] W. McMahon, A. Haggag, K. Hess, *Reliability scaling is-sues for nanoscale devices*, IEEE Transaction on Nanotechnology, vol. 2, pp. 33 38, 2003.
- [32] K. Hess, L.F. Register, B. Tuttle, J. Lyding, I.C. Kizilyalli, Impact of nanostructure research on conventional solidstate electronics: The giant isotope effect in hydrogen desorption and CMOS lifetime, Physica E, vol. 3, pp. 1 - 7, 1998.
- [33] S. E. Rauch, G. La Rosa, F.J. Guarin, Role of E-E scattering in the enhancement of channel hot carrier degradation of deep-submicron NMOSFETs at high Vgs conditions, IEEE Transactions on Device and Materials Reliability vol. 1, pp. 113 - 119, 2001.
- [34] S. Rauch, G. La Rosa, The energy driven paradigm of NMOSFET hot carrier effects, presented at IEEE International Reliability Physics Symposium (IRPS)International Reliability Physics Symposium (IRPS), pp. 708 - 709, 2005.

- [35] S. Rauch, F. Guarin, G. La Rosa, Impact of E-E Scattering to the Hot Carrier Degradation n Deep Submicron NMOS-FETs, IEEE Electron Device Letters, vol. 19, pp. 463 - 465, 1998.
- [36] C. Guerin, V. Huard, A. Bravaix, General framework about defect creation at the Si/SiO2 interface, Journal of Applied Physics, vol. 105, pp. 114513-1 - 114513-12, 2009.
- [37] C. Guerin, V. Huard, A. Bravaix, *The energy-driven hot-carrier degradation modes of nMOSFETs*, IEEE Transactions on Device and Materials Reliability, vol. 7, pp. 225 235, 2007.
- [38] C. Guerin, V. Huard, A. Bravaix, *The energy-driven hot carrier degradation modes*, presented at IEEE Proceedings of the International Reliability Physics Symposium (IRPS), pp. 692 693, 2007.
- [39] A. Bravaix, V. Huard, D. Goguenheim, E. Vincent, Hotcarrier to cold-carrier device lifetime modeling with temperature for low power 40nm Si-Bulk NMOS and PMOS FETs, presented at IEEE International Electron Devices Meeting (IEDM), pp. 622 - 625, 2011.

- [40] Y. M. Randriamihaja, X. Federspiel, V. Huard, A. Bravaix, P. Palestri, New hot carrier degradation modeling reconsidering the role of EES in ultra short n-channel MOSFETs, presented at IEEE Proceedings of the International Reliability Physics Symposium (IRPS), pp. 1 - 5, 2013.
- [41] M. Aoulaiche, Bias temperature instabilities in MOSFETs with high-k dielectrics and metal gates, Ph.D. dissertation, Departement Elektrotechnieka, Katholieke Universiteit Leuven, Leuven, Belgium, 2009.
- [42] M. F. Bukhori, S. Roy, and A. Asenov, Simulation of statistical aspects of reliability in nano CMOS, presented at IEEE International Integrated Reliability Workshop (IRW), pp. 82 - 85, 2009.
- [43] A. Ghetti, C. M. Compagnoni, A. S. Spinelli, A. Visconti, Comprehensive analysis of random telegraph noise instability and its scaling in deca-nanometer Flash memories, IEEE Transactions on Electron Devices, vol. 56, pp. 1746 -1752, 2009.
- [44] M. Toledano-Luque, B. Kaczer, J. Franco, Ph.J. Roussel, T. Grasser, G. Groeseneken, *Defect-centric perspective of*

time-dependent BTI variability, Microelectronics Reliability, vol. 52, pp. 1883 - 1890, 2012.

- [45] S. E. Rauch, Review and reexamination of reliability effects related to NBTI statistical variations, IEEE Transactions on Device and Materials Reliability, vol. 7, pp. 524 - 530, 2017.
- [46] V. Huard, C. Parthasarathy, C. Guerin, T. Valentin, E. Pion, M. Mammasse, N. Planes, L. Camus, *NBTI degradation: From transistor to SRAM arrays*, presented at IEEE Proceedings of the International Reliability Physics Symposium (IRPS), pp. 289 - 300, 2008.
- [47] B. Kaczer, T. Grasser, J. Martin-Martinez, E. Simoen, M. Aoulaiche, P. J. Roussel, and G. Groeseneken, NBTI from the perspective of defect states with widely distributed times, presented at IEEE Proceedings of the International Reliability Physics Symposium (IRPS), pp. 55 - 60, 2009.
- [48] T. Kauerauf, Degradation and breakdown of MOS gate stacks with high permittivity dielectrics, Ph.D. dissertation, Departement Elektrotechnieka, Katholieke Universiteit Leuven, Leuven, Belgium, 2007.

- [49] L. M. Procel, F. Crupi, J. Franco, L. Trojman, B. Kaczer, Defect-Centric Distribution of Channel Hot Carrier Degradation in Nano-MOSFETs, IEEE Electron Device Letters, vol. 35, pp. 1167 - 1169, 2014.
- [50] L. M. Procel, F. Crupi, J. Franco, L. Trojman, B. Kaczer, N. Wils, H. Tuinhout, A Defect-Centric perspective on channel hot carrier variability in nMOSFETs, Microelectronic Engineering, vol. 147, pp. 72 - 74, 2015.
- [51] J. Franco, B. Kaczer, M. Toledano-Luque, Ph. J. Roussel, J. Mitard, L.-A. Ragnarsson, L. Witters, T. Chiarella, M. Togo, N. Horiguchi, G. Groeseneken, *Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs*, presented at IEEE Proceedings of International Reliability Physics Symposium (IRPS), pp. 5A.4.1 5A.4.6, 2012.
- [52] M. Toledano-Luque, B. Kaczer, T. Grasser, P. Roussel, J. Franco, G. Groeseneken, From mean values to distributions of BTI lifetime of deeply scaled FETs through atomistic understanding of the degradation, presented at Symposium on VLSI Technology (VLSIT), pp. 152 - 153, 2011.

- [53] M. Toledano-Luque, B. Kaczer, J. Franco, Ph.J. Roussel, T. Grasser, T.Y. Hoffmann, G. Groeseneken, *Toward a streamlined projection of small device BTI lifetime distributions*, Journal of Vacuum Science and Technology B, vol. 31, pp. 01A114, 2013.
- [54] J. Franco, B. Kaczer, Ph. J. Roussel, M. Toledano-Luque, P. Weckx, *Relevance of non-exponential singledefect-induced threshold voltage shifts for NBTI Variability*, presented at IEEE International Integrated Reliability Workshop (IRW), pp. 69 - 72, 2013.
- [55] B. Kaczer, J. Franco, M. Cho, T. Grasser, Ph. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. De Keersgieter, T. Chiarella, N. Horiguchi1, G. Groeseneken, A. Thean, *Origins and Implications of Increased Channel Hot Carrier Variability in nFinFETs*, presented at IEEE International Reliability Physics Symposium (IRPS), pp. 3B.5.1 3B.5.6, 2015.
- [56] B. Kaczer, J. Franco, Ph. J. Roussel, G. Groeseneken, T. Chiarella, N. Horiguchi, T. Grasser, Extraction of The Random Component of Time-Dependent Variability Using

Matched Pairs, IEEE Electron Device Letters, vol. 36, pp. 300 - 302, 2015.

- [57] T. Mizutani, A. Kumar, T. Hiramoto, Analysis of transistor characteristics in distribution tails beyond ±5.4σ of 11 billion transistors, presented at IEEE International Electron Devices Meeting (IEDM), pp. 33.3.1 - 33.3.4, 2013.
- [58] M. J. M. Pelgrom, A. C. J. Duinmaijer, A. P. G. Welbers, *Matching Properties of MOS Transistors*, IEEE Journal of Solid-State Circuits, vol. 24, pp. 1433 - 1439, 1989.
- [59] C. M. Mezzomo, A. Bajolet, A. Cathignol, R. Di Frenza, G. Ghibaudo, *Characterization and Modeling of Transistor Variability in Advanced CMOS Technologies*, IEEE Transactions on Electron Devices, vol. 58, pp. 2235 - 2248, 2011.
- [60] A. Kerber, Methodology for Determination of Process Induced BTI Variability in MG/HK CMOS Technologies Using a Novel Matrix Test Structure, IEEE Electron Device Letters, vol. 35, pp. 294 - 296, 2014.