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Random Telegraph Signal in CMOS Single Photon Avalanche Diodes

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Abstract

This dissertation is focused on single photon devices that have triggered a real revolution in the world of imaging, the Single Photon Avalanche Diodes (SPADs). These devices acquired immediately a great interest in the field of single photon imaging, since they showed great performances in several fields, such as quantum mechanics, optical fibres, fluorescent decays and luminescence in physics, chemistry, biology, medical imaging, etc. These applications require single photon detectors able to assure high performances in photon counting, such as high photon detection efficiency, high speed and extremely low noise detection. The interest on SPAD became wider as they have been implemented in Complementary Metal-Oxide Semiconductor (CMOS) technology, reaching the integration of quenching and post-processing circuits on the pixel itself. The high timing and spatial resolution, the low power performance, the easy integration of circuits made CMOS SPADs the best choice in the field of single photon detectors. The ability to detect individual photons with very high timing resolution, at the order of few tens of picoseconds, and with an internal gain of 10^6 allowed to reduce the complexity in amplification circuit.

However, SPAD performance is also influenced by Dark Count Rate (DCR), i.e. no-photon induced count rate, and by Random Telegraph Signal (RTS) occurrence, i.e. DCR discrete fluctuations. DCRs are mainly due to defects introduced in the semiconductor lattice and in the oxide during the fabrication process. In addition, radiation environment can induce new defects in the silicon structure, knows as radiation-induced defects. These defects or cluster of defects create new energy levels in the bandgap and cause the generation of carriers in depletion regions through thermal processes (Shockley Read-Hall, SRH, processes) and tunneling processes. This results in the increase of the mean dark current and in RTS. An

increased occurrence of RTS effects degrades the performances of the devices, since the randomisation of this signal makes impossible to calibrate correctly the device. Therefore, it is important to investigate RTS behaviour and recognize the defects involved in this mechanism. The identification of defects responsible for RTS and the understanding of its evolution could be very useful to limit the effects on the devices operating in radiation environment.

The thesis is structured in four chapters.

The first chapter introduces the semiconductor-based photodetectors, the evolution of these devices until to CMOS Single-Photon Counting Detectors (SPADs). SPADs are described in detail, by explaining the working principle and the associated electronic circuits. SPAD performances are also discussed, taking into consideration the crosstalk and the afterpulse.

The second chapter explains the mechanisms responsible for DCR increase and RTS occurrence, focusing on generated electron-hole pairs due to thermal trap-assisted transition or to trap-assisted tunnelling (TAT) and band-to-band tunnelling (BTBT) at high electric field. RTS phenomenon is described and several theoretical models to explain its origin are presented in this chapter.

The third chapter describes SPADs device investigated in the experimental analysis, focusing on two different layouts implemented in the test-chip: P+/Nwell and Pwell/Niso layout. The experimental setup and SPAD characterization before irradiation is reported.

The fourth chapter describes the proton irradiation test and presents the experimental RTS data and the evolution in frequency and time domain. The chapter reports also the experimental results obtained by RTS investigation on two different SPAD layouts. The results allowed to hypothesize an explanation involved in RTS phenomenon.

1. Photon Detectors in CMOS Technology

Introduction

In the last decade a great interest has been focused on photons detection techniques due to its large employment in different fields, such as Fluorescence Lifetime Imaging Microscopy (FLIM), Time Of Flight (TOF) imaging, biomedical imaging (Positron Emission Tomography, PET), etc. [1, 2]. A photon detection system consists mainly in a photodetector, light sensitive device, an electronic circuit to amplify the signal and a data processing unit to manage the data [3]. When this system is used to detect an optical signal, great attention should be payed to the noise of the entire system, especially for low-level light applications, since it could alter the optical signal. In order to reach an appropriate signal detection, photodetectors able to amplify internally the photocurrent can be employed, i.e. photomultiplier tubes, microchannel plates, or avalanche diodes. However, for low-level light applications, like FLIM and PET, these sensors could not be appropriate, since these applications require very high detection sensitivity and accuracy [1]. In order to successfully detect weak signal, it is necessary to improve the detection system and to employ photodetectors able to count each single photon in the input optical signal. Photon counting detectors, such as Single Photon Avalanche Diodes (SPADs), fulfil well this requirement, since they possess very high single-photon sensitivity. Moreover, the excellent timing resolution makes them the best candidates in those applications in which the time of arrival of individual photons on detector should be known very accurately [3, 4]. One of these applications is FLIM [2, 5, 6], in which the fluorescence time allows the identification of molecules families. The fluorescence lifetime is the mean time in which the molecules go from excited to the ground state. A useful technique to determine the fluorescence lifetime is called time-correlated single photon counting (TCSPC) [2, 3]. This technique measures the decay time of the fluorescence light emitted by a sample

excited with a laser pulse. Since a sub-ns accuracy is required in these applications, single-photon counting detectors are the best solution for accurate photon detection [2, 7].

SPADs can find application even in time-of-flight (TOF) imaging [3]. TOF technique measures the distance between a sensor and an object, by evaluating the time between the emission of a signal ad its return to the sensor after the reflection on the object.

Even biomedical imaging has benefited from single-photon imaging, such as PET application. Indeed, in order to estimate the position of the two annihilation photons with excellent spatial resolution, the detection system must possess picosecond timing accuracy [8, 9, 10].

This chapter will introduce the photodetectors, focusing on the SPADs. The structure implemented in CMOS technology and the associated electronic circuits will be described in order to explain SPADs working principle and to demonstrate the excellent performances. On the other hand, noise performance will also be deepened in correlated noise sources: afterpulse and crosstalk.

1.1 Photosensor properties

Semiconductor based photosensors are able to detect optical signals and to convert the incident light in an electrical signal proportional to the light intensity [4]. The basic structure of a photodetector is a simple p-n junction reverse biased. The detection principle is based on thermoelectric or photoelectric effect. However, thermal detectors suffer from long time response in temperature change, so they do not find wide application. The photons absorbed in the depletion layer create drifting electrons and holes that are separated by the electric field and collected on the electrodes.

The operation of a general photodetector consists mainly in three processes: carrier generation (electrons and holes) coming from photon absorbed in the

semiconductor, carriers transport process and/or multiplication carriers and current extraction, coming from transport process, to provide the output signal.
However, in order to travel inside the bandgap (E_g) and generate an electron-hole pair, photon energy E_{ph} has to follow the relationship

$$E_{ph} = h\nu = \frac{hc_0}{\lambda} \geq E_g \tag{1.1}$$

with h the Planck's constant ($h = 6.623 \cdot 10^{-34} J \cdot s$), ν the frequency, λ the wavelength, c_0 the light speed in the vacuum ($c_0 = 3 \cdot 10^8\, m/s$). Only if the photons energy is greater than the bandgap energy level, the photoelectric effect occurs: photons are absorbed and e-h pairs are created in the semiconductor. Generated carriers can travel in a high electric-field and free new carriers by means of impact ionization processes.
The minimum frequency necessary for photoelectric effect is

$$\nu = \frac{E_g}{h} \tag{1.2}$$

The wavelength limit for photon detection is

$$\lambda = \frac{1.24}{E_g\ (eV)}\ \ (\mu m) \tag{1.3}$$

Moreover, an important parameter that influences the photon detection is the material absorption coefficient, μ. The photons intensity that penetrates the material decreases exponentially with the distance according to

$$I = I_0 e^{-\mu x} \tag{1.4}$$

with μ, absorption coefficient, depending by material and radiation frequency (Fig. 1.1).

The penetration depth is the inverse of absorption coefficient and it is defined as the distance in which the photon intensity decreases of $1/e$. High μ means that the photon is absorbed near the surface, while low μ means the photon can penetrate deeply in the semiconductor.

Photons with short wavelengths (UV range) will be absorbed near the surface, while photons with long wavelengths can penetrate deeper in the semiconductor. Therefore, according to wavelength of photon to detect, in the photodiode fabrication process, materials with the penetration depth of the same size of depletion regions have to be chosen.

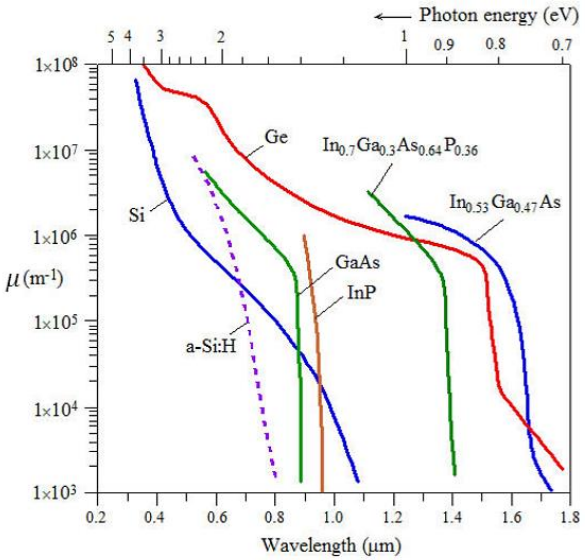


Figure 1-1. Absorption coefficient as a function of incident light wavelength for semiconductor material [11]

1.2 Avalanche photodiodes

When a p-n junction is biased with a high reverse voltage, a high electric field exists in the depletion layer of the diode. If the electric field is sufficiently high, an electron drifting in the electric field can gain enough kinetic energy to excite an

electron in the conduction band after collision, leaving a hole in the valence band. The threshold kinetic energy has to be obviously larger than the bandgap energy. This process is known as impact ionization, and it can be due even to a hole drifting. In high electric field the carriers can cause further impact ionizations and create an avalanche of carriers in the photodiode [12].

The avalanche process depends on two factors: the number of pairs generated by a carrier (carrier ionization rate), and the rate at which electrons and holes leave the high electric field region and they are collected (carrier extraction rate) [13].

When a photon is absorbed in the depletion region, the photo-generated carriers begin the carrier multiplication process, resulting in an internal gain multiplication of the photodiode and therefore, in a signal amplification. As the reverse bias voltage increases until the breakdown voltage, the ionization rate is compensated by the extraction rate, so the carrier concentration and the photocurrent increase according to a finite multiplication factor or gain, M, defined as

$$M = \left\{1 - \int_0^{W_D} \alpha_n \, exp\left[-\int_x^{W_D} \left(\alpha_n - \alpha_p\right) dx'\right] dx\right\}^{-1} \tag{1.5}$$

with W_D the depletion layer, α_n and α_p respectively the electron and hole ionization rates. For $\alpha_n = \alpha_p = \alpha$, the multiplication in high field region at $x = 0$ becomes [14]

$$M = \frac{1}{1 - \alpha W_D} \tag{1.6}$$

This multiplication process occurs in Avalanche Photodiode (APD), in which the current increases linearly to the incident light intensity with a multiplication factor between few tens and few hundreds [13]. However, when more and more carriers are generated in the multiplication region, space-charge reduces the electric field, leading to carrier avalanche extinction [4]. Therefore, APD results a linear signal amplifier but with limited amplification gain [1].

1.3 Single Photon Avalanche Diodes

When the reverse bias voltage overcomes the breakdown voltage, charge carriers in the depletion layer can create an infinite number of electron-hole pairs in a self-sustaining avalanche of carriers ($\alpha W_D = 1$) [14]. Above the breakdown voltage, the electric field is so high to overcome the space-charge effect. As a result, the ionization rate increases and it can be not compensated by the extraction rate: the carrier concentration reaches very high values. The internal gain can become infinite due to positive feedback in the avalanche multiplication and no further amplification is necessary. Biased over breakdown voltage, due to its internal amplification, the photodiode is able to detect low intensity light levels and identify the contribution to the signal of each single photon, hence the name Single Photon Avalanche Diodes (SPADs), or Geiger-mode Avalanche Photodiodes (GAPDs).

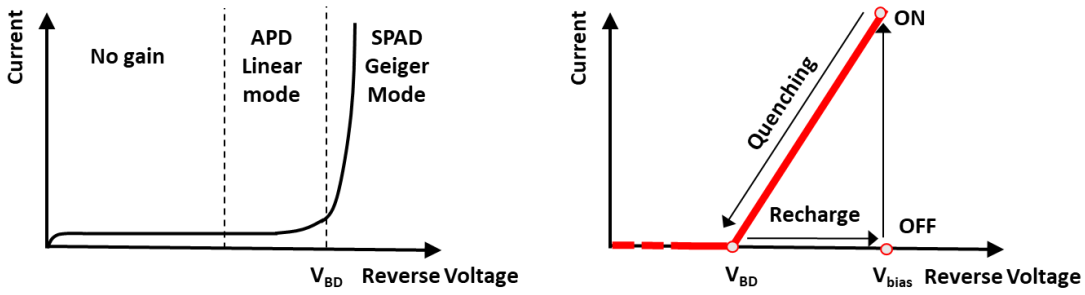


Figure 1-2. a) Current-voltage characteristic; b) Description of working processes in SPAD [1]

The avalanche current increases rapidly as shown in Fig. 1.2a, b and it would continue to increase until the destruction of the diode due to device heating [4]. Therefore, a quenching circuit that decreases the bias voltage below the breakdown voltage, is necessary to stop the self-sustaining avalanche. The electric field becomes lower and the carriers do not possess sufficient energy to trigger the avalanche. When the avalanche is quenched, the bias voltage has to be reset above

the breakdown voltage. In this way, the photodetector is ready to detect another photon [7].

1.3.1 SPAD performance parameters

First of all, in order to describe SPAD technology and its working principle, it is necessary to define some important parameters:

- Photon detection efficiency (PDE) is the ratio between the number of detected photons and the number of incident photons. In an ideal condition PDE value is 100%, but in real condition phenomena like self-reflection, absorption and self-quenching can decrease PDE:
  - photons can be reflected at device surface or at interface of many layers. An antireflection coating helps to maximize photon transmission and to minimize the material reflectance;
  - photons can be absorbed close to the surface of active region or deeper in silicon substrate;
  - an avalanche event can be triggered, but the event may not yield enough potential difference to trigger an output pulse. In this condition, the avalanche event becomes self-quenching. Higher bias voltage assures enough high electric fields to minimize self-quenching effect and to increase impact ionization [1,15].
- Time resolution (jitter) represents the precision of photon arrival time. It is defined as the spread in time between photon absorption and pulse detection by timing electronics [7]. It is quantified in standard deviation of photon arrival time distribution, or with the full-width half-maximum (FWHM) [1]. The jitter is modelled as a Gaussian distribution that represents the timing uncertainty by the statistical nature of the impact ionization process [1]. A predominantly Gaussian shape in the histogram of avalanche events

indicates that the bulk of photon triggering the avalanche occurs in high field active region detector, while a long tail means that the photons are absorbed in the neutral region and most of avalanche events are due to photon generated carriers diffusing into the high field region after a delay time [7, 13, 15].

- Dead Time is the time necessary to reset the photodetector to bias condition after avalanche quenching and in which the photodetector is not able to detect new photons. In passive quenching circuits the dead time is constituted by the time needed to quench the avalanche and the time needed to reset the detector to operative bias conditions [1]. It can occur that the photodetector is biased above breakdown voltage and it is able to detect new photons before the reset. This results in fluctuations in reset waveform [13]. In active quenching circuit, an additional hold-off time, in which the detector is insensitive to photons, has to be set in the circuit [1]. Dead time should be as short as possible, to increase the dynamic range of incident photon flux and to decrease the variations in photon counting output. Regarding this, active quenching circuits offer a better performance with short, well-defined dead time and high counting rates. However, as it will explain in Section 1.3.2 and 1.7.1, short dead time increases the afterpulsing probability [13].

Taking into consideration arrays of SPADs, other parameters, such as fill factor and pixel pitch, become important:

- Fill factor contributes to photon detection probability. It is defined as the ratio between sensitive active area and the total area of the cell. Low fill factor means the sensitive area is small, and therefore, photon detection probability decreases [7].
- Pixel Pitch (PP) is the distance between the centers of neighbouring pixels. Smaller PP means higher spatial resolution of detector, but lower fill factor.

1.3.2 Quenching circuit

Several type of quenching circuits can be employed in SPAD pixel. They can be divided in passive, active or mixed active/passive quenching circuits. The most simple passive circuit consists in a resistor in series to SPAD pixel, with a high resistance value, R_Q (100 $k\Omega$ to 1 $M\Omega$) [16]. When the SPAD current increases during the avalanche, the voltage at SPAD V_D, due to the voltage drop through the resistor, decreases until to reach V_{BD} and to quench the avalanche. After, the SPAD is restored again to V_{bias} [7].

In order to better understand SPAD operation with resistor quenching circuit, SPAD is replaced by an equivalent circuit in Fig. 1.3.

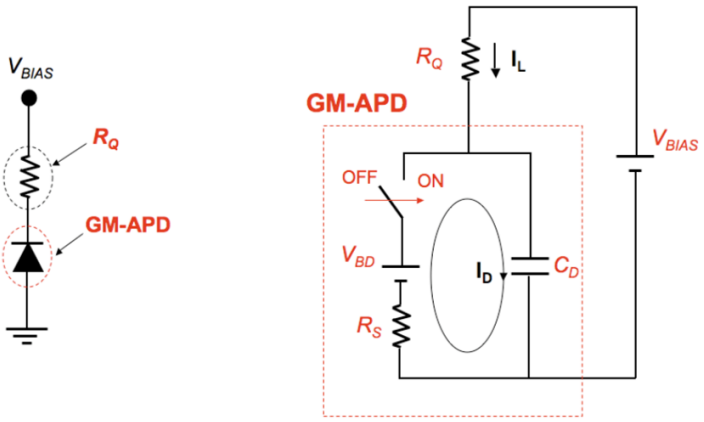


Figure 1-3. Schematic representation of SPAD with equivalent circuit [11]

SPAD, or GM-APD, is modelled by a junction transition capacity C_D, an internal resistance R_S and a DC generator to reach the breakdown voltage, V_{BD}, during the operation. If the diode is in stand-by, the circuit is open, there is no current and the capacitor is charged to V_{bias}. When a charge carrier is injected in the region, due to incident photon on the detector, the electric field related to SPAD voltage, is enough high to start a self-sustaining avalanche. The equivalent circuit closes and the capacitor is charged to V_{BD} through the internal resistor R_S.

The diode current I_D reaches the maximum value:

$$I_D = \frac{V_{BD} - V_{bias}}{R_Q} \tag{1.7}$$

The voltage V_D begins to decrease towards the following asymptotic value:

$$V_D = V_{bias} - \frac{(V_{bias} - V_{BD})R_Q}{R_Q + R_S} = V_{bias} - \frac{V_{OV}}{1 + R_S/R_Q} \tag{1.8}$$

where V_{OV} is the excess bias voltage with respect to the breakdown voltage. Since $R_Q \gg R_S$, V_D will tend to V_{bias} [11].

While V_D decreases, the lower electric field in the depletion region quenches the avalanche and the equivalent circuit is again open allowing the capacitor to recharge to V_{bias}. At the end of recharging process, GM-APD is able to detect another photon. In order to reach fast response, the diode should be quenched and recharged very rapidly. An accurate choice of R_Q value can accelerate quenching and recharging operations. R_Q has to be sufficiently high to quench the avalanche of carriers avoiding spurious pulses, but no excessively high to have a long dead time. Since during dead time the detector is not able to detect photons, a long dead time causes the decrease of the detector sensitivity [11].

Notwithstanding the passive quenching circuit appears simple and compact, for high-rate events or for afterpulsing effects, due to de-trapping of carriers after a random time (Section 1.7.1), SPAD may create a current avalanche before the complete recharge and cause spurious carriers avalanches. Therefore, it is necessary to add a delay time, hold-off time, in the circuit design to avoid distortion in the timing response [1, 17].

The active quenching circuit is able to force the quenching and recharging process in short time and with controlled bias-voltage source [17], even if it requires much large area, at the expense of fill factor. It consists in a fast comparator to insert in

the circuit, whose output forces the bias voltage source below V_{BD} after the avalanche. After an adjustable hold-off time, the bias voltage is set again to V_{bias}. Basic circuits of passive and active quenching circuits are shown respectively in Fig. 1.4a, b.

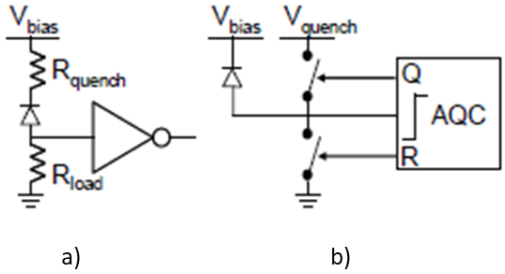


Figure 1- 4. Basic circuit of SPAD with passive a) and active b) quenching circuit [13]

The active quenching circuit benefits from fast recharge, fast transitions between quenching and recharging process and shorter and controlled avalanche time and dead time [1, 7, 17].

Another solution can be the employment of a mixing active/passive circuit in order to have lower afterpulsing probability and shorter hold-off time, even if the circuit is not so compact [1].

1.4 SPAD architectures

In order to assure high level performance, SPADs require particular attention in the design and fabrication process. A highly doped region and a thin junction are required to obtain a high electric field, while a large depletion region contributes to increase the absorption efficiency [11]. In addition, in order to prevent spurious avalanches, high purity level of semiconductor, without lattice imperfections, has to be employed in SPAD design process [1]. Finally, in order to avoid premature edge breakdown (PEB) due to high doping profile curvature near the device edge, guard rings have to be insert in the structure. Guard rings avoid even spurious

avalanche due to carrier diffusion in the active region since they separate active region from surrounding. Sometimes so called “virtual” guard rings are employed; the term “virtual” is due to the lack of real structure in the edge of device. A “virtual” guard ring is created where the graded doping profile of the retrograde deep n-well cathode implant encourages breakdown in the central active region rather than at the device periphery [18].

According to different design, SPAD can be divided in Reach-Through avalanche photodiode, in which thick substrate constitutes the absorption region, and Planar avalanche photodiode, in which only a thin layer in the substrate is used as absorption region.

One of the first Reach-Through SPAD has been developed in the early 70s by McIntre and Webb. A Reach-Trough SPAD consists in a thin $p+$ doped layer, a slightly p type doped substrate (π layer), thin p doped layer and $n+$ doped layer (Fig. 1.5) [11, 19]. In π layer the electric field is low, as shown in Fig. 1.5, while in $p-n+$ junction there is a region with high electric field.

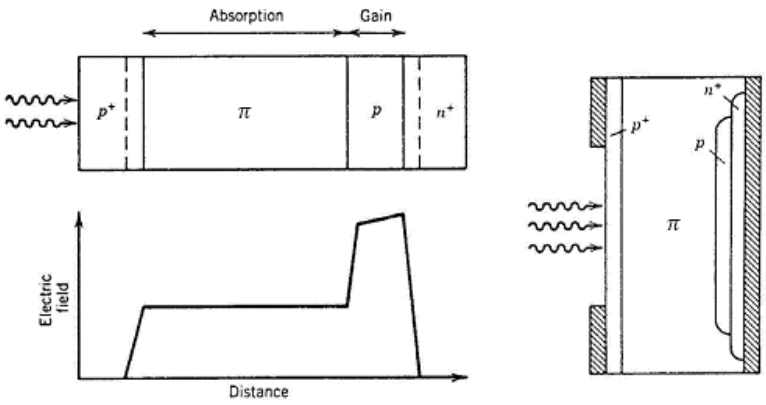


Figure 1-5. Structure of Reach-Trough SPAD [11]

When a photon hits the device, it is absorbed in the π layer, resulting in generation of free carriers. The electric field moves the carriers towards $p-n+$ junction, in which the high electric field triggers the impact ionization generating new carriers. According to different wavelength of photons to detect, the fabrication process has

to assure the employment of materials that guarantee photon absorption in π layer. In this way, the device can detect photons of specific wavelengths, according to fabrication material. The guard ring of the structure is "virtual", since, as mentioned before, it consists simply in the lack of p implant layer near the edge of $p+$ layer. Additional p dopants in $p+$ layer assure higher electric field in the center than in the edge region [16]. These thick devices feature high breakdown voltage, high detection probability in the visible and even in InfraRed light, large active area but poor timing resolution, due to thick junction [4].

Several types of planar SPAD have been developed since the beginning of 1970s. The thin depletion region reduces the detection probability but it improves timing performances, in timing jitter and dead time. Haitz developed one of the first planar SPAD [20]. In these devices $n+$ layer creates a $n+-p$ junction with n-well guard ring in order to overcome the PEB problem. The multiplication layer is under $n+$ layer (Fig. 1.6).

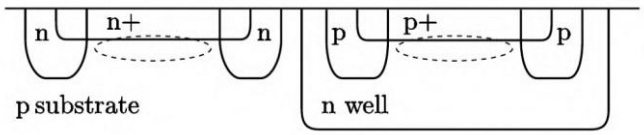


Figure 1-6. Structure of planar SPAD [16]

The proximity of avalanche region to surface makes the devices sensitive to blue and UltraViolet light. This structure has been successfully integrated in Complementary Metal-Oxide-Semiconductor (CMOS) processes. In addition to planar structure with $n+-p$ junction, CMOS SPADs can be developed in different configurations. If CMOS process has a deep n-well, the active region is constituted by $p+$ layer with p-well guard ring. The deep n-well helps to isolate the SPAD from substrate noise, since it adds another junction between n-well and p substrate that prevents free carriers in the substrate. The n-well allows to isolate SPADs from each other and from the rest of circuitry, reducing the crosstalk probability between SPADs. The crosstalk is an unpleasant phenomenon occurring

when SPADs are so close that an avalanche in a SPAD causes the avalanche in neighbouring SPAD (Section 1.7.2). However, n-well isolation causes larger distances between neighbouring SPADs reducing the fill factor of the device.

1.5 CMOS SPAD technology

In the last years Complementary Metal-Oxide-Semiconductor (CMOS) technology has become the most diffused technology in digital integrated circuits for high speed, low power consumption, low fabrication costs and small area occupation. In particular, CMOS technology allows the monolithic integration of additional circuit for quenching processing and data readout and storage in the same substrate of the photodiode [21]. The integration improves the signal temporal response, reduces detector size as well as the fabrication cost. Even if CMOS technology became available in 1980s, the feasibility of CMOS SPAD has been proved only in 2003.
The SPAD integration in CMOS technology requires complex processes to assure high level of performance. The fabrication material and the fabrication process have to guarantee very low level of impurities, since they could constitute energy levels in the silicon bandgap in which carriers can be trapped and after released, or in which carriers annihilate each other. Moreover, the high electric field in the depletion region should be not so high to avoid the transitions of carriers between valence and conduction bands, band-to-band tunnelling effects. The tunnelling becomes significant when electric field goes beyond $10^6\ V/cm$ [11].
However, the most important goal of SPAD in CMOS technology is to reduce the electric field in the peripheral edges to avoid premature edge breakdown (PEB).
At this purpose, guard ring has to be insert in the structure. As introduced above, PEB is due to high doping profile curvature at the edge of junction, resulting in a high electric field. The key to reduce PEB probability is to reduce the electric field

at the edge of junction and to increase the avalanche probability in the center of multiplication region.

The first requirement against PEB consists in adding $n+$ layer in the central part of the junction, between n substrate and p surface, enhancing and confining the electric field in the central part of the junction (Fig. 1.7 a). The second option could be the insertion of low doped p guard ring enclosing the junction, in order to decrease the electric field in peripheral edge (Fig. 1.7 b). Another solution consists in a p diffusion close to the edge p well at sensing area, resulting in low-doped n region between p area. The bias of additional gates placed on low-doped n region causes the depletion of this region (Fig. 1.7 c).

Finally, the development of CMOS process has developed the Shallow Trench Isolation (STI) employment as guard ring. They are trenches of dielectric materials (e.g. silicon dioxide), which stop the electric current leakage in the silicon and confine the electric field (Fig. 1.7 d) [22].

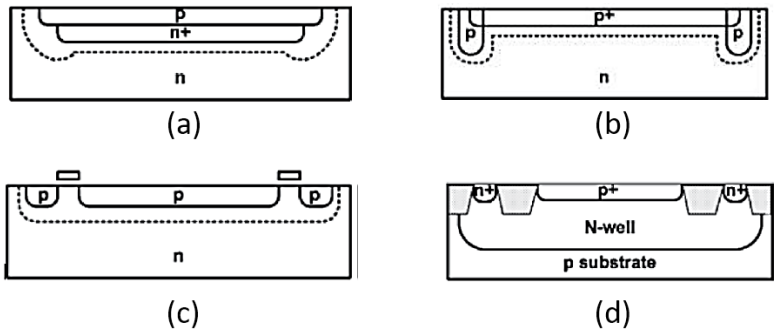


Figure 1-7. a) N+ layer between n substrate and p surface, b) low doped p guard ring enclosing the junction, c) low-doped n region between p area, d) structure with STI guard ring [22]

However, STI can increase the noise level device, since they inject free carriers from STI surface to the depletion region. To reduce this level sources, implant "virtual" guard ring near STI should be designed in the device.

1.6 Silicon Photomultipliers

In each CMOS SPAD all electronic circuits, quenching, reset, control and read-out, are integrated in the same pixel resulting in higher time resolution and lower size and cost. Despite of these advantages, a single SPAD works as photon-trigger switch, ON or OFF state, and the output signal does not give information about the number of photons hitting the device. The signal will be the same if one or more photons simultaneously hit the device. To obtain a signal proportional to the photon flux, CMOS SPAD can be assembled in arrays. Silicon photomultipliers (SiPMs) are arrays of independent SPADs in parallel configuration with quenching resistor. Each SPAD and quenching resistor represents a cell that works independently: if a cell detects a photon triggering the avalanche, other SPADs are ready to detect another photon. This increases the photon detection capability of SPAD.

The sum of SPADs signal results in analog signal output proportional to the incident photon flux, in particular to the triggered cells and then, to the number of photons hitting the cells.

In addition to high photon detection capability, SiPMs benefit from compactness, excellent time resolution, low operative voltage. However, the analog SiPMs are susceptible to electronic noise [23] and the output signal could be altered from parasitic effects due to interconnections between SiPM and read-out electronic circuit. A buffer to isolate SPAD from the external processing electronic circuits can reduce the electronic noise effect.

The signal read-out circuit integrated in CMOS SPADs is typically constituted by a CMOS inverter used as discriminator, even if voltage comparators or source follower circuits can be found in other applications.

In addition to analog ones, SiPMs can be assembled in Digital SiPMs with each cell containing a SPAD and a more complex quenching circuit. Each cell gives an output digital signal that is successively sum up with other cells outputs.

Contrary to analog SiPMs, each SPAD has an own readout circuit. A digital memory is integrated in the electronic circuit to select and enable or disable SPADs in specific row and column of the array. A photon counter is connected to the cell to count the number of detected photons. This processing data configuration is known as photon counting modality.

SPAD arrays are a good solution for low light level detection applications, since it is possible to have a sensitivity down to single photon level, working in photon counting mode.

In order to have information not only about the number of detected photons, but even about the arrival time of photons, a time-to-digital converter (TDC) is co-integrated in the sensor.

In Fig. 1.8 each cell provides a fast asynchronous trigger signal and a slower synchronous data output signal. The trigger signal is connected to a balanced, low skew trigger network connected to on-chip TDC. The trigger network can be set to start the TDC at the detection of the first photon, or at higher photon threshold [23].

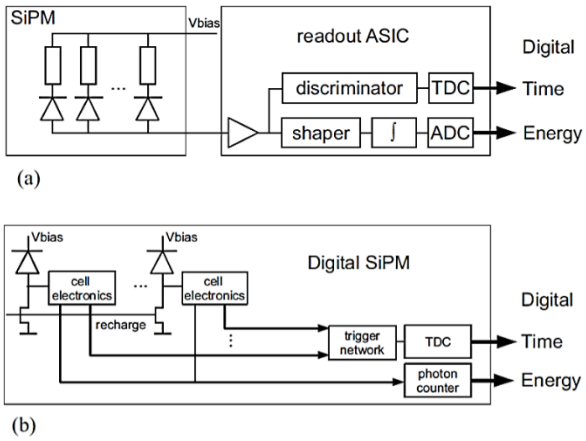


Figure 1-8. Scintillation light detector systems based on the analog (a) and digital (b) silicon photomultiplier [23]

Even if TDC in SPAD arrays exhibits excellent time resolution [9], it reduces the fill factor, as well as the photon detection efficiency, since it covers a large part of

pixel. In order to increase the FF, SPAD layout has to be put very close to read-out electronic circuit with an appropriate implant to be electrically isolated.

1.7 SPAD Noise Performance

SPAD performance is influenced to intrinsic noise sources, such as dark counts and afterpulsing events, and external noise sources due to electrical and optical crosstalk between neighbouring pixels [22].

An avalanche process can be triggered even in dark condition. The Dark Count can be constituted by avalanche pulses due thermal generation, diffusion from neutral regions, band-to-band tunnelling, trap assisted tunneling, etc. The dark counts will be deepened in the Chapter 2, while in the next paragraphs afterpulsing events and crosstalk will be explained.

1.7.1 Afterpulsing events

The impurities and crystal defects due to semiconductor material or due to fabrication process can create new energetic levels inside the bandgap of the semiconductor. These levels become trapping centers, that capture charge carriers during avalanche process. Some charges carriers can be trapped during SPAD discharge. Trapping centers are characterized by finite lifetime, i.e. the emission rate of filled traps [3], that it may vary from short time until hours. Therefore, they can be released in random time interval (Fig. 1.9). If a carrier is released when SPAD bias voltage is over the breakdown value, it can trigger another avalanche and induce a time correlated noise called afterpulse [24].

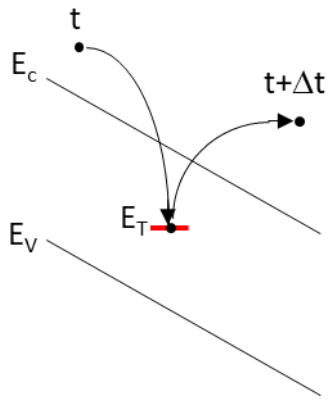


Figure 1-9. Mechanism of trapping and delayed realising of a free carrier by an impurity in the depletion region (afterpulsing event)

The afterpulsing probability at a time t after the first avalanche is:

$$P_{ap}(t) = N_c \cdot P_t \cdot \frac{e^{-t/\tau}}{\tau} \cdot P_{BD} \tag{1.9}$$

with N_c the carriers numbers coming from the first avalanche, P_t the probability that carriers remain trapped, τ the time constant of capture depending on the position of trap level inside the bandgap, P_{BD} the probability that a free carrier generates an avalanche process. The Dark Count Rate (DCR) due to afterpulse can be evaluated as

$$DCR = \frac{DCR_0}{1 - \langle P_{ap} \rangle} \tag{1.10}$$

with DCR_0 the dark count rate without afterpulsing events [11].

Afterpulses can introduce a significant noise source (strong DCR increase), especially if afterpulse probability is so large that each pulse generates a new afterpulse. Therefore, it is important to reduce as much as possible the afterpulsing probability, P_{ap}. Firstly, P_{ap} minimization can be reached by operating in design and manufacturing process. In design process, small depletion area reduces the parasitic SPAD capacitance (C_{SPAD}), resulting in decrease of charge flowing in an avalanche:

$$Q = C_{SPAD} \cdot (V_{bias} - V_{bd}) \quad (1.11)$$

manufacturing process should be performed assuring high cleanness level to decrease the number of traps. Successively, during SPAD operation, it is possible to act on operating parameters, such bias voltage and temperature, to decrease afterpulse probability. If SPAD works at low bias voltage, a small number of carriers generates an avalanche. Moreover, at low voltage, the avalanche trigger probability P_{BD} will be also reduced, decreasing the probability P_{ap}.

If SPAD works at low temperature, the lifetimes of traps will increase and the random release of trapped carriers will become slower, increasing the afterpulsing events at long time from the first avalanche. Working at higher temperature, SPAD afterpulse probability will decrease.

As explained in the Section 1.3.2, a circuit with large quenching resistor can be designed to introduce a dead time after photon detection in order to allow the release of all carriers. During dead time, the voltage is decrease below the breakdown value and all charges are released without any afterpulse event. Increasing the dead time, the afterpulse probability will be lower, but as well as the photon detection, since, during the dead time, the system is not able to detect photon (Fig. 1.10). By replacing a quenching transistor to a quenching resistor, the dead time can be changed modulating gate voltage in the transistor [3, 11].

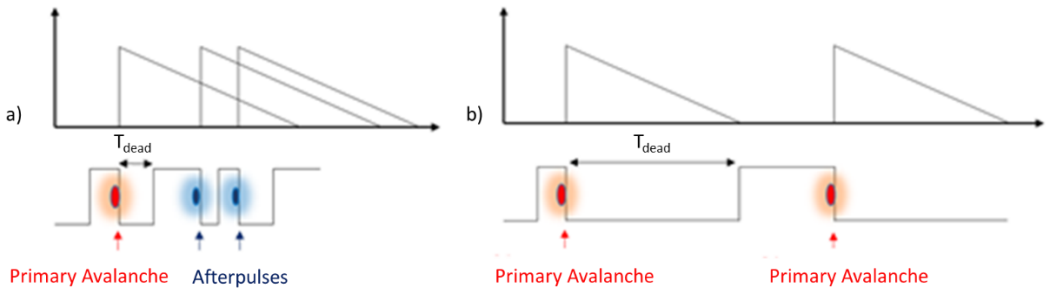


Figure 1-10. Afterpulsing events introducing a short a) or long b) dead time after first carriers avalanche

1.7.2 Crosstalk

In addition to afterpulsing, representing a time-correlated noise source, there is a spatial correlated noise, called crosstalk, optical or electrical, between neighbouring pixels.

The optical crosstalk is triggered by emission of secondary photons from carrier avalanche (Fig. 1.11). If the photons have greater energy than the silicon bandgap, they can travel in the silicon bulk and hit directly or indirectly (optical reflection on substrate) neighbouring SPADs, triggering correlated avalanches. The crosstalk influences strongly the photon counting. SPAD output will be an incorrect evaluation of the optical signal detected by each pixel.

Crosstalk research indicated that photons triggering avalanche in adjacent pixels can be generated even by Bremsstrahlung with charged impurity centers or recombination of free charges in avalanche region [11].

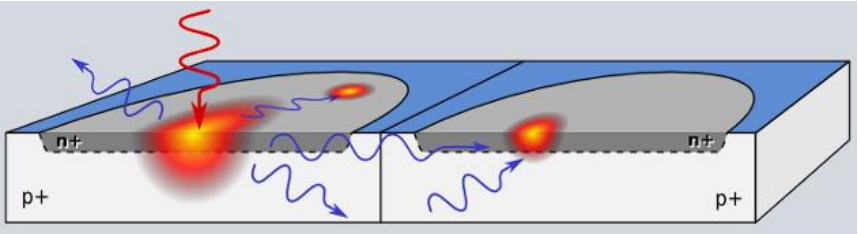


Figure 1-11. Optical Crosstalk between neighbouring pixels [13]

The crosstalk probability increases with long wavelength photons, since they can cross the silicon device without being absorbed, and with SPAD density [11, 24]. Therefore, a solution to decrease the crosstalk in SiPM applications results in increasing the distance between adjacent pixels. However, this configuration would decrease the fill factor and detection efficiency. For this reason, several strategies have been employed in order to reduce crosstalk probability. Barriers with optical absorbing material between adjacent pixels can reduce the optical crosstalk, but not completely prevent it: photons can be reflected at the bottom of device bypassing

the barrier (Fig. 1.12). As an alternative, thick and highly doped substrates increase the absorption of secondary photons generated from carrier avalanche [25].

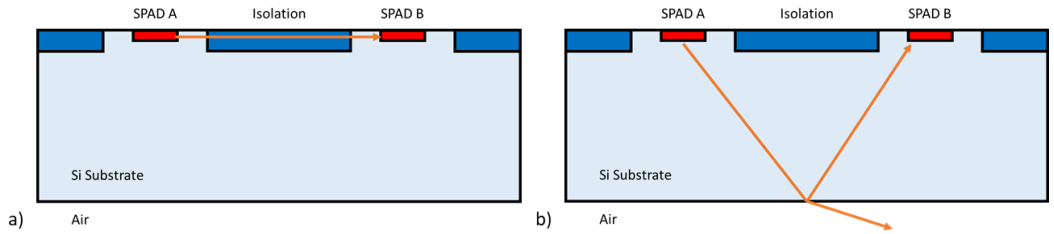


Figure 1-12. Direct a) and reflected b) optical path at bottom of substrate

The electrical crosstalk is due to lateral diffusion and drift of photo-generated carriers in neighbouring pixels. When multiple p-n junctions are located in the same substrate, the charge carriers can exit from depletion region and be injected in depletion region of another SPAD.

The electrical crosstalk is not influenced by temperature as afterpulse event, but it is strongly dependent on overvoltage. The charge flow in the high field region and the avalanche triggering probability are proportional to overvoltage. Working with low voltage can reduce the crosstalk probability, but even the photon detection efficiency. Another solution to decrease electrical crosstalk, as well as the optical one, consists in the isolation of pixel by STI. Exploiting dielectric material assures the electrical isolation of pixel, but influences negatively the fill factor and the photon detection efficiency. Moreover, STI can introduce defects at interface Si/SiO_2 resulting in the increase of dark count rate and in DCR switching, known as Random Telegraph Signal, as it will explain in the Chapter 2.

2.Noise Sources

Introduction

The optical devices performance can be seriously compromise by level of noise, a limiting factor which impacts on the photon counting performance and detection dynamic range. The noise can be external or internal, if it is caused respectively by external factors or if it depends by internal factors.
Some noise contributions are due to:

- Photon shot noise. It is due to fluctuations in the photon arrival time. The photons arrive at random intervals and the number of charges producing photocurrent is random. The fluctuations probability is governed by Poisson statistics. It is called even "white noise" because its power spectral density is constant with frequency.
- Johnson or thermal noise. It is generated by thermal fluctuations in conducting materials. The electrons move in a semiconductor and they collide each other and with atoms of materials creating a current. To reduce the thermal noise, the system should be cool. Thermal noise is independent by the frequency, so it could be also considered "white noise".
- $1/f$ noise or Flicker Noise. This type of noise is present when the frequency f is low. The mechanism that causes Flicker Noise is not clear yet. To reduce $1/f$ noise, the detector should operate at higher frequency [1].

In addition to these signal fluctuations, dark counts in SPAD represent the main intrinsic noise source contribution. Dark counts are spurious signal pulses recorded without incident light. The noise can be uncorrelated or correlated to signal photons. The correlated noise is due to crosstalk and afterpulsing events described in the first chapter. The uncorrelated contribution can come firstly from diffusion of thermally generated minority carriers from neutral region to depletion region, or from

generated electron-hole pairs in depletion region due to band-to-band transition or trap-assisted transition [26, 27].

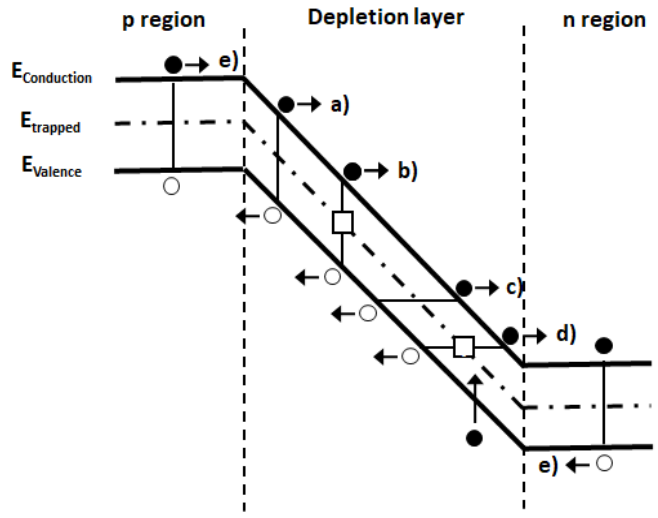


Figure 2-1. Source of noise in SPADs: a) thermal generation, b) trap-assisted thermal generation, c) band-to-band tunneling, d) trap-assisted tunneling, e) direct thermal generation and diffusion

In semiconductor material the thermal generation of carriers depends strongly on the density of local defects located in the bandgap and it increases with the temperature. These local defects depend on intrinsic material impurities or to the technological processes used in device fabrication [25]. As example, in CMOS technology STI or high doping profile can introduce a large number of defects resulting in increase of DCR. In the applications where the time of arrival of photons is unknown, the dark counts constitute an important physical background not distinguishable from the real signal.

In addition to thermal generation, the uncorrelated noise can come from trap-assisted tunnelling (TAT) or band-to-band tunnelling (BTBT) at high electric field (Fig. 2.1) [26]. SPAD bias voltage can contribute to DCR increase by means of different carriers generation mechanisms, such as Poole-Frenkel effects [28, 29] and TAT, occurring at high electric fields ($> 10^5\, V/cm$). These mechanisms can strongly enhance the emission rate of deep energy levels (field-enhanced

generation). At higher electric field ($> 7 \cdot 10^5\, V/cm$) direct band-to-band tunnelling (BTBT) can occur, resulting in a strong generation of free carriers in SPAD junction without the transition in deep bandgap energy levels. If the thermal carrier generation depends on temperature profile, the tunneling generation depends on electric field profile in SPAD junction. Therefore, cooling the detector can contribute to decrease thermal generation rate, but in addition an appropriate electric field profile should be designed to avoid band-to-band tunnelling and field-enhanced generation of carriers.

In addition to defects introduced during technological process, the radiation environment can introduce radiation-induced defects in silicon structure. An impinging particle can interact with silicon structure, dislodging the atom from the normal lattice site. This results in new energy levels in semiconductor bandgap, that can facilitate the transition of electrons and holes between valence band and conduction band, or that can act as trapping centres, catching carriers for a short time and releasing them later [30].

Single defects or cluster of defects may cause the switching in device current resulting in the Random Telegraph Signal (RTS) effect. In the last years different theories have been developed in order to explain the RTS. However, further investigations are necessary to clarify this phenomenon.

This chapter is focused on the main mechanisms that contribute to DCR increase and to RTS effect. RTS is deeply described in the main characteristics and in the causes that could induce it. If the dark current fluctuations between two dark discrete levels (bi-level RTS) can be easily analysed by evaluating the RTS characteristics, the analysis becomes more complicated if the fluctuations are more complex (multi-level RTS). Anyhow RTS analysis can provide tools to recognize the defect responsible for RTS, as explained in this chapter. In addition, annealing process can help in the investigation of RTS defects, since each defect anneals at specific temperature.

2.1 Shockley-Read-Hall thermal processes

When a thermally excited electron moves from the valence band to the conduction band leaves a hole in the valence band. This mechanism generates a charge current. Both electrons and holes contribute to charge current, so the process is known as electron-hole pair generation. The inverse mechanism is known as electron-hole pair recombination.

In silicon devices, due to large and indirect bandgap of silicon, such transitions are rare at working temperature, without extra energy [19]. However, the trap levels introduced in the bandgap by material impurities or defects can assist electron transfer and act as intermediate states between valence and conduction band. This results in a significant increase of rate of free carrier generation in darkness in semiconductor devices. This trap-assisted thermal generation is known as Shockley-Read-Hall (SRH) process [11]. The mechanisms involved (Fig. 2.2) in SRH process are:

a) electron capture: an electron transfers from conduction band to free trapped level;
b) electron emission: an electron moves from trapped level into the conduction band;
c) hole capture: an electron transfers from trapped level to a valence band, annihilating the hole;
d) hole emission: an electron moves from valence band to trapped level.

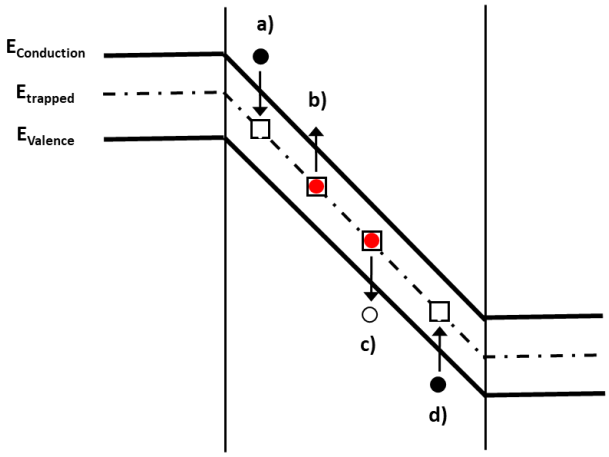


Figure 2-2. Processes involved in the Shockley Read Hall model: a) electron capture, b) electron emission, c) hole capture, d) hole emission

The SRH generation/recombination rate due to trapped levels in forbidden band is

$$G_{SRH} = \frac{n_i^2 - pn}{\tau_{e0}\left(p + n_i e^{\frac{-(E_t - E_0)}{k_B T}}\right) + \tau_{h0}\left(n + n_i e^{\frac{(E_t - E_0)}{k_B T}}\right)} \qquad (2.1)$$

in which G indicates the net generation (if negative the recombination rate is higher than the generation rate), n_i is the intrinsic carrier concentration, n and p are non-equilibrium electron and hole concentrations, E_t the trap level energy, E_0 the Fermi level, k_B the Boltzmann's constant, T the absolute temperature, τ_{e0} and τ_{h0} the lifetimes respectively of electrons and holes

$$\tau_{e0} = \frac{1}{v_{th}\sigma_n N_t} \qquad (2.2) \qquad\qquad \tau_{h0} = \frac{1}{v_{th}\sigma_p N_t} \qquad (2.3)$$

with σ_n e σ_p are the electron and hole capture cross section, N_t is the density of generation centres, v_{th} is the thermal velocity of electron and hole given by

$$v_{th} = \sqrt{\frac{3k_B T}{m^*}} \qquad (2.4)$$

with m^* the electron or hole effective mass.

The SRH generation/recombination rate can be rewritten [3, 31]:

$$G_{SRH} = \frac{v_{th}\sigma_n\sigma_p N_t(n_i^2 - pn)}{\left[\sigma_p\left(p + n_i e^{\frac{-(E_t-E_0)}{k_B T}}\right) + \sigma_n\left(n + n_i e^{\frac{(E_t-E_0)}{k_B T}}\right)\right]} \tag{2.5}$$

If $E_t = E_0$, so taking into account only those traps with energy level in the mid-gap as generation/recombination (GR) centres, G is maximized and it results:

$$G_{SRH} = \frac{v_{th}\sigma_n\sigma_p N_t(n_i^2 - pn)}{\left[\sigma_p(p + n_i) + \sigma_n(n + n_i)\right]} \tag{2.6}$$

Since in the reverse-biased junction the minority carrier concentration in depletion region is lower than the equilibrium concentration ($pn \ll n_i^2$), the generation process is dominant with respect to the recombination process in order to reach the equilibrium. If $p \ll n_i$ e $n \ll n_i$, the generation rate results:

$$G_{SRH} = \frac{v_{th}\sigma_n\sigma_p N_t n_i}{\left[\sigma_p + \sigma_n\right]} = \frac{n_i}{\tau_g} \tag{2.7}$$

where $\tau_g = v_{th}\sigma_n\sigma_p N_t / \left[\sigma_p + \sigma_n\right]$ is called the generation lifetime and it describes the rate at which electron-hole pairs are generated in a depletion layer [3].

The SPAD dark count rate due to SRH generation is obtained integrating on depletion region (width W_D) the product of generation/recombination rate G times the probability for an electron-hole pair to trigger an avalanche P_{BD}:

$$DCR_{SRH} = S \int_0^{W_D} G_{SRH} \cdot P_{BD}(z)\, dz \tag{2.8}$$

with S the surface of photodiode.

DCR due to thermal generation in depletion region depends on crystal defects and impurities due to fabrication process. Low DCR means a good CMOS process with

low defect density, while high DCR indicates high concentration of defects acting as GR centers according to SRH model.

In order to reduce DCR, it is necessary to employ devices with low impurities and, as shown Eq. 2.8, to act on design parameters such as photodiode surface (S): the decreasing of size pixels reduces trap centers for trap-assisted thermal generation. Moreover, DCR caused by thermal generation depends even on working parameters such as bias voltage and temperature. Indeed, DCR increases with bias voltage since the probability to trigger an avalanche increases and the depletion region becomes larger. In addition to bias voltage, the dark count generation rate is also dependent from intrinsic concentration n_i of material, depending on temperature and bandgap energy E_g [14]:

$$n_i \propto T^{\frac{3}{2}} \cdot e^{-\frac{E_g}{2k_B T}} \tag{2.9}$$

The bandgap of silicon is obtained by [19]

$$E_g(T) = 1.17 - \frac{4.73 \cdot 10^{-4} \cdot T^2}{(T + 636)} \tag{2.10}$$

Therefore, employing a device with low intrinsic defects and working at low temperature would strongly decrease DCR [11].

2.2 Tunneling process

In order to obtain carriers avalanche, a high electric field exists in SPAD depletion region. At high electric field, the carrier generation and emission rate are increased by tunneling of electron from trap level into conduction band (Trap Assisted Tunneling, TAT) and by tunneling of electron from valence band into conduction band (Band-to-Band Tunneling). The probability of TAT is dependent on process conditions and steps introducing trap levels [19]. When electron tunnels into

conduction band, it leaves a hole in the valence band, therefore the tunneling process generates electron-hole pairs. TAT contribution is taken into consideration by replacing the lifetimes τ_{e0} and τ_{h0} in Eq. 2.1 with respectively $\tau_{e0}/1+\Gamma$ and $\tau_{h0}/1+\Gamma$, where the function Γ is defined as field-effect enhancement factor [31]:

$$G_{SRH,\ TAT} = \frac{(n_i^2 - pn)(1+\Gamma)}{\tau_{e0}\left(p + n_i e^{\frac{-(E_t-E_0)}{k_B T}}\right) + \tau_{h0}\left(n + n_i e^{\frac{(E_t-E_0)}{k_B T}}\right)} \quad (2.11)$$

The function Γ [31] is the field effect function of the TAT model, and it is expressed by

$$\Gamma = 2\sqrt{3\pi}\frac{|E(z)|}{F_\Gamma} e^{\left(\frac{E(z)}{F_\Gamma}\right)^2} \quad (2.12)$$

with $E(z)$ the local electric field intensity and

$$F_\Gamma = \frac{\sqrt{24 m^* (k_B T)^3}}{qh} \quad (2.13)$$

where $m^* = 0.25 m_0$ is the effective mass for tunneling (m_0 is the free electron rest mass), q is the electron charge and h is the reduced Planck's constant. The DCR caused by thermal generation (SRH model) and TAT is given by:

$$DCR_{SRH,\ TAT} = S \int_0^{W_D} G_{SRH,\ TAT} \cdot P_{BD}(z)\, dz \quad (2.14)$$

The probability of tunneling is highly dependent on depletion thickness, electric field intensity and doping concentration [19]. Indeed, at high doping concentrations, the influence of TAT enhances the DCR, due to higher electric field intensity, and the strong bias voltage dependence of DCR. At low doping concentrations, the influence of TAT becomes negligible [3].

If the electric field intensity in avalanche region is very high, electrons are able to penetrate directly from valence band into conduction band through the bandgap (Band to Band Tunneling, BTBT). Contrary to TAT that occurs more frequently, BTBT is expected in extreme conditions (Fig. 2.3) [19]. The width of the bandgap is E_{gap}/qE, therefore increasing electric field intensity, the width of this barrier decreases [3]. BTBT becomes the main noise source if the electric field intensity exceeds $7 \cdot 10^5\ V/cm$ [11, 31].

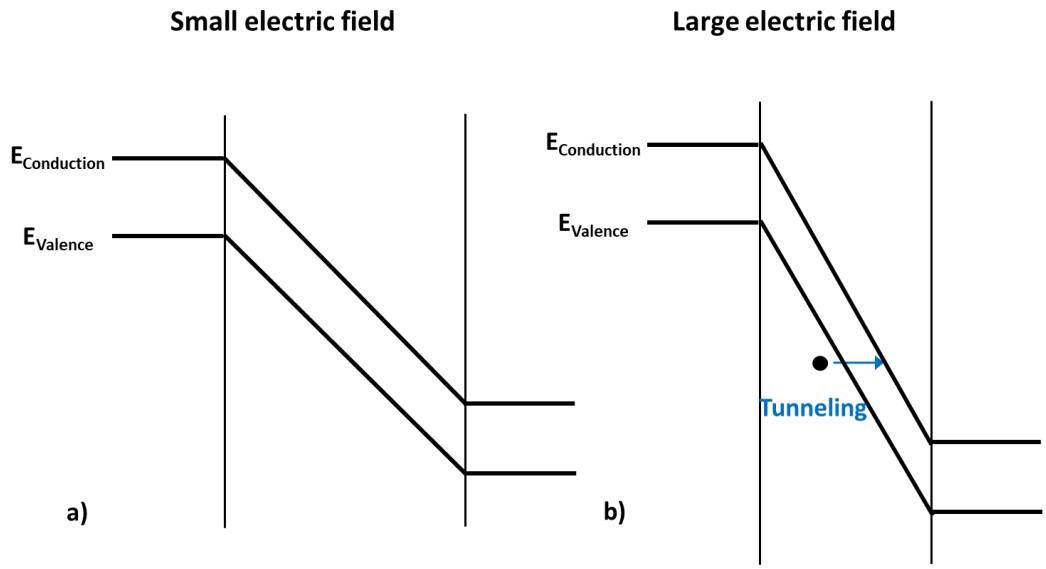


Figure 2-3. Tunneling probability variation in a) small electric field and b) large electric field

The generation rate due to BTBT is given by:

$$G_{BTBT} = B \cdot E(z)^{5/2} \cdot D \cdot e^{-\frac{F_0}{E(z)}} \tag{2.15}$$

where factor B is $4 \cdot 10^{14}\ cm^{-1/2}V^{-5/2}s^{-1}$, $E(z)$ is the electric field intensity, D is 1 in depletion region in which tunneling effect occurs, while it is 0 on the edges of depletion region, F_0 is a constant depending on the form of the potential barrier in the forbidden band. This value is important since it determines the temperature dependence of the tunneling current. In literature it is given by $1.9 \cdot 10^7\ V\ cm^{-1}$

[3]. Moreover, BTBT is strongly dependent on electric field intensity and on doping profile: with high doping profile, the depletion region is thinner and BTBT probability increases.

The dark count rate due to tunneling is

$$DCR_{BTBT} = S \int_0^{W_D} G_{BTBT} \cdot P_{BD}(z)\, dz \tag{2.16}$$

The total DCR is given by all three contributions [31]:

$$DCR_{TOT} = DCR_{SRH} + DCR_{TAT} + DCR_{BTBT} \tag{2.17}$$

2.3 Poole-Frenkel effect

Depending on the electric field, it could be necessary take into account in Dark Count the contribution due to Poole-Frenkel (PF) effect [28, 29]. This effect becomes dominant at moderate electric fields ($10^4\ V/cm$) [32].

The Poole-Frenkel effect is an electric-field-induced lowering of potential barrier for the thermal emission of a carrier from a level in the bandgap (Fig. 2.4) [33].

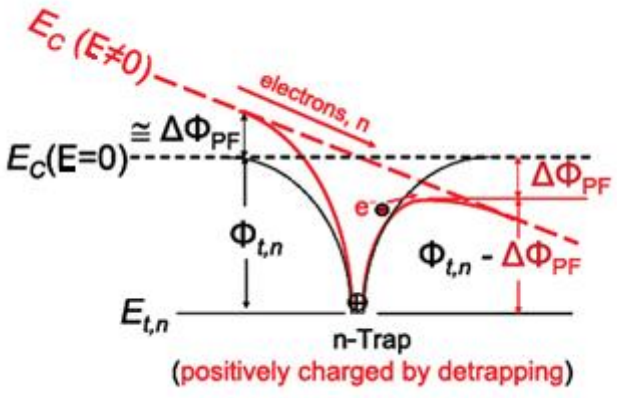


Figure 2-4. Schematic representation of Poole-Frenkel effect [34]

In Poole-Frenkel effect, the barrier for an electron to escape from the trap at energy level E_{tn} into conduction band is

$$e_0\phi_{tn} = |E_c - E_{tn}| \tag{2.18}$$

While the barrier for a hole to escape into the valence band is

$$e_0\phi_{tp} = |E_{tp} - E_V| \tag{2.19}$$

If the electric field $E = 0$, the barriers are equal in both directions. If the electric field with appropriate sign exists, $E \neq 0$, in the direction of drift of the electrons, the barrier is lowered by $\Delta\phi_{PF}$ with respect to the one in field free state. In case of electric field with opposite sign, the barrier enlarges in the same direction by about the same value [34].

The barrier reduction $e_0\Delta\phi_{PF}$, expressed in $[eV]$, is evaluated to be

$$e_0\Delta\phi_{PF} = \left[(e_0^3E)/(\pi\varepsilon_{r,opt}\varepsilon_0)\right]^{1/2} \tag{2.20}$$

where e_0 is the elementary charge, ε_0 the vacuum permittivity and $\varepsilon_{r,opt}$ is the relative optical permittivity (relative optical dielectric constant) of dielectric material. With PF effect, traps escape more often and the density of free electrons and holes in the bands, respectively n_{PF} and p_{PF}, increases with respect the ones without PF effect. This may increase the leakage current due to increased conductivity $\sigma_{PF} = e_0\mu_n n_{PF}$ for electrons with respect to no PF effect ($\sigma_0 = e_0\mu_n n_0$)

$$\sigma_{PF} = e_0\mu_n n_{PF} = e_0\mu_n n_0\, exp\frac{e_0\Delta\phi_{PF}}{k_BT} = e_0\mu_n n_0 exp\left[\frac{e_0}{k_BT}\left(\frac{e_0}{\pi\varepsilon_{r,opt}\varepsilon_0}\right)^{1/2}E^{1/2}\right] \tag{2.21}$$

with μ_n the field independent electron mobility, k_B the Boltzmann constant and T the temperature. This results in the PF current density [34]

$$j_{PF} \propto Eexp\left\{-\frac{e_0}{k_B T}\left[\phi_t - \left(\frac{e_0}{\pi \varepsilon_{r,opt} \varepsilon_0}\right)^{1/2} E^{1/2}\right]\right\} \tag{2.22}$$

2.4 Diffusion from neutral region

In reverse biased SPAD device lower minority carrier density at the edges of depletion region is lower than equilibrium carrier density. Therefore, electrons and holes tend towards the equilibrium carrier state by diffusing respectively from p-type neutral region and from n-type neutral region. The process of diffusion acts against the gradient of carrier concentration in a semiconductor. However, when diffused carriers reach the depletion region in which high electric field exists, they may contribute to the dark count rate.

Taking into account the diffusion and drift processes, the total diode current in p-n junction is obtained by:

$$I = I_0\left(e^{\frac{qV}{k_B T}} - 1\right) \tag{2.23}$$

with q the electron charge, V the bias voltage, k_B the Boltzmann's constant, T the absolute temperature and I_0 the saturation current in reverse biased SPAD.

$$I_0 = I_{0p} + I_{0n} = qn_i^2 \cdot \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) \tag{2.24}$$

Taking into consideration $I = -I_0$ in reverse biased SPAD, DCR due to diffucion process is obtained by:

$$DCR_{diff} = S\left(\frac{I_{0e}}{q} P_{BDe}(0) + \frac{I_{0h}}{q} P_{BDh}(W_D)\right) \tag{2.25}$$

with S the diode surface and W_D the depletion region width.

Taking in consideration the Eq. 2.24, DCR_{diff} is strongly dependent on temperature since

$$\frac{D}{L} \propto T^{\gamma} \qquad (2.26) \qquad\qquad n_i \propto T^{\frac{3}{2}} \cdot e^{-\frac{E_g}{2k_B T}} \qquad (2.27)$$

with γ a constant. Therefore, the thermal dependence is given by:

$$I_{0p} = \frac{D_p}{L_p} \cdot \frac{qn_i^2}{N_D} \propto T^{\gamma} \cdot T^{\frac{3}{2}} e^{-\frac{E_g}{2k_B T}} \qquad (2.28)$$

$$I_{0n} = \frac{D_n}{L_n} \cdot \frac{qn_i^2}{N_A} \propto T^{\gamma} \cdot T^{\frac{3}{2}} e^{-\frac{E_g}{2k_B T}} \qquad (2.29)$$

The stronger DCR_{diff} temperature dependence is clearly due to exponential term $e^{-\frac{E_g}{2k_B T}}$, therefore to n_i dependence [11].

2.5 Radiation effects

The bandgap energy levels, responsible for carrier transitions between the valence band and the conduction band in silicon structure, can be induced not only by CMOS fabrication process, but even by radiation interaction processes.
The radiation induced damage can be separated in two main mechanisms: ionization effects and displacement damage effects.

2.5.1 Total Ionizing effect

When an ionising radiation hits the detector, charge carriers (electron-hole pairs) are created along the particle track. The electron-hole pairs generated in the bulk detector can recombine or move in the oxide electric field: the electrons toward

Si/SiO_2 interface and holes toward the metallic contact. A very short time is available for recombination process, since it is determined by the time required for electrons to swept out of oxide. The mobility of electrons is higher than the one of holes. The fraction of holes and electrons that escape recombination (hole and electron yields) will move respectively toward the gate and toward the Si/SiO_2 interface [35]. The holes that escape initial recombination may be trapped in the oxide by local defects or move through localized states in the oxide toward Si/SiO_2 interface. This results in an increase of oxide positive space charge and in a generation of trapped charges and interface states at Si/SiO_2 (Fig. 2.5). New energy levels are created in the bandgap at Si/SiO_2 interface, which can act as electron-hole generation centers.

The ionising effect is clearly a surface damage, since it causes the build-up of trapped charge in SiO_2 insulator layer that covers the silicon detectors or at interface between the silicon substrate of the device and the oxide [36]. The progressive build-up of defects due to ionising particles is known as Total Ionizing Dose (TID) effect.

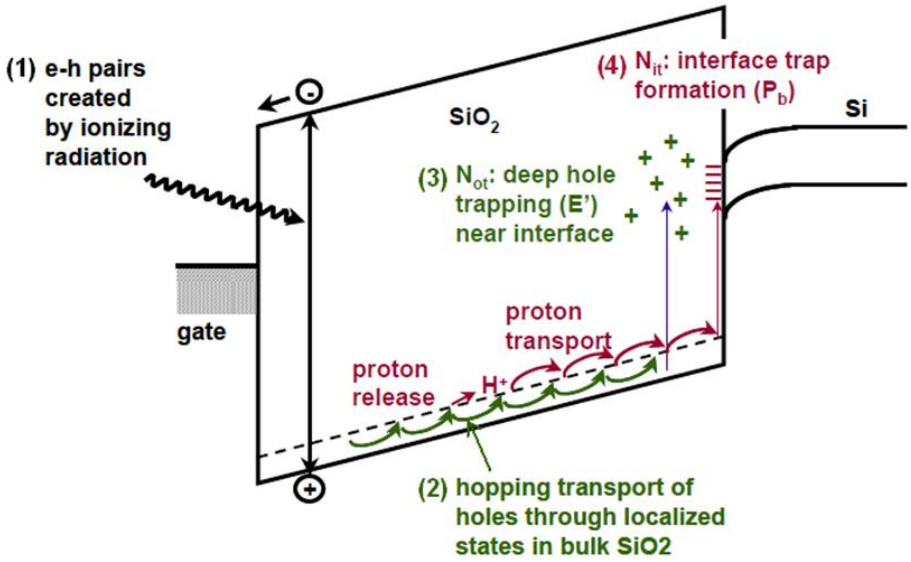


Figure 2-5. Basic radiation-induced processes at Si-SiO_2 [35]

The number of electron-hole pairs generated by ionising radiation is proportional to the energy deposited in the device. The amount of absorbed energy per unit mass of material is defined Total Ionizing Dose (TID) and it is given by:

$$TID = \frac{d\varepsilon_{ION}}{dm} \tag{2.30}$$

The International System Unit for dose is Gray (Gy)

$$Gy = \left[\frac{J}{kg}\right] \tag{2.31}$$

even if the rad (radiation absorbed dose) is the conventional unit used in the radiation effects ($1\ rad = 10^{-2}\ Gy$). The absorbed dose is linked to the particles fluence by means of the ionising stopping power or Linear Energy Transfer (LET). It measures the amount of energy transferred from ionising radiation to a material per unit of length [35]

$$LET = \frac{d\varepsilon_{ION}}{dx} \tag{2.32}$$

Usually LET is expressed in MeV/cm^2g. If a beam of dN/dA particles per area units (A) of energy E hits the device, the particles will deposit in the thickness dx an average energy of $(d\varepsilon_{ION}/dx)dx$. The total TID $[Gy]$ deposited by beam particles per mass units is correlated to LET $[MeV/cm^2g]$ and fluence particles φ $[p/cm^2]$ as follows

$$TID = \frac{d\varepsilon_{ION}}{dm} = \frac{\frac{dN}{dA}dA \cdot \frac{d\varepsilon_{ION}}{dx}dx}{dm} = \frac{1}{\rho} \cdot \frac{d\varepsilon_{ION}}{dx} \cdot \frac{dN}{dA} = k \cdot LET \cdot \varphi \tag{2.33}$$

where $k = 1.6 \cdot 10^{-10}$ is the constant factor from Joule to MeV unit conversion [11].

In photodiode dark current increase due to TID comes mainly from the device perimeter in which STI surrounds the photodiode. Trapped charges and interface states localized in STI are in contact with photodiode active region. This results in Shockley-Read-Hall generation, increasing SPAD dark current [37]. However, many works in literature [38] demonstrated that SPAD devices are quite immune to ionising damage up to Mrad doses. Therefore, radiation damage effects in SPAD are mainly due to displacement damage effect [39].

2.5.2. Displacement Damage effect

If the ionizing energy loss by incident particles results in electron-hole pairs generation in irradiated material, nonionizing energy loss results in phonon production and displacement damage.

The Displacement Damage (DD) mechanism consists in the dislodging of atoms from normal lattice structure due to enough energetic radiation hitting the target material. This results in the degradation of electronic and optical properties of materials due to new energy levels in the semiconductor bandgap introduced by radiation-induced defects. The energy transferred in the interaction results in an energetic primary recoil (Si) atom, known as primary knock-on-atom (PKA), that, if enough energetic, can dislodge other atoms. If PKA has to be displaced, it is necessary that the energy of incoming particle to lattice atom is higher than $25\ eV$, displacement threshold energy for silicon [39]. PKAs create lattice defects such as vacancies and interstitials (Fig. 2.6). A vacancy is constituted by the absence of an atom from its normal lattice position, while the interstitial is the dislodged atom. The combination of a vacancy and adjacent interstitial is called “Frenkel pair” [30]. The interstitials and vacancies are mobile in silicon structure at room temperature; a part of these annihilate with no damages, while the remaining part can migrate in

the silicon lattice and interact each other or with impurity atoms, creating secondary defects [11].

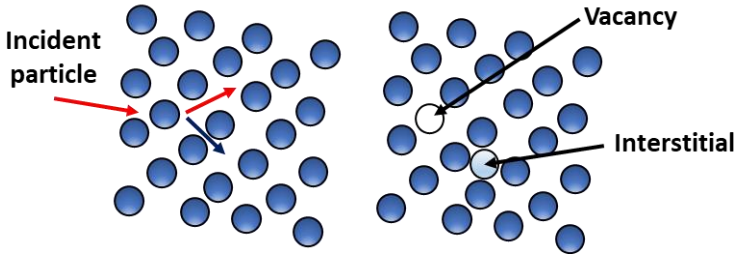


Figure 2-6. Point defect damage in silicon with vacancy and interstitial atoms

This results in the damage of silicon bulk material. Differently to surface ionising damage, DD acts in the bulk material. The main effects of the introduction of defect centers are:

- thermal generation of electron-hole pairs through energy levels near mid bandgap. Only the energy levels near mid bandgap contributes significantly to charge carriers generation, while an exponential decrease in generation rate occurs if levels move from mid bandgap;
- recombination of electron-hole pairs. Recombination is the opposite of generation process, since it removes electron-hole pairs. The mean time that a minority carrier spends in its band before the recombination is defined recombination lifetime. Radiation induced recombination centers decrease the lifetime resulting in the degradation of the gain.
- Compensation of donors or acceptors by radiation-induced centers that reduces carrier concentration. In n-type material radiation-induced acceptors can compensate some of the free electrons in the donor level, reducing the equilibrium in majority-carrier concentration.
- Tunneling of carries through potential barrier by means of defect levels (TAT), that can increase the device current.

- Temporary carrier trapping. A carrier is captured by a defect center and after it is released. This affects the charge collection efficiency in Si particle detectors.
- Decrease of carrier mobility due to radiation-induced centers acting as scattering centers. As well as mobility decreases with increased ionized impurity concentration, the introduction of radiation-induced defects causes the decrease of mobility.
- Type material conversion due to displacement damage-induced carrier removal. The introduction of acceptors can increase the resistivity of n-type material, which may lead to conversion to p-type material.
- Enhancement effectiveness of thermal carrier generation due to high electric field region in which defects are localized. One mechanism responsible of this process can be the reduction of potential barrier for thermal generation (Poole-Frenkel effect) [40].

In order to classify the damage, usually specific parameter, such as minority-carrier lifetime or current gain, is evaluated as a function of particle fluence, to obtain the degradation rate, commonly known in literature as damage factor.

In displacement damage analysis the identification and characterization of defects responsible for mid bandgap level could help to limit the degradation of device properties. However, the identification of defects is not so easy to perform. Indeed, in addition to point defects, the radiation impinging on silicon can also create divacancy, constituted by two adjacent vacancies, or defect-impurity complexes when vacancies or interstitials combine with impurity atoms, such as vacancy-phosphorous pair, P-V complex defect, known as E centers in Si. Therefore, it is clear how the identification process results complex. Moreover, radiation-induced defects may also be created closely together and create defects clusters depending on incident particle type and energy. It is expected that more isolated defects will be created in proton-irradiated Si with respect to neutron-bombarded material, due

to the occurrence of many low-energy Coulombic interactions. The absence of such interactions for neutrons limits the isolated-defect production to low-energy nuclear scattering [30].

2.5.2.1. Niel Scaling

In order to compare the effects of different incident particles in the silicon structure, the radiation damage is scaled with Non-Ionizing Energy Loss (NIEL) or displacement mass-stopping power $1/\rho(dE_{de}/dx)$, evaluated in $[MeVcm^2/g]$ units [36]. NIEL evaluates the energy deposited in the material by non-ionizing radiation interactions (Fig. 2.7).

NIEL takes into account all silicon interactions (ν) with incoming particles and it can be evaluated as follows

$$NIEL\ (E) = \frac{N}{A}\sum_{\nu}\sigma_{\nu}(E_i)\int_{0}^{E_R^{max}} f_{\nu}\ (E_i,\ E_R)P(E_R)dE_R \qquad (2.34)$$

where N_A/A is the number of silicon atoms per gram, E_i is the incident particle energy, E_R is the recoil energy, f_ν is the probability of PKA generation, σ is the cross section for interaction ν and $P(E_R)$ is the Lindhard partition function, that represents the energy available by PKA with recoil energy E_R ($P(E_R) = 0$ under DD threshold) [11].

The comparison of various damage effects in silicon for different particles is shown in Fig. 2.7 [41].

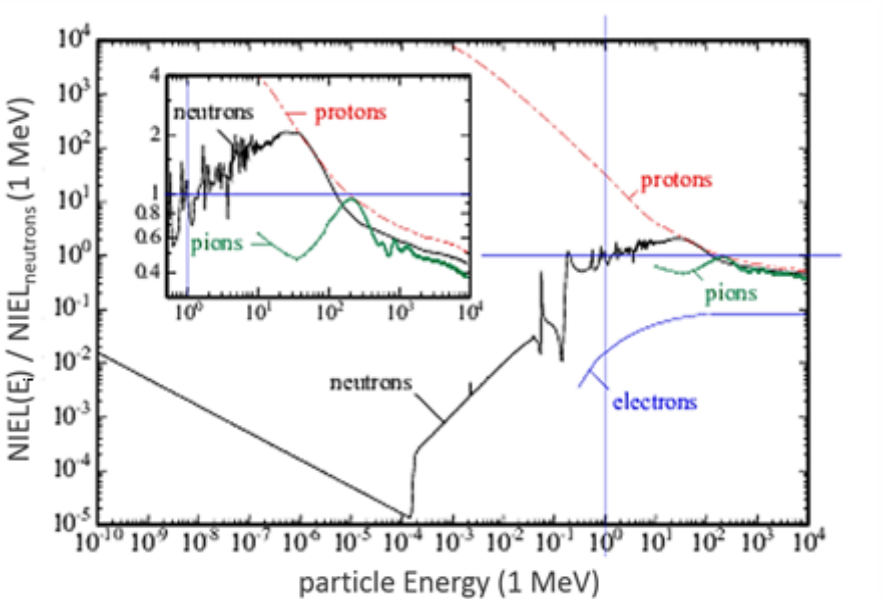


Figure 2-7. NIEL as a function of energy for electrons, pions, neutrons and protons [42]

The displacement damage in Fig. 2.7 is expressed in terms of reference particles. The common reference particles are 1 MeV neutrons. The minimum energy of neutrons to transfer energy by displacement damage is 190 eV. Below this value, damage cross section increases with decreasing energy due to the neutron capture in which gamma ray emitted results in displacement damage. In the region between 100 keV up to 10 MeV, the fluctuations are due to nuclear resonance [11]. For neutrons with energy range in MeV, nuclear reactions increase displacement damage function. At low energies, proton damage function is dominated by Coulombic interactions, and it results higher than neutrons. For high energy (GeV), proton and neutrons show similar damage function. Indeed, in this region the Coulombic interactions becomes negligible and the dominant nuclear are the same for both particles [41].

As in the ionising damage, the radiation displacement damage is proportional to the energy deposited in the lattice structure during the interaction. The displacement damage dose per mass, expressed in $[MeV/g]$ units, for mono-energetic particles beam fluence φ $[cm^{-2}]$ is given by:

$$DDD = \frac{1}{\rho}\frac{dE_{de}}{dx} \cdot \varphi = NIEL \cdot \varphi \tag{2.35}$$

NIEL application allows to take into account the contributions of all particles with different energies in a radiation environment.

Applying the "hardness factor" k, it is possible to correlate the displacement damage of energy integrated flux of all particles source to reference displacement damage of 1 MeV neutron fluence.

$$k = \frac{\int NIEL(E_i) \cdot \varphi(E_i)\, dE_i}{NIEL_{neutrons}\,(1\ MeV) \cdot \int \varphi(E_i)\, dE_i} \tag{2.36}$$

The equivalent fluence of radiation environment is given by:

$$\varphi_{eq} = k\ \varphi_{tot} \tag{2.37}$$

2.6 Random Telegraph Signal

In small area MOS devices, single defects or cluster of defects introduced in the bandgap during CMOS fabrication or irradiation environment, may cause the switching in device current between two or more discrete levels, resulting in well-known mechanism Random Telegraph Signal (RTS). RTS can strongly influence the low-frequency noise in semiconductor devices, therefore understanding the mechanism may supply guidelines in the design process to overcome RTS effects. However, although the first RTS has been observed many years ago, the causes of RTS remain uncertain. In [43] it is supported the theory for which RTS comes from the capture and the emission of charge carriers by means of defect states acting as generation-recombination centers or trapping centers: when an electron results trapped in a defect state, the current switches in the lower state, until the trapped

electron will be released and the current will jump in the upper state. The current will return in the lower state only if another electron will be trapped.
Several theories [44, 45] link the discrete switching of DCR to the Flicker noise, $1/f$ noise, asserting that the origin of $1/f$ noise comes from RTS mechanism. This theory is strongly supported since it has been proved that the superimposition of RTSs creates $1/f$ spectrum noise. Further investigations need to better understand this phenomenon.

2.6.1 Probability distribution of RTS

In order to explain the capture and emission process of charge carriers, standard Shockley-Read-Hall (SRH) theory is applied [46]. Even if the majority of RTSs shows very complex behaviour (more than two levels), possibly due to collective capture in a defect cluster or to physical reconfiguration in a defect cluster after Coulombic interaction [44], mainly two levels RTS will be analysed.
RTS is characterized by following parameters, shown in Fig. 2.8 [46]:

- τ_{up}, the time spent in the high level, corresponding to the time in which the trap is empty;
- τ_{down}, the time spent in the low level, corresponding to the time in which the trap is filled;
- A_{RTS}, the amplitude of RTS switching between the high and low level.

Supposing to define the high level as the state 1 and the low level as the state 0, the probability per unit time of instantaneous transition from state 1 to state 0 results $1/\overline{\tau_1}$ (capture probability), and from 0 to 1 results $1/\overline{\tau_0}$ (emission probability). These assumptions imply that the times in states 0 and 1 are exponentially distributed, being the switching a Poissonian process.

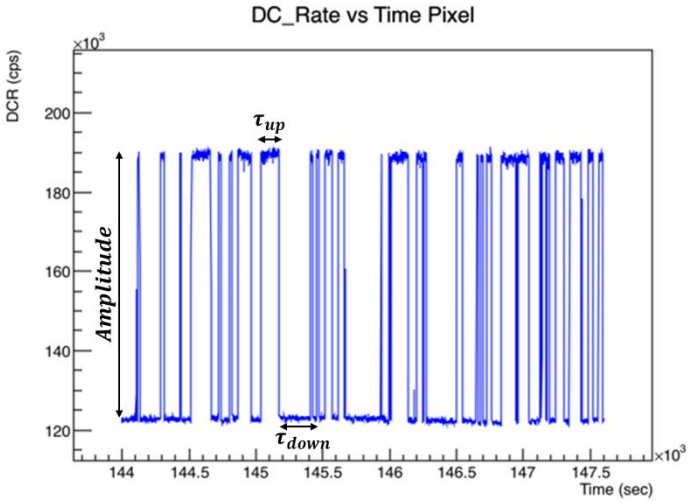


Figure 2-8. RTS behaviour with parameters: $\tau_{up}, \tau_{down}, A_{RTS}$

In order to demonstrate it, let $p_1(t)dt$ be the probability that state 1 will not make a transition for times t, then it will make a transition between the interval t and $t + dt$:

$$p_1(t) = A(t) \cdot \frac{1}{\overline{\tau_1}} \tag{2.38}$$

with $A(t)$ the probability that after time t state 1 will not have transition, and $1/\overline{\tau_1}$ the probability per unit time of making a transition to state 0 at time t [44, 47, 43]. However, the probability of not making transition after time $t + dt$ is given by

$$A(t + dt) = A(t)(1 - \frac{1}{\overline{\tau_1}} dt) \tag{2.39}$$

that is the product of the probability of not making transitions between 0 and t and the probability of not making transitions during t and $t + dt$.

Rearranging Eq. 2.39,

$$\frac{A(t + dt) - A(t)}{dt} = -\frac{A(t)}{\overline{\tau_1}} \tag{2.40}$$

$$\frac{dA(t)}{dt} = -\frac{A(t)}{\overline{\tau_1}} \tag{2.41}$$

and integrating both sides, the probability $A(t)$ becomes

$$A(t) = \mathrm{e}^{-\frac{t}{\overline{\tau_1}}} \tag{2.42}$$

Therefore, the probability $p_1(t)$ becomes

$$p_1(t) = \frac{A(t)}{\overline{\tau_1}} = \frac{1}{\overline{\tau_1}}\mathrm{e}^{-\frac{t}{\overline{\tau_1}}} \tag{2.43}$$

That is correctly normalized since

$$\int_0^\infty p_1(t)dt = 1 \tag{2.44}$$

Similarly, $p_0(t)$ is given by

$$p_0(t) = \frac{A(t)}{\overline{\tau_0}} = \frac{1}{\overline{\tau_0}}\mathrm{e}^{-\frac{t}{\overline{\tau_0}}} \tag{2.45}$$

Therefore, it is possible to conclude that the times in states 1 and 0, respectively τ_{up} and τ_{down}, are exponentially distributed, and the capture and emission process is a Poisson stochastic process, according to the previous assumptions.
The mean time spent in state 1 is then given by

$$\int_0^\infty t p_1(t)dt = \overline{\tau_1} \tag{2.46}$$

while the time spent in state 0 is given by

$$\int_0^\infty t p_0(t)dt = \overline{\tau_0} \tag{2.47}$$

2.6.2 $1/f$ noise

The recent developments in the technological process allowed the fabrication of devices in which the active area is so small to contain only a few number of carriers. Although these devices appear very attractive for speed and compactness, the device scaling imposes a great attention to the low frequency noise (LFN) which becomes an important issue for many circuits [47]. Indeed, the scaling down of device dimensions can change the fluctuations in the time domain, as well as the corresponding power spectral density, resulting in RTS noise contributions [48].

During the last decades, the origin of $1/f$ noise has been deeply investigated. The investigation led to assert that in large devices $1/f$ noise is due to the summation of many RTSs due to defects localized in the device. Therefore, RTS is the result of the decomposition of $1/f$ spectrum into its individual fluctuating components. [44, 47]. The $1/f$ noise is characterized by power spectral density function given by:

$$S_x(\omega) = \frac{C}{\omega} \tag{2.48}$$

where C is a constant and ω is the frequency. The power integrated in the spectrum between ω_1 and ω_2 is given by:

$$P_x(\omega_1, \omega_{2)} = \frac{1}{2\pi}\int_{\omega_2}^{\omega_1} S_x(\omega)d\omega = \frac{C}{2\pi}\ln\frac{\omega_2}{\omega_1} \tag{2.49}$$

As shown the Eq. 2.49, if the frequency ratio ω_2/ω_1 is constant, the integrated noise power is constant [47].

The associated power spectral density $S_I(\omega)$ of two level RTS in Fig. 2.9b, so-called Lorentzian spectral density, is characterized by a constant plateau (P) at low frequency and $1/\omega^2$ roll-off at higher frequencies (Fig. 2.9a) [48].

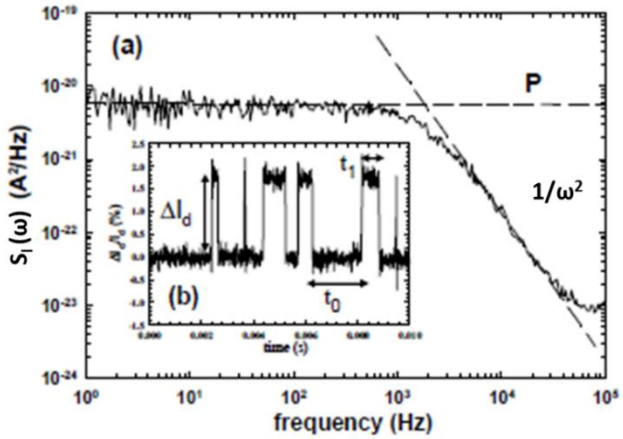


Figure 2-9 a) RTS noise power spectral density (Lorentzian shape) and b) corresponding current fluctuactions [48]

Taking into consideration a noise waveform $z(t)$, that it could due to trapping and de-trapping of carriers in defect trap (RTS), with time constant τ_z, the power spectral density $S_z(\omega)$ has a Lorentzian shape given by [49]:

$$S_z(\omega) = \frac{g(\tau_z)}{1 + \omega^2 \tau_z^2} \tag{2.50}$$

where $g(\tau_z)$ depends on the generation mechanism of random pulse trains [47]. Supposing a distribution of defects traps that contributes to trapping and de-trapping of carriers, the overall noise waveform $x(t)$ is obtained from linear superposition of RTS processes, with time constants distribution between τ_1 and τ_2 and probability density $p(\tau_z)$. The noise spectral density is found by integrating the Lorentzian spectrum characteristic of a single trap:

$$S_x(\omega) = \int_{\tau_1}^{\tau_2} S_z(\omega)\, p(\tau_z) d\tau_z = \int_{\tau_1}^{\tau_2} \frac{p(\tau_z)\, g(\tau_z)}{1 + \omega^2 \tau_z^2} d\tau_z \tag{2.51}$$

If $p(\tau_z)\, g(\tau_z)$ is independent of τ_z and equal to a constant P

$$S_x(\omega) = P\, [\tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_1)]/\omega \tag{2.52}$$

when the conditions $\omega\tau_2 \gg 1$ and $0 \leq \omega\tau_1 \ll 1$ is satisfied, the two terms are respectively $\pi/2$ and 0. Therefore, the superposition of RTS processes can give rise to a spectrum

$$S_x(\omega) = \left(\frac{\pi P}{2}\right)/\omega \tag{2.53}$$

Different models explaining the origin of $1/f$ noise have been developed during the two last decades. Assuming that the fluctuations in the time domain are caused by trapping-detrapping at the interface, the process results limited by the numbers of available traps and the relative noise current spectrum results inversely proportional to the square of carrier concentration. This model explains the origin of $1/f$ spectrum by assuming that is a summation of large number of uncorrelated Lorentzian spectra, each caused by a single trap (Fig. 2.10) [45].

The trap characteristics directly impact the shape of the noise power spectral density of the signal [48]. It is known that RTS is caused by capture and emission of charge carriers in trap levels. Therefore, assuming that traps are isolated and do not interact each other, we can assert that the summation of RTSs with corresponding Lorentzian spectra results in $1/f$ noise in large device [45]. When DCR is due to Flicker noise or to RTS noise, respectively the slope of $1/f$ or $1/f^2$ can be recognized in PSD. Moreover, PSD can also indicate the different configuration of traps or defects showing multi-stable behaviour [19].

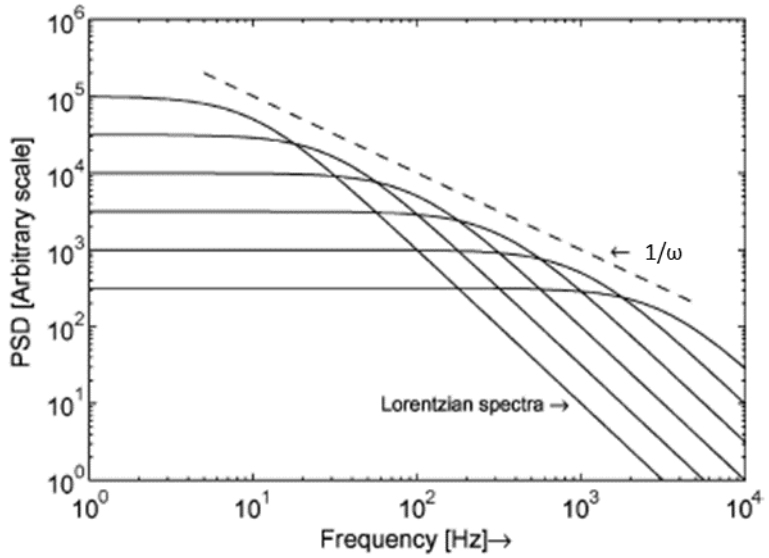


Figure 2-10. The summation of RTS noise results in a 1/f noise spectrum in the frequency domain [45].

2.6.3 Time Lag Plot

The greater part of RTS shows very complex behaviours that make very difficult the analysis. Many DCR levels could be present and some of them could be very close each other making difficult to distinguish them. To overcome this issue, RTS analysis can be performed by means of Time Lag Plot (TLP) by following the current fluctuation (Fig. 2.11) [50]. TLP is obtained by plotting in $x - y$ plane the current at time i versus the current at time $i + 1$ with i and $i + 1$ data point measured at fixed time Δt [51]. As long as the current stays in high or low level in a bi-level RTS, TLP points appear as two clouds of data localized on the diagonal passing from the origin. In the prevalent case of multi-level RTS, a number of clouds equals to number of level will appear in the diagonal, as will be shown in Section 4.3.

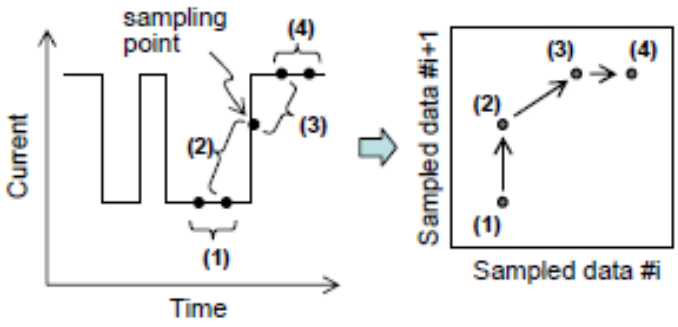


Figure 2-11. Schematic explanation of Time Lag Plot [50]

2.6.4 Surface and bulk damage in semiconductor

Both surface and bulk damage effects can be found in the irradiated devices, according to radiation type and energy spectrum. At $Si - SiO_2$ interface a great number of interface traps exists due to the boundary of two materials. Since the generation rate at $Si - SiO_2$ interface is higher than that in the epitaxial bulk silicon, the interface traps represent the dominant noise source of dark current. The increase of surface dark current is the main effect due to radiation-induced interface defects [52]. Moreover, more impurities are localized at surfaces and interfaces rather than at bulk, since they are strongly exposed during the device fabrication process. For this reason, at surface the density of traps is larger than that in the semiconductor bulk. The traps on the surface of depletion region act as generation-recombination centers [53].

In addition to impurities, radiation-induced bulk defects cause the dark current increase. Irradiation with heavy particles can create large non-uniformities in the dark current spatial distribution resulting in pixels with higher dark current than the average value. They are known as “dark current spike” or “hot pixels” [52]. Random Telegraph Noise could be induced by surface [44] or bulk defects [54, 55]. The capture and emission process in RTS can be explained by Shockley-Read-Hall (SRH) theory. Originally SRH theory has been developed to describe generation-

recombination process through bulk defects. However, it can be applied even to describe the trapping and de-trapping of carriers by interface defects.

The probability that a trap of energy E_t is filled by charge carrier is obtained through the Fermi-Dirac statistics

$$f(E_t) = \frac{1}{1 + \exp\left(\frac{E_t - E_F}{k_B T}\right)} \tag{2.54}$$

with E_F the Fermi-level energy, k_B the Boltzmann's constant and T the absolute temperature. The probability that a trap is empty is given by

$$1 - f(E_t) \tag{2.55}$$

Therefore, the capture rate of an electron is obtained by

$$R_c = v_{th}\sigma_n n[1 - f(E_t)] \tag{2.56}$$

with v_{th} the thermal velocity of the electron, σ_n the electron capture cross section, and n the concentration of electrons, given by

$$n = N_c exp\left[\frac{E_F - E_c}{k_B T}\right] \tag{2.57}$$

with N_c the density of states at energy E_c in the conduction band. Similarly, the emission rate of an electron from trap to conduction band is obtained by

$$R_e = v_{th}\sigma_n n_t f(E_t) \tag{2.58}$$

where n_t is the electron concentration in the conduction band when Fermi level falls at E_t

$$n_t = N_c exp\left[\frac{E_t - E_c}{k_B T}\right] \tag{2.59}$$

From Eq. 2.57 and 2.59,

$$\frac{n}{n_t} = exp\left[\frac{E_F - E_t}{k_B T}\right] \tag{2.60}$$

The mean capture and emission time are obtained by

$$\tau_c = \frac{1}{v_{th}\sigma_n n} \tag{2.61}$$

$$\tau_e = \frac{1}{v_{th}\sigma_e n_t} \tag{2.62}$$

From the previous equations and Eq. 2.60, and by introducing the degeneracy factor g (usually $g = 1$ for electron)

$$\frac{\tau_e}{\tau_c} = \frac{n}{n_t} == \frac{f(E_t)}{1 - f(E_t)} = g\ exp\left[\frac{E_F - E_t}{k_B T}\right] \tag{2.63}$$

If $E_F = E_t$, then $\tau_e = \tau_c$. This means that the mean capture time and mean emission time would be equal if the trap energy (E_t) coincides with Fermi energy level (E_F) [53].

It is difficult to establish that RTS effects are due to radiation-induced defects in the bulk of the silicon rather than at the silicon dioxide interface [54].

It is well known that the trapping by defects in the bulk silicon would have well-defined energy levels and would give rise a distinct Lorentzian on $1/f$ spectrum. However, since in [44] in small-area MOSFETs no evidence of this effect has been found, it would seem that the majority of trapping must take place into oxide defects.

However, [56] demonstrated that in un-irradiated or gamma irradiated CCD devices, no RTS fluctuations have been observed, and that dark current fluctuations, RTS amplitudes and time constants, are not influenced by surface conditions or by small changes in minority carrier density. This indicates that the defects responsible

for RTS are localized in the silicon bulk rather than at Si/SiO_2 interface. Contrary to [44], in [54] the well-defined energy levels, time constants and activation energies indicates that RTS effect is likely due to bulk silicon rather than oxide defects. Moreover, in [54] RTS behaviour changes around 100°C, demonstrating a response to annealing process and confirming that RTS phenomena can be associated with bulk defects.

Another theory that supports RTS effects due to semiconductor bulk defects, comes from RTS correlation with $1/f$ noise. According to [57] , $1/f$ noise is assumed to be originated from semiconductor bulk instead of surface. As explained in Section 2.6.2, in large devices the summation of RTSs effects results in $1/f$ noise, therefore it could be possible that RTS is originated from semiconductor bulk defects [53].

Among proton irradiated SPAD arrays, in [58] the observed RTS seems to be induced by multistable defects located in the silicon bulk. Indeed, it has been found that by increasing the bias voltage, the lower level of RTS is more populated, demonstrating that the defects lie in space charge region. If the defect relies in the diffusion region outside the space charge region, the bias voltage change would not alter the distance between the quasi-Fermi levels and defect voltage and it would not decrease the probability of defects to release electrons. Therefore, the bias dependency proved that the defects are localized inside the space charge region, and not in the oxide or diffusion region [58].

In [59] both DC-RTS due to total ionizing dose (TID) and displacement damage dose (DDD) have been investigated in CMOS image sensors to understand the origin of the phenomenon. The maximum amplitude of DC-RTS transition and the mean time between transition have been investigated. DC-RTS due to DDD showed larger amplitudes than TID induced DC-RTS. Moreover, DDD induced DC-RTS showed that the most of DC-RTS exhibit a short mean inter-transition time, while TID induced DC-RTS exhibit inter-transition time constant distributed uniformly. The amplitude and time distribution represent the first way to distinguish TID or DDD induced DC-RTS [59].

In [38] SPAD devices demonstrated higher sensitivity to bulk displacement damage due to proton irradiation than surface ionizing damage due to gamma rays.
In general, the damage induced by protons is qualitatively different from that induced by gamma rays. Indeed, protons induce a larger numbers of cluster of defects, resulting in larger damage and then, in a higher dark count increase. Moreover, if the clusters of defects are formed in the region where the electric field is high, SPAD dark counts increase, otherwise the damage is similar to that produced by gamma rays, which is not affected by cluster formation. Gamma rays cause mainly the increase of SPAD leakage current due to total ionizing dose, but it does not alter the SPAD operations [60].

2.6.5 Hypotheses for RTS origin

Despite of the relevance of RTS mechanism, its origin is still not well-explained. Several hypotheses in literature have been formulated in order to recognize the defects responsible for RTS behaviour and to understand how they are formed, they evolve over time and change with temperature [61]. This investigation would provide new insights and could help to limit the RTS effects on semiconductor devices.
One of the first RTS explanation lies in a model involving multi-stable defect with two or more stable states. Each defect state has a stable configuration depending on a particular charge state of defect [56, 61, 62].
Fig. 2.12 shows the energy as a function of a lattice configuration coordinate (assuming, as it is common, that defect interacts with only a coordinate). State A is stable for a particular charge state (thick line), and it is separated by an energy barrier from state B, stable for another charge state. The energy level of each state A and B will correspond to different thermal generated electrons in conduction band and, therefore, to the different dark count rate level. The configuration can change from state A (lower energy) to state B if thermal fluctuations are able to overcome

the energy barrier. Once in state B, the process can be accompanied by lattice relaxation via phonon emission to dissipate the excess energy [63], and state B (lower energy) will become the stable state (thin line). In this model the charge associated with switching defect is a consequence of the change in defect configuration [56]. This model can explain the RTS discrete transitions between two stable states by temperature changes. The energy levels of two stable states will determine the dark current generation.

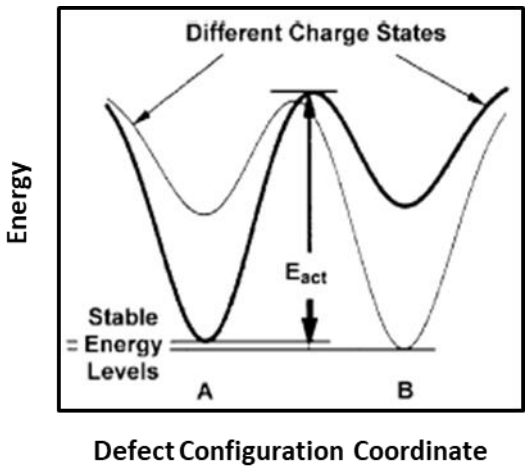


Figure 2-12. Energy versus defect configuration for a defect with two stable states A and B. In one charged state (thick line) state A has the lower energy. In the other (thin line), B is the more stable [56]

According to the position of energy state in the bandgap, the thermal generation of electrons in the conduction band may change and dark current may fluctuate. The step which determines the RTS time constants for two stable states is the crossing of the energy barrier, and it is strongly dependent on the temperature. The detailed description of the configuration coordinate diagram and the knowledge of the energy levels involved allow the identification of the defects responsible for RTS [56].

Although it is possible that RTS effects are due to switching of bulk metastable defects between two configurations, another RTS explanation involves the possibility that dark current generation occurs via a defect with a dipole moment

[61]. In [64], it is shown that the dipole moment of the defect has to be oriented at a particular angle with respect to the field to obtain the maximum field enhancement.

Vacancies and interstitials, formed in displacement damage, diffusing through the crystal can react with other defects or impurity atoms in silicon crystal (O, C, P, etc.) to form stable complexes [65]. Some of these stable complexes and corresponding energy levels are reported in Table 2.1 and in Table 2.2.

Among these complexes, the reorientation of phosphorus-vacancy (P-V) center, known as E-center, is considered one of defects responsible for RTS effects [54]. As reported in Watkins and Corbett [66], the P-V center in neutral charge state has a dipole moment, due to an extra positive charge on P atom, compensated by an extra electron in the orbitals around the vacancy [54, 61]. As introduced before, the field-enhancement factor depends on the orientation of electric field with respect to dipole moment of the defect.

$\boldsymbol{I}$ reactions	$\boldsymbol{V}$ reactions	$\boldsymbol{C_i}$ reactions
$\boldsymbol{I + C_s \rightarrow C_i}$	$V + V \rightarrow V_2$	$C_i + C_s \rightarrow CC$
$\boldsymbol{I + CC \rightarrow CCI}$	$V + V_2 \rightarrow V_3$	$C_i + O \rightarrow CO$
$\boldsymbol{I + CCI \rightarrow CCII}$	$V + O \rightarrow VO$	
$\boldsymbol{I + CO \rightarrow COI}$	$V + VO \rightarrow V_2O$	
$\boldsymbol{I + COI \rightarrow COII}$	$V + P \rightarrow VP$	
$\boldsymbol{I + VO \rightarrow O}$		
$\boldsymbol{I + CV_2 \rightarrow V}$		
$\boldsymbol{I + VP \rightarrow P}$		

Table 2-1. Some defect reactions in silicon. The *i* subscript stands for interstitials, *s* for substitutional, *I* for Si interstitials, *V* for vacancy, *C* for carbon, *O* for oxygen and *P* for phosphorus [65]

Defect	Energy level	Defect type
$\boldsymbol{VO}$	$E_C - 0.17$	acceptor
$\boldsymbol{V_2O}$	$E_C - 0.50$	acceptor
$\boldsymbol{V_2}$	$E_C - 0.23$	acceptor
	$E_C - 0.42$	acceptor
	$E_V + 0.25$	donor
$\boldsymbol{VP}$	$E_C - 0.45$	acceptor
$\boldsymbol{CC}$	$E_C - 0.17$	acceptor
$\boldsymbol{CO}$	$E_V + 0.36$	donor

Table 2-2. Energy levels in eV of some defect states. The subscript *c* stands for conduction and *v* for valence [65]

As shown in Fig. 2.13, the P-V center can reorient its axis: the vacancy taking place of any one of four silicon atoms closest to P atom (position 1), can move through the lattice, overcoming thermally potential barriers, and approach again to P atom (new position 1) from a different direction. This determines the reorientation of P-V vector with respect to the electric field vector [54].

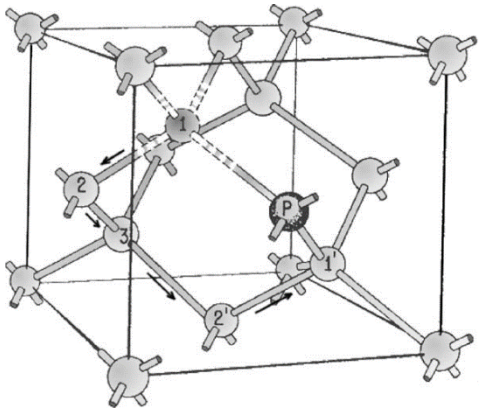


Figure 2-13. The silicon lattice containing the E-center defect [67, 68]

If this mechanism is responsible for RTSs, the time constants between high and low level should depend on the kinetics of reorientation of the P-V center, calculated by Watkins and Corbett as

$$\tau^{-1} = 1.6 \cdot 10^{13} exp\left(-\frac{E_{act}}{k_B T}\right) \tag{2.64}$$

where

$$E_{act} = 0.93 \pm 0.05\ eV \tag{2.65}$$

The RTS time constants measured with a CCD device in [54]

$$\tau_{up}^{-1} = 2.4 \cdot 10^{13} exp\left(-\frac{0.95}{k_B T}\right) \tag{2.66}$$

$$\tau_{down}^{-1} = 5.9 \cdot 10^{13} exp\left(-\frac{0.94}{k_B T}\right) \tag{2.67}$$

confirm that the reorientation of P-V center, common bulk defect in proton irradiated devices, could be responsible for RTS [54, 67].

The level of dark current generation is dependent on the orientation of the defect in the applied electric field. The movement of the vacancy from a small or large angle relative to the electric field vector results respectively in a not significant difference (small RTS amplitude) or in a large difference in dark current generation (large RTS amplitude) [54, 67].

This model assumes that the RTS amplitude is dependent on defect reorientation and not on electric field intensity. However, in this model the electric field seems to influence the reorientation kinetics of defects, producing a possible variation in time constants [54].

The third RTS explanation involves the enhanced generation through intercenter transfer mechanism due to clusters of divacancies [61, 69]. In severe radiation

environment, such as protons in Van Allen belt in space, or neutrons in nuclear reactor, or heavy particles incident on the silicon detectors in high energy nuclear experiments, recoil atoms can produce many displacements, resulting in vacancy aggregations, such as cluster of divacancy V_2, or higher vacancy complexes, V_3, V_4, etc. [70]. The enhanced formation of divacancies is due to high density of close vacancies in the same cluster, rather than in clusters related to different displacement events [65].

As explained in the Section 2.6.4, the emission rates for electron and hole from SRH center is given by

$$\lambda_n = \frac{1}{\tau_{en}} \tag{2.68}$$

$$\lambda_p = \frac{1}{\tau_{ep}} \tag{2.69}$$

The generation rate from a single defect level is given by

$$G = \frac{1}{\tau_e} = \frac{1}{\tau_{en} + \tau_{ep}} = \frac{\lambda_n \lambda_p}{\lambda_n + \lambda_p} = \lambda_n f_T \tag{2.70}$$

with f_T the fractional occupancy of the center equal to

$$f_T = \frac{\lambda_p}{\lambda_n + \lambda_p} = \frac{1}{1 + \frac{\tau_{ep}}{\tau_{en}}} \tag{2.71}$$

As shown in Fig. 2.14, if the defect lies above mid-gap, τ_{ep} is larger than τ_{en}. Supposing a lower state close to the valence band, the holes emission time from his level is short compared to electrons emission time, then the lower state will be almost permanently occupied. In case of an intercenter transfer occurrence, or coupled defect generation reaction, the electron captured by lower state is directly

transferred to higher state in the neighbouring defect without reaching the conduction band [71, 72].

The fractional occupancy of higher state is obtained by

$$f_{T,coupled} = \frac{1}{1 + \frac{\tau_{ep,coupled}}{\tau_{en}}} \tag{2.72}$$

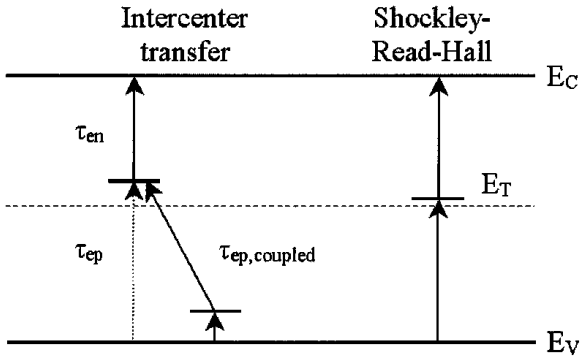


Figure 2-14. Schematic representation of intercenter transfer mechanism with diagram of SRH generation [71]

If the emission of electrons is fastest transition in both cases, the enhancement factor is

$$enhacencement\ factor = \frac{f_{T,coupled}}{f_T} \approx \frac{\tau_{ep}}{\tau_{ep,coupled}} \tag{2.73}$$

Taking into account the exponential dependence of the time constants on energy differences of transitions, the generation through these coupled defects can be considerably enhanced.

The divacancy has three energy levels associated with four charge state $(VV)^+$, $(VV)^0$, $(VV)^-$, $(VV)^{2-}$ depending upon whether there are one, two, three, or four electrons trapped into the well-separated remaining two dangling bonds, with measured level positions indicated in Fig. 2.15 [70].

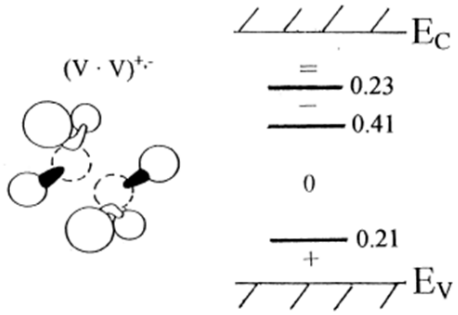


Figure 2-15. Structures of trapped vacancies and their electrical level positions [70]

In reverse bias condition, the neutral state is most probable. If two neutral state divacancies are physically close and an intercenter transfer is present, the leakage current can be strongly enhanced with respect to the isolated defects condition, through the charge exchange reaction (Fig. 2.16).

$$V_2^0 + V_2^0 \rightarrow V_2^+ + V_2^- \tag{2.74}$$

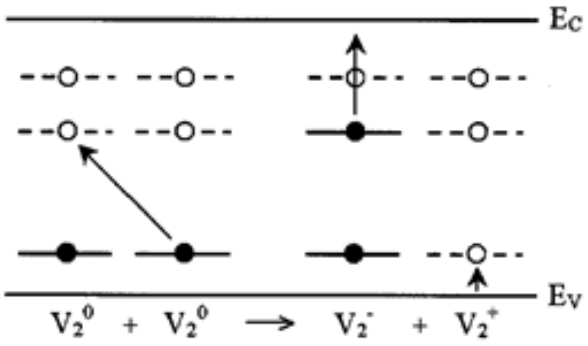


Figure 2-16. Intercenter transfer mechanism in case of two adjacent divacancies. Each energy level in the bandgap corresponds to the energy levels in Fig. 2.15 [71]

The generation process is enhanced since the coupled system reduces the distance between the valence band and defect level through lower level. If the coupling of two adjacent vacancies or vacancy cluster is not stationary, RTS behaviour may occur, since the defects can move in different configurations in which the

intercenter transfer is more or less probable. Therefore, the DCR could be enhanced in a particular position of divacancy that increases the occurrence of intercenter transfer, or come back to its initial value when the divacancy moves in a position in which defects are mutually independent. The time constants in high and low level should depend on kinetics of defects reorientation. The activation energy of these time constants can be associated with potential barrier that a vacancy has to overcome thermally to move from one position to the other [71].

2.6.6 Annealing process

Radiation-induced defects are mobile at room temperature and may recombine. By heating up the irradiated devices, it is possible to reduce the radiation-induced damage by reordering the defects in the crystal. The defect reordering is known as annealing and it is temperature dependent. Each defect type anneals at different temperature, according to its nature. Therefore, it is clear how the investigation of annealing behaviour is important in identifying the defects responsible for RTS and in determining the possibilities for damage reduction.

The investigation of annealing can be performed experimentally through isothermal annealing and isochronal annealing. In the first case, the properties of a device are analysed as a function of time at fixed temperature. In the second case, the properties of a device are monitored after annealing process, performed for a fixed time duration and at increasing temperature steps [40].

Isochronal annealing is usually performed to investigate the annealing of defects [70]. Fig. 2.17 reports the annealing temperature of defects in $\sim 15 - 30$ min isochronal annealing.

As shown in Fig. 2.17 the vacancy disappears in $15\ min$ isochronal annealing at $\sim 70K$ in n-type silicon device, $\sim 150K$ in p-type silicon device and $\sim 200K$ in high-resistivity material. In addition to isolated vacancy, Fig. 2.17 reports also the

annealing temperature of several vacancy-defect. The stability of these pairs reflects the binding energy between the vacancy and each defect [70].

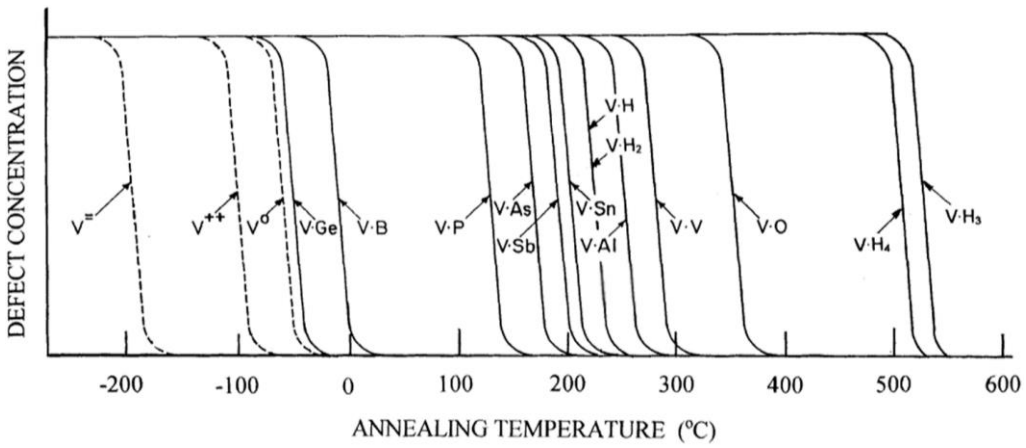


Figure 2-17. Vacancy and vacancy-defect pair annealing stages [70]

The comparison between dark current annealing with theoretical prediction for defect annealing allows the identification of defect responsible for dark current increase. Initially, studies of displacement damage on silicon detectors asserted that only intrinsic defects composed by vacancies and interstitials are responsible for dark current increase [73]. Recent studies proved that even cluster of defects could induce the dark current increase. Indeed, it has been observed that the dark current decreases slowly with temperature, since first defects located around the cluster are annealed, then the defects in the middle. On the contrary, if point defects were responsible for degradation, a steep dark current decrease is expected [37]. Similarly, to dark current decrease, the annealing process involves the RTS transitions. As the temperature increases, RTS switches more slowly and RTS occurrence decreases due to the annealing of the defects involved in RTS. The defects related to post irradiation RTS and dark current increase could have the same nature.

3.SPAD characterization

Introduction

CMOS SPAD devices investigated in the experimental analysis feature different structures and sizes. The test-chip has been supplied by Fondazione Bruno Kessler (FBK). It contains both arrays and matrices of SPADs with different architectures. In this work the attention has been focused on two main structures, named PN and PWNISO. The first structure is based on P+/Nwell junction enclosed in a low-doped region in order to create a guard-ring to avoid premature edge breakdown. The second one is constituted by Pwell/Niso junction. In this layout no well implantation is implemented at the junction periphery, so the guard ring is obtained. Each pixel is integrated in a front-end circuit able to quench and recharge the device or to reset it. SPAD pixels have been characterized before irradiation test.

The experimental setup has been assembled to perform measurements before and after irradiation. For such measurements, a single SPAD can be enabled by a digital pattern and the digital output signal is sent to a counter. SPAD power supply, digital counter and micro-controller communicate with a computer by means of a LabView software, implemented to gather measurement data.

This chapter describes SPAD design, focusing on different structures implemented in the test-chip, and the experimental setup used to characterize the test-chip. A campaign of measurements has been carried out in order to extract SPAD characteristics before irradiation. The results are presented in this chapter.

3.1 SPAD device under test

Single Photon Avalanche Diodes under investigation have been supplied by Fondazione Bruno Kessler (FBK). SPADs are implemented in $150\ nm$ standard CMOS technology. The test-chip features different architectures of SPAD with

different geometries (circular and square) and different optical window sizes, $5\ \mu m, 10\ \mu m, 15\ \mu m, 20\ \mu m$. The analysis performed in this thesis does not take into consideration $5\ \mu m$ SPADs, due to its limited performances.

Each pixel is developed in three different structures.

The avalanche region of first structure, identified as "PN" structure (Fig. 3.1), is based on P+/Nwell junction, enclosed in a region with low doping concentration in order to create a guard-ring region to prevent early periphery breakdown. The other two structures, "PWNISO1" (Fig. 3.2) and "PWNISO2" (Fig. 3.3), are based on Pwell/Niso junction. In the first structure, no well implantation is implemented at junction periphery, so the guard ring is obtained. Moreover, poly-Si gate prevents P+ implantation in guard ring region and contributes to keep the STI at safe distance from active area. Indeed, it is well known that STI can introduce a large dark current in SPAD, due to high number of defects of oxide-silicon interface. On the contrary, in the second structure P+ implantation extends to the STI region. In all structures a metal layer shields non active area realizing an optical window. Moreover, all structures are designed with a retrograde deep n-well, which results on low-noise SPADs due to the isolation from substrate [74, 75].

Taking into consideration the different junction types, the analysis performed in this thesis, gathered data in two main groups, PN type and PWNISO type pixels.

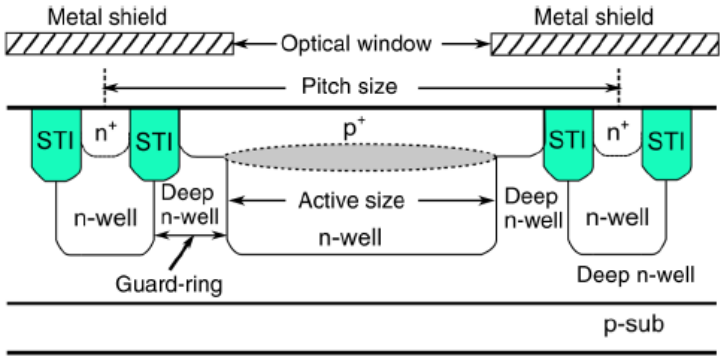


Figure 3-1. Layout of PN layout (P+/Nwell junction) [74]

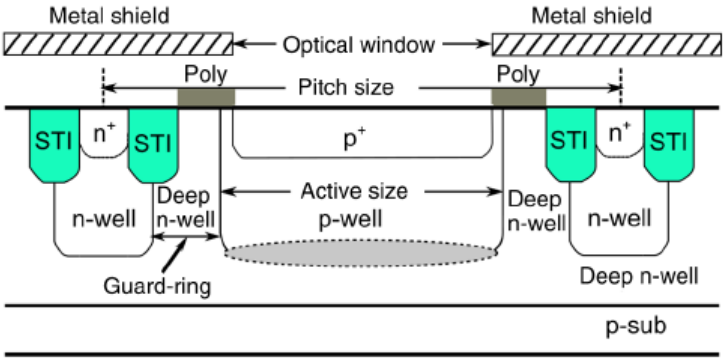


Figure 3-2. Layout of PWNISO1 layout (Pwell/Niso junction) [74]

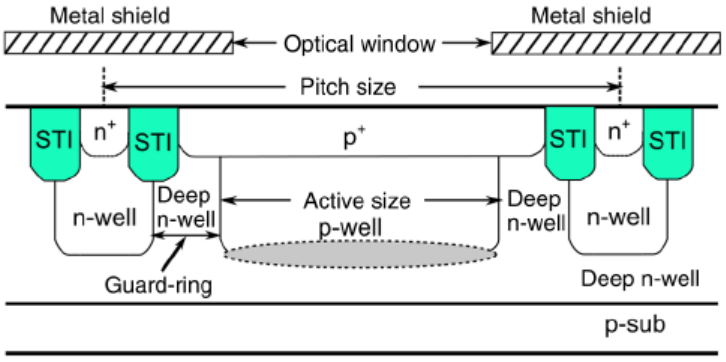


Figure 3-3.Layout of PWNISO2 layout (Pwell/Niso junction) [74]

On the test-chip, SPADs are implemented in a test block of linear arrays and another of matrix [11].

The array block consists of 8 linear arrays, 4 circular and 4 square. Both circular and square arrays have been realized in 4 different sizes each ($5, 10, 15, 20\ \mu m$). For each size 20 pixels are present in the array (Fig. 3.4) [76].

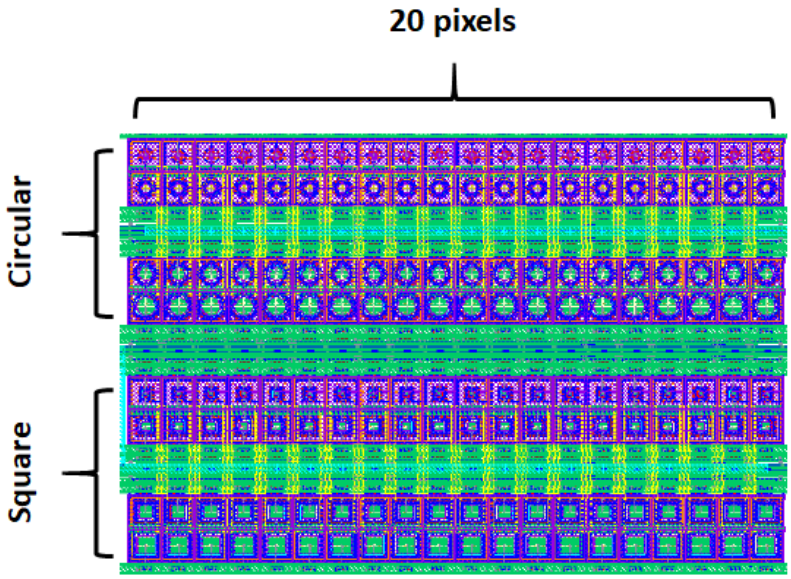


Figure 3-4. Array block with 8 linear arrays [76]

The matrix block consists of $5x5$ matrix, 25 square pixels. The device corners are cut at 45 degrees in order to prevent sharp edges introducing hot spots of high electrical field (Fig. 3.5).

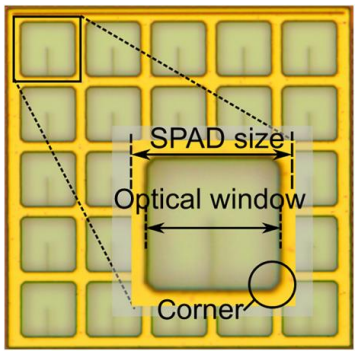


Figure 3-5. Square SPADs matrix with cut corners [74]

The guard ring width has been designed in three different configurations: extreme configuration (ext) $0.6\,\mu m$, moderate configuration (mod) $1.1\,\mu m$, and conservative configurations (con) $1.6\,\mu m$ [74] (Table 3.1). Only the conservative configuration has been analysed in this work. The test chip features two different

SPAD pitches (R_{pitch}), 15.6 μm and 25.6 μm, defined as the distance between cathodes of two adjacent SPADs (Fig. 3.6a, b) [74].

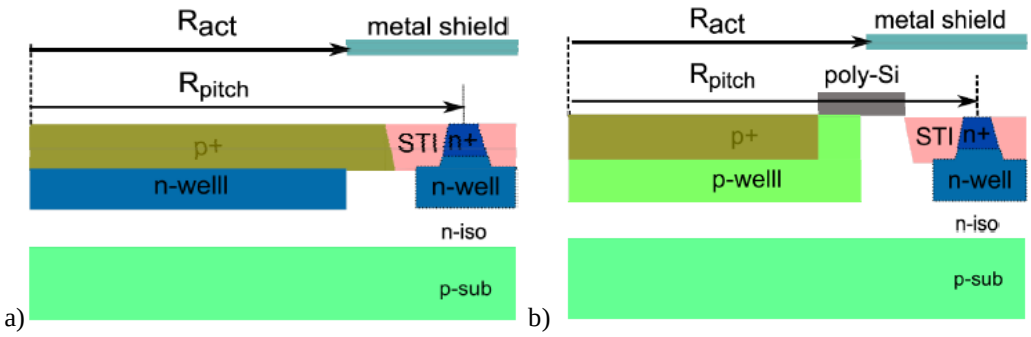


Figure 3-6. a) Cross section of PN layout; b) Cross section of PWNISO layout [76]

Guard ring type	**Conservative** ($\mathbf{1.6\ \mu m}$)		**Moderate** ($\mathbf{1.1\ \mu m}$)		**Extreme** ($\mathbf{0.6\ \mu m}$)	
Optical window (μm)	10	20	11	21	12	22
Pitch size (μm)	15.6	25.6	15.6	25.6	15.6	25.6
Fill factor (%)	39.9	60.6	48.5	66.9	60	73.4

Table 3-1. Geometrical features of SPADs [74]

PN layout features an active junction that is shallower and narrower than in PWNISO layout [74].

The geometrical dimensions of optical window and area in array and in matrix are reported in Table 3.2 and in Table 3.3.

Shape	**Circular**				**Square**			
Optical window ($\boldsymbol{\mu m}$)	5	10	15	20	5	10	15	20
Optical area ($\boldsymbol{\mu m^2}$)	19.63	78.54	176.71	314.16	22.12	97.12	222.12	397.12

Table 3-2. Geometrical features of SPADs array

Guard ring type	**Conservative** ($\mathbf{1.6\ \mu m}$)		**Moderate** ($\mathbf{1.1\ \mu m}$)	
Optical window ($\boldsymbol{\mu m}$)	10	20	10	20
Optical area ($\boldsymbol{\mu m^2}$)	97.12	397.12	97.12	397.12

Table 3-3. Geometrical features of SPADs matrix

A simple front-end circuit, shown in Fig 3.7, has been implemented on each pixel. The SPAD is connected to a quenching transistor (M2), an enable transistor (M1), a clamping transistor (M3) and a comparator. The quenching transistor M2 acts as a resistor whose value can be modified acting on voltage V_{BQ} [74]. The enable transistor M1 is used to recharge the SPAD when the cell is active. A $1.8\,V$ comparator converts the voltage pulse from SPAD to $3.3\,V$ digital output by digitalizing SPAD pulse from M3 and comparing it to a reference voltage V_{REF} [11]. The clamping transistor M3 allows to limit the SPAD pulse voltage to $1.8\,V$ in order to protect the following digital circuits [77, 74, 76].

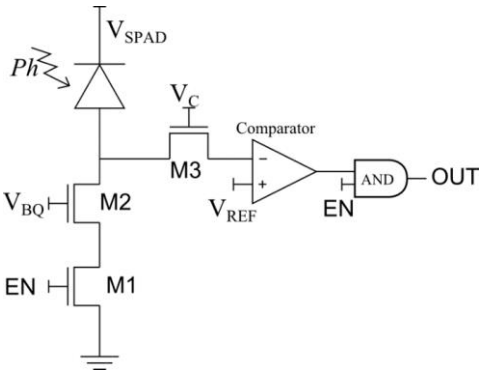


Figure 3-7. Schematic SPAD front-end circuit [76]

3.1.1 SPAD depletion region

The SPAD cross sections of PN and PWNISO layout and the relative simplified doping profile are shown in Fig. 3.8a, b. [78]. The SPAD space-charge region with W width and n-iso/substrate space charge regions with W_{sub} width are highlighted.

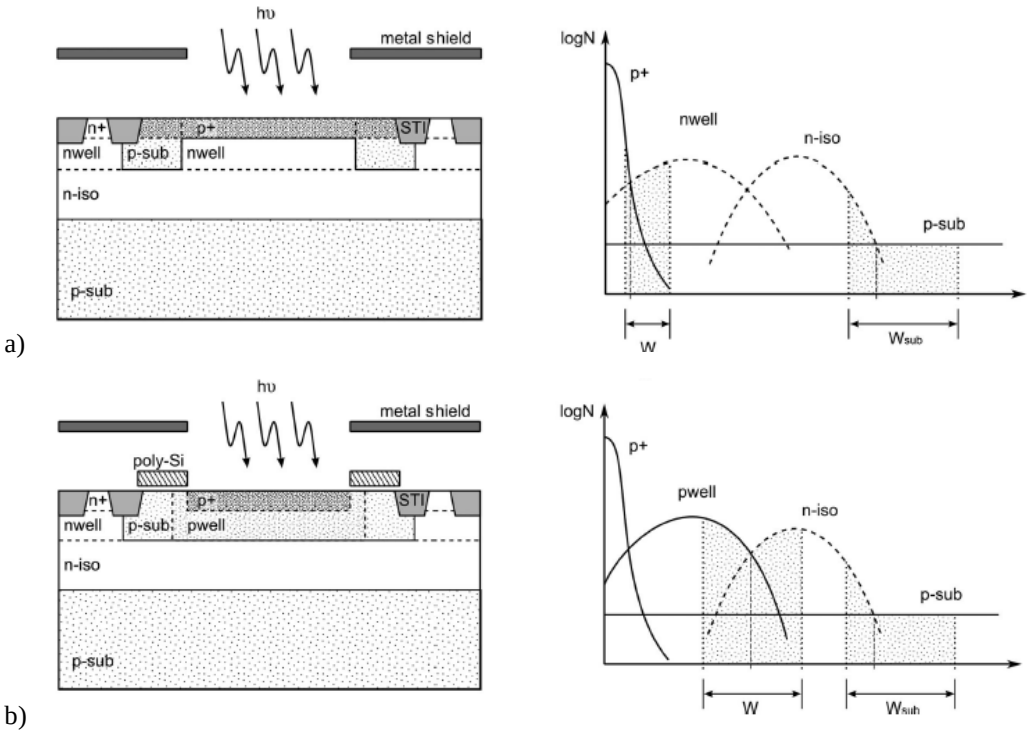


Figure 3-8. Cross section and simplified doping profile of PN (a) and PWNISO (b) layout [78]

In [78] P+/Nwell junction has been modelled with an asymmetric abrupt junction. Indeed, the presence of tunneling observed experimentally in [78] suggested that a high-peaked electric field is present in the junction, the same field shape obtained with an abrupt junction. On the contrary, Pwell/Niso junction has been modelled with a graded junction through which a smooth electric field shape is obtained [78]. Applying these models, the width of depletion region (W_D) of P+/Nwell and Pwell/Niso junction are respectively obtained by

$$W_{D\,PN} = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{qN}} \qquad (3.1) \qquad W_{D\,PWNISO} = \left(\frac{12\varepsilon_s \psi_{bi}}{qa}\right)^{1/3} \qquad (3.2)$$

with ψ_{bi} defined as the built-in potential or diffusion potential obtained by

$$\psi_{bi} \approx \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \qquad (3.3)$$

n_i the intrinsic carrier concentration in cm^{-3}, q the charge in Coulomb, N the concentration of donors (N_A) or acceptors (N_D) depending on whether $N_A \gg N_D$ or vice versa, a the doping gradient in cm^{-4} and ε_s the permittivity of semiconductor. When a voltage V is applied to the junction, the total electrostatic potential variation across the junction is given by $(\psi_{bi} - V)$ where V is positive in case of forward bias and negative for reverse bias [14].

Taking into consideration the following parameter:

$N_D = 6.20 \cdot 10^{16}\ cm^{-3}$ [78]

$N_A = 1 \cdot 10^{17}\ cm^{-3}$

$V_{PN} = 20\ V$

$V_{PWNISO} = 27\ V$

$a = 3.7 \cdot 10^{21}\ cm^{-4}$ [78]

The depletion region has been evaluated

$$W_{D\,PN} = 0.66\mu m \qquad\qquad W_{D\,PWNISO} = 0.84\mu m$$

PN layout features a thinner depletion region than PWNISO layout. These values are in good agreement with the electric field simulated in [78] (Fig. 3.9). The left edge of the space-charge region corresponds with the origin of x-axis and the simulation domain extends up to the right edge ($x = W_D$).

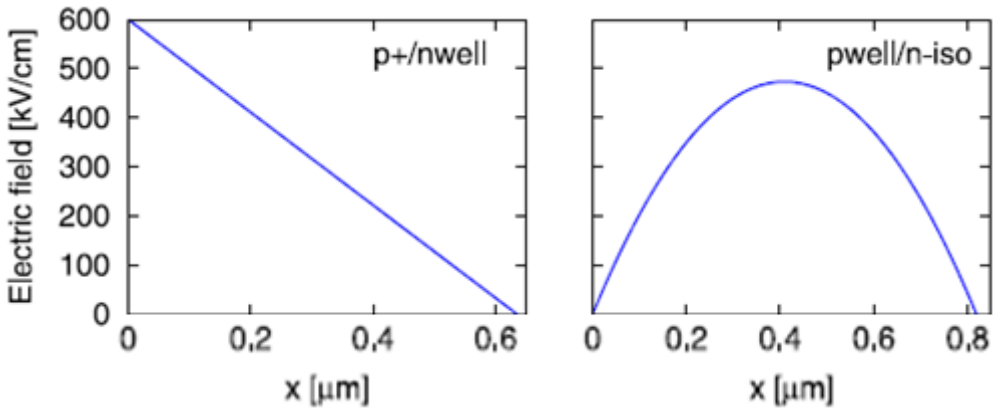


Figure 3-9. Simulated electric field in PN (left) and PWNISO (right) layout [78]

3.2 Experimental setup

Measurements of Dark Count have been performed in dark environment at room temperature. The experimental setup assembled to acquire data is schematically shown in Fig. 3.10. In order to enable a selected pixel and connect it to the output, a 25-to-1 multiplexer (MUX) has been used. A serial digital pattern has been sent to the on-chip MUX by means of an external micro-controller board Arduino. The Arduino board has been programmed to drive the chip MUX, once the digital pattern has been received via serial PC interface.

Two different circuit boards have been developed to provide right power supply to the chip. Two DC voltage generator have been employed: a Hewlett Packard

E3610a as power supply for two chip boards, and an Hewlett Packard 6634A as power supply for SPADs. The chip output signal has been sent to an oscilloscope Agilent DSO6032A and to a counter Hewlett Packard 53131A (255 MHz frequency). SPADs power supply and HP counter have been connected to a computer through GPIB serial port by means of GPIB Network adapter. This allowed to obtain a fully automatized measurement system.

A dedicated software developed in LabVIEW allowed the communication of SPAD power supply, digital counter and micro-controller with computer and gathered measurements data.

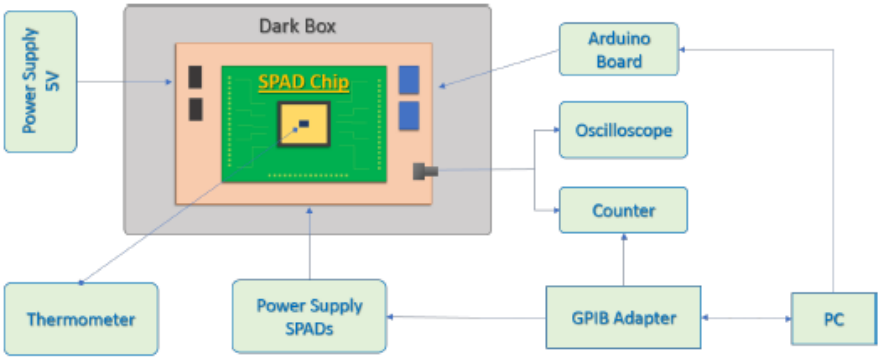


Figure 3-10. Schematic diagram of experimental setup [11, 79]

3.3 Dark Count Rate Measurements

A campaign of measurements has been carried out in order to characterize SPAD devices before irradiation test. The characterization has been performed at room temperature in dark environment obtained by a dark box placed on the chip.

This section reports the results of the characterization both of PN and PWNISO SPAD layout, in circular and square configuration. The measurements have been performed at $V_{ov} = 3\ V$.

The cumulative DCR distribution for both layouts obtained by 10 um circular and square SPADs are shown respectively in Fig. 3.11 and Fig. 3.12. It can be observed

that PN layout shows a higher DCR level (about factor two) than the one observed in PWNISO. This could be due to the different electric field shape, more peaked in PN layout. Indeed, the higher doping profile and the thinner depletion region, creates high electric field in the multiplication region.

In Table 3.4 the average DCRs of 10 um circular and square SPADs are reported. The slightly higher DCR observed in square layout is due to the larger area size.

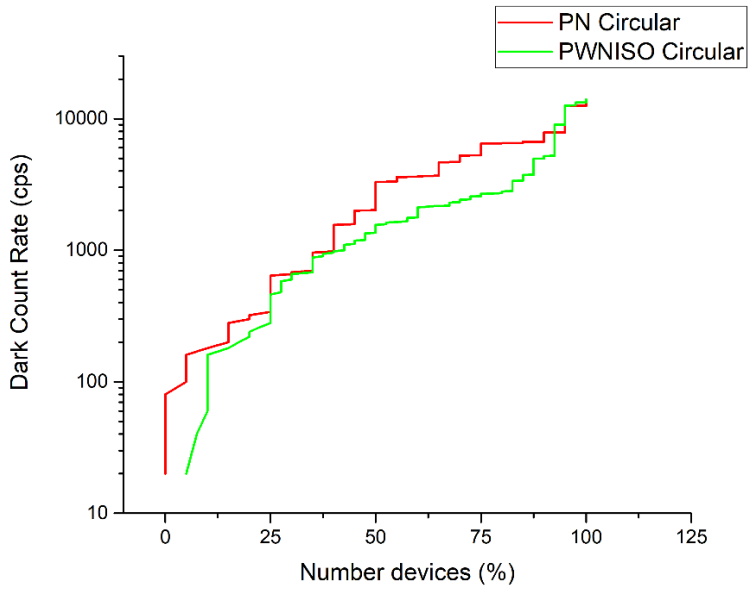


Figure 3-11. Dark Count Rate in circular PN and PWNISO layout

	PN Circular	PN Square	PWNISO Circular	PWNISO Square
Average DCR (cps)	3387	3430	1726	1927

Table 3-4. Average Dark Count Rate in circular and square layout

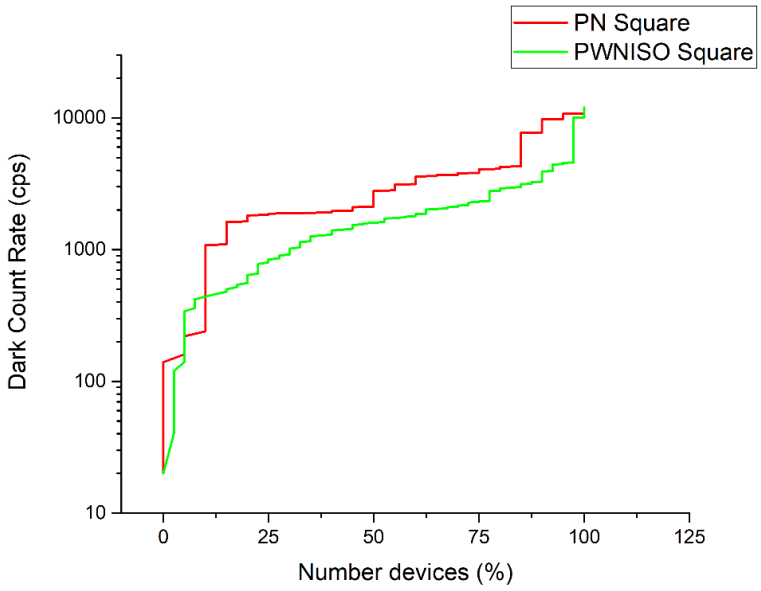


Figure 3-12. Dark Count Rate in square PN and PWNISO layout

Moreover, DCR measurements have been also performed on long observation time of 2 hours for each SPAD, in order to monitor the stability of the device response and the presence of RTS fluctuations before irradiation. In Fig. 3.13 DCR behaviour in four pixels is reported. It has been observed that the response of pixels is very stable and that only in 5 % of devices discrete fluctuations of DCR with very small occurrence probability have been observed.

A characterization as a function of temperature has been performed inserting the chip inside the climatic chamber. The measurements have been performed in the range between $-35°C$ and $40°C$ increasing the temperature by $5°C$ temperature step. The influence of temperature on DCR can give more information about the physical mechanism involved in dark count generation.

Fig. 3.14 shows the DCR distribution as a function of temperature for PN and PWNISO layout. The Fig. 3.14 confirms higher tunneling contribution in DCR in PN than in PWNISO layout. Indeed, it is clearly visible that the transition between

tunneling dominated-DCR and SRH dominated-DCR, observed by the change of slope, occurs around $15°C$ in PN layout, while around $-20\ °C$ in PWNISO layout.

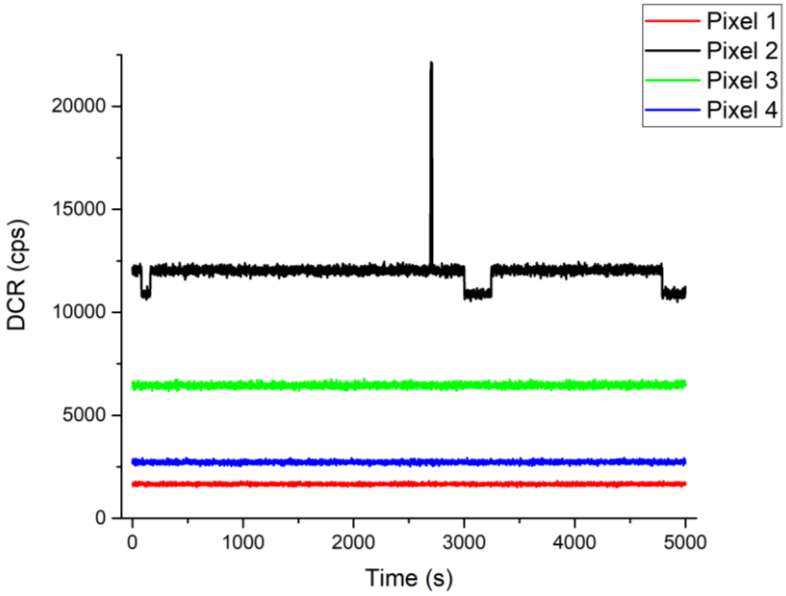


Figure 3-13. DCR vs. time behaviour of four pixels before irradiation

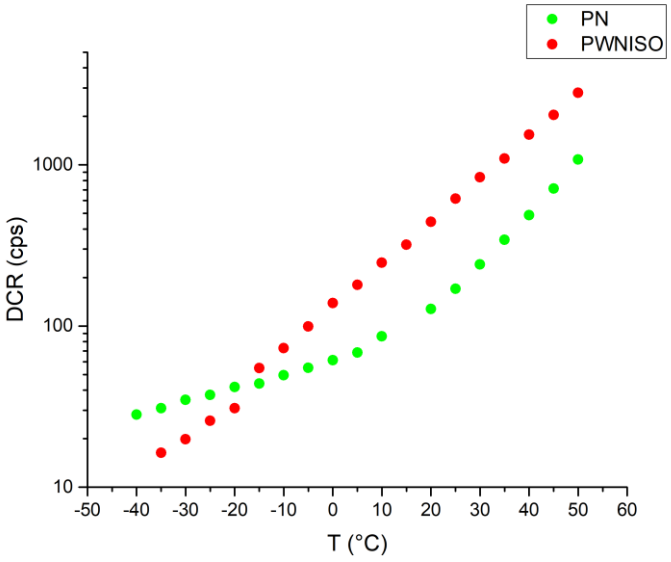
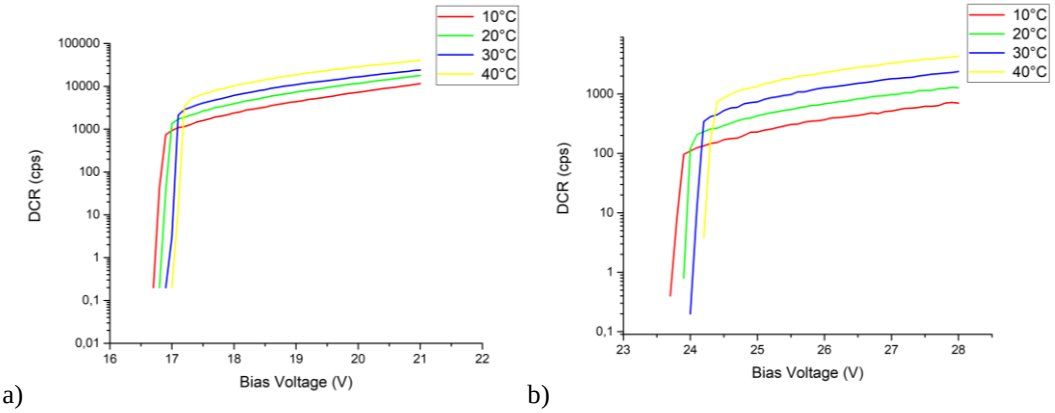


Figure 3-14. Dark Count Rate as a function of temperature in PN and PWNISO layout

3.4 Activation energy

The Fig. 3.15a, b reports the DCR distribution as a function of bias voltage in PN and PWNISO layouts for different temperatures $(10 - 40\ °C)$. Both layouts show decrease of DCR by decreasing temperature.



a) b)

Figure 3-15. Dark Count Rate as a function of Bias Voltage at different temperatures in PN (a) and PWNISO (b) layout

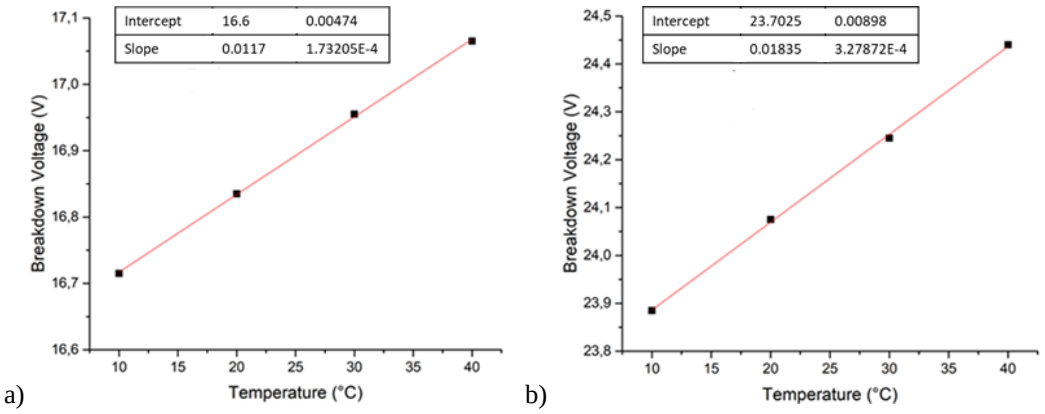
However, in order to see correctly the DCR temperature dependence in both layouts, it is necessary to refer the measurements to the same overvoltage, defined as the difference between the bias voltage and the breakdown voltage.

$$V_{OV} = V_{bias} - V_{BD} \tag{3.4}$$

The bias voltage results $19.6\ V$ for PN layout, and $27\ V$ for PWNISO one.

The breakdown voltage value has been evaluated for each SPAD by monitoring the output counts as a function of bias voltage. DCR, initially zero, begins to increase as the bias voltage increases. The value of breakdown voltage has been extracted from the curves in Fig. 3.15a, b.

The breakdown voltage as a function of temperature in two different junctions is reported in Figure 3.16a, b. From these curves, the linear distribution of breakdown voltage as a function of temperature has been extracted.

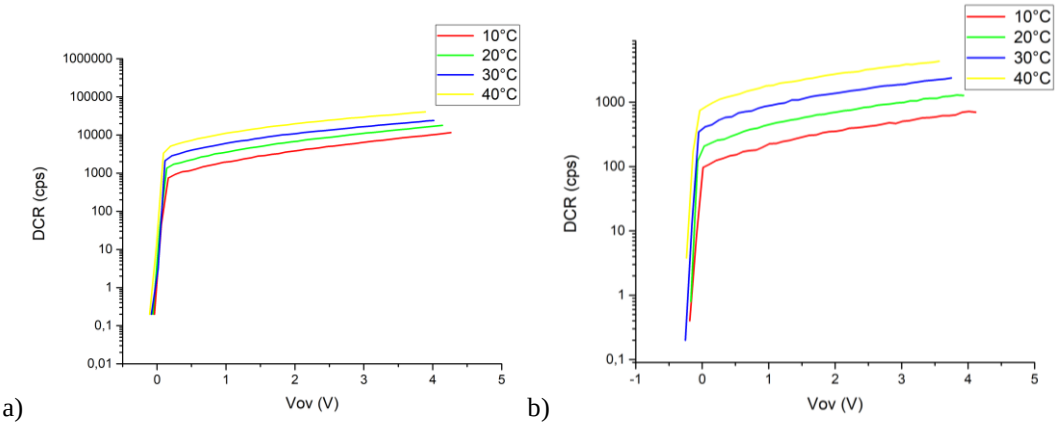


a) b)

Figure 3-16. Breakdown voltage as a function of temperature for PN (a) and PWNISO (b) layout

The breakdown voltage evaluated at $20°C$ is $16.8\,V$ for PN layout and $24.1\,V$ for PWNISO layout.

The value of breakdown voltage evaluated for each pixel at different temperatures allowed to correct the bias voltage and obtain the DCR distribution replotted at the same overvoltage in Fig. 3.17a, b.



a) b)

Figure 3-17. Dark Count Rate as a function of overvoltage at different temperatures in PN (a) and PWNISO (b) layout

The corrected DCR as a function of specific overvoltage has been extracted for each temperature. The activation energy (E_A) has been evaluated by Arrhenius equation

$$DCR = Ae^{-\frac{E_A}{k_B T}} \tag{3.5}$$

where k_B is Boltzmann's constant, A is a constant, and T is the absolute temperature [80]. The activation energy evaluation provides an important tool to investigate the mechanism leading to the generation of dark counts generation, indicating the dark counts origin, i.e. if it is due to diffusion of minority carriers, or to generation process from SRH centers, or from tunneling mechanism [80, 81]: if E_A is close to the bandgap energy ($E_A = E_G = 1.12eV$), the diffusion of thermally generated minority carriers from neutral region contributes to DCR, if E_A is close to the mid bandgap energy ($E_A = E_G/2$) the generation of dark counts is mainly due to traps with ionization energy close to the mid bandgap value acting as SHR centers [80, 81], if E_A is lower than the mid bandgap energy, electric field enhancement contributes to decrease the barrier height and therefore, the activation energy.

The Fig. 3.18 and Fig. 3.19 show the Arrhenius plot ($\ln(DCR)\ vs\ 1/k_B T$) respectively of PN and PWNISO layout at $V_{ov} = 3\ V$. The slope of the curve results the activation energy value.

In two pixels reported in Fig 3.18 and 3.19, as in almost all pixels, it is possible to extract two different slopes from Arrhenius plot. The transition point between two regions is around $15°C$ in PN layout and $-20°C$ in PWNISO. The activation energy value for each pixel are reported in Table 3.5.

Layout	**Activation energy** $[eV]$ T_{low}	**Activation energy** $[eV]$ T_{high}
PN	0.12 ± 0.01	0.58 ± 0.02
PWNISO	0.22 ± 0.01	0.43 ± 0.01

Table 3-5. Activation energy values for PN and PWNISO layout at positive and negative temperatures

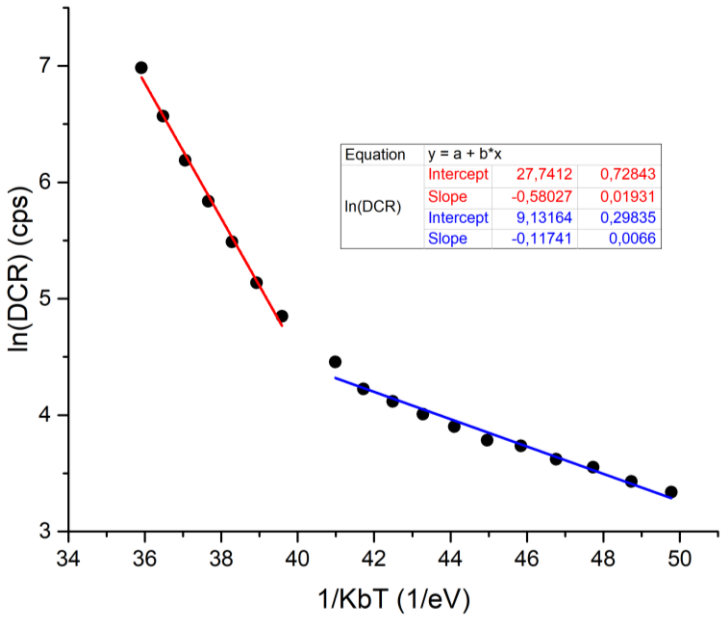


Figure 3-18. Arrhenius plot of PN SPAD at Vov=3V

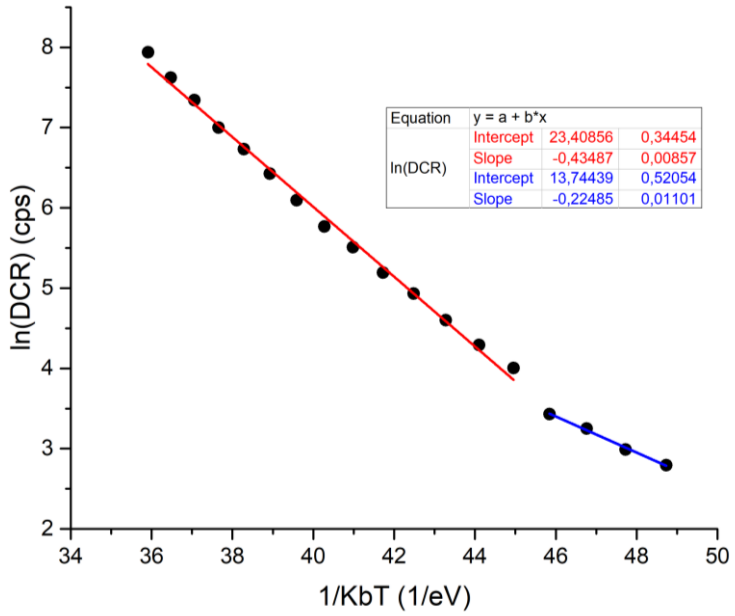


Figure 3-19. Arrhenius plot of PWNISO SPAD at Vov=3V

Both PN and PWNISO layout show a lower activation energy at low temperatures. This is due to the prevalence of tunneling contribution in DCR generation at low temperature. On the contrary, activation energy increases at high temperature, due to the presence of traps with ionization energy close to the mid bandgap value acting as SRH centers. Focusing only on T_{high}, the activation energy has been evaluated on all pixels with the aim to obtain an estimation of the activation energy with higher statistics and to investigate its spread in two layouts. The average activation energies obtained by 60 PN and 160 PWNISO pixels have been measured respectively $0.35\ eV$ and $0.50\ eV$.

The Fig. 3.20 shows the distribution of activation energy as a function of DCR at $20°C$. In both layouts, the activation energy decreases by increasing dark count rate. This behaviour results a clear evidence of electric field enhancement effects, as reported in [71]. The activation energies are lower than the mid bandgap value that is the classical SRH activation energy evaluated without electric field enhancement [33, 82]. Therefore, this means that electric field enhancement mechanisms, such as Poole-Frenkel effects, are involved in the physics of the DCR generation, resulting in the decrease of the barrier to tunnel through. In particular, PN layout shows a lower activation energy with respect to PWNISO layout. Indeed, the PN higher doping concentrations and the smaller junction dimension in PN layout create higher electric field in the multiplication region.

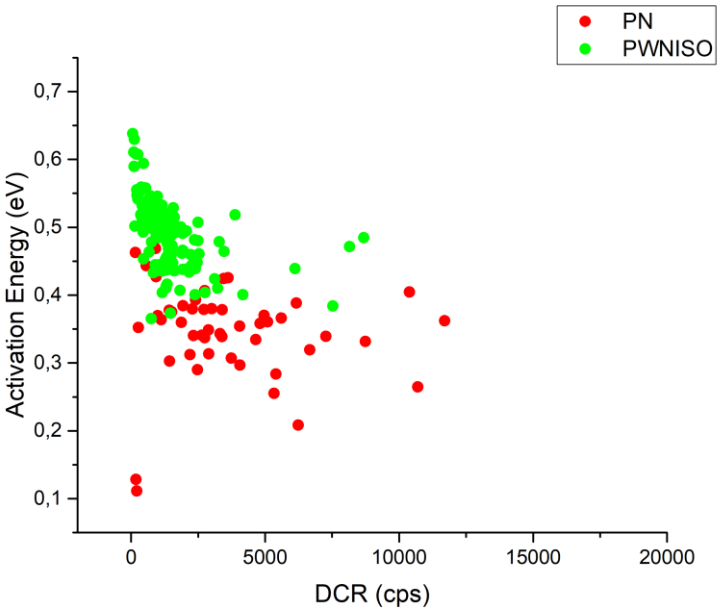


Figure 3-20. Activation energy as a function of Dark Count Rate at 20°C for different PN and PWNISO pixels

4.Random Telegraph Signal Investigation

Introduction

This chapter shows all results obtained by a long-lasting analysis performed on RTS behaviour on CMOS SPADs devices. The investigation has been focused on RTS behaviour on two different proton-irradiated SPAD layouts.

The test chips have been irradiated at Laboratori Nazionali del Sud (LNS) – Istituto Nazionale di Fisica Nucleare (INFN) in Catania.

After proton irradiation dark count rate measurements have shown, not only an average increase of DCR of almost one order of magnitude, but also the occurrence of two or multi-level RTS, both in PN and PWNISO layout. RTS pixels have been analysed both in time and frequency domain.

The classification of RTS pixel proved that the number of RTS pixels with more than two levels is significantly greater than the number of two levels RTS pixel. Moreover, higher RTS occurrence probability is observed in PN than in PWNISO layout. Several hypotheses related to the different electric field magnitude in two layouts and to the different generation mechanisms involved in the DCR increase, have been formulated to justify different RTS behaviours.

In order to investigate deeply the RTS behaviour in PN and PWNISO layout, a deep investigation has been performed on four 2-level RTS pixels for each layout, PN and PWNISO. RTS time constants and amplitude as a function of voltage and temperature have been analysed. An exponential distribution has been found for time of occupancy of two levels, as foreseen by a Poissonian distribution of random switching events. To obtain reasonable estimation of time constant values, a sufficient number of RTS transitions (> 100) has been acquired, resulting in data acquired from several hours to days for each pixel at a given temperature. The RTS time constants have been measured in the climatic chamber in the range $10\ °C - 45\ °C$.

The time constants activation energy value has suggested that RTS origin could be linked to the vacancy relative to the phosphorous atom (P-V defect). Moreover, the annealing analysis is described in the chapter. Since each defect has an annealing temperature, isochronal annealing has been performed to study the annealing of point defects. Annealing process has provided a further insight in the identification of defects responsible for RTS effect.

4.1 Proton irradiation test

The irradiation tests have been performed at Tandem accelerator and at Cyclotron accelerator in Laboratori Nazionali del Sud (LNS) – Istituto Nazionale di Fisica Nucleare (INFN), in Catania (Italy).

Five chips, identified with number 4, 5, 10, 15, N2 have been irradiated with proton beam: chip 4 and chip 5 have been irradiated at Tandem accelerator, while chip 10, 15 and N2 have been irradiated at Cyclotron accelerator at different energy.

For irradiation test at Tandem accelerator, 24 MeV proton beam has been extracted in air through $50\ \mu m$ kapton window in the 80° beam line.

A pneumatic beam stopper has been assembled in front of kapton window in order to have the remote control on the beam line. The beam stopper consists of a thick lead disk, driven by an actuator, inserted between the kapton window and the boarding test in which the chip is mounted. The chip has been fixed in an aluminum frame and aligned with the beam line. In order to monitor continuously the alignment of the beam on DUT, fluorescent strips have been fixed as a frame around the DUT. A webcam pointed on chip for all irradiation test allowed to check the position of the beam inside the fluorescent frame, exactly on DUT (Fig. 4.1 a, b).

As shown in Fig. 4.1, an ionization chamber has been placed between the kapton window and the pneumatic beam stopper to monitor the proton beam intensity during irradiation test and to adjust it before each irradiation. The ionization chamber is made by two parallel plates separated by $9\ mm$ air and constituted by

25 μm kapton layer coated by 5 μm copper layer. The ionization chamber is 800 V polarized and it provides an output current signal related to the intensity of the beam that crosses it.

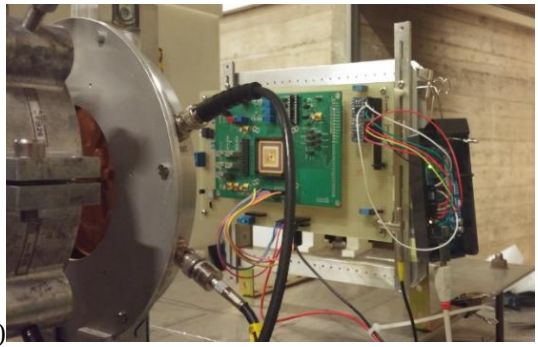
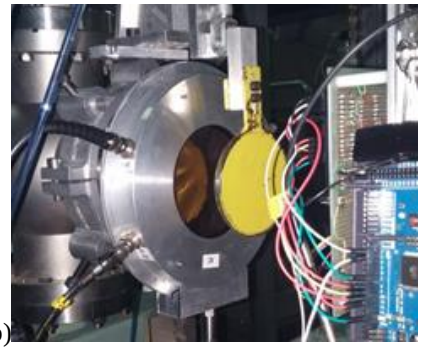
a)  b) 

Figure 4-1. Proton irradiation test at Tandem accelerator: experimental setup with the boarding test (a) and the beam stopper and ionization chamber on the beam line (b)

The ionization chamber has been calibrated before irradiation test. A thick lead plate, able to absorb the proton beam, has been placed on DUT position and connected through a picoammeter to the ground. The current induced by proton beam on the plate has been measured by picoammeter. By dividing the current by the electron charge, the number of stopped protons has been obtained.

The calibration is obtained by measuring simultaneously the current on the lead plate and the output of the chamber. The linear correlation coming from calibration is shown in Fig. 4.2.

The amount of charge delivered on chip for each run is evaluated by integrating each second the beam current measured according to calibration. The amount of charge allows to know the proton beam fluence ($protons/cm^2$).

In order to measure the beam intensity profile, a GAFchromic (GAF) film EBT3 has been irradiated at the same DUT irradiation condition and at DUT position (Fig. 4.3).

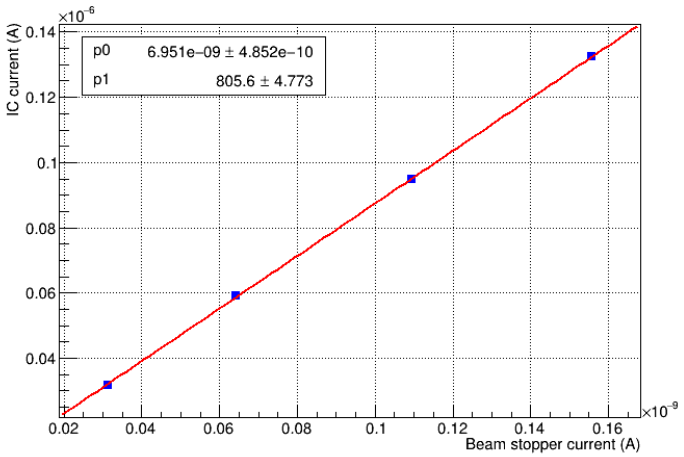


Figure 4-2. Ionization chamber output current vs. beam current [11]

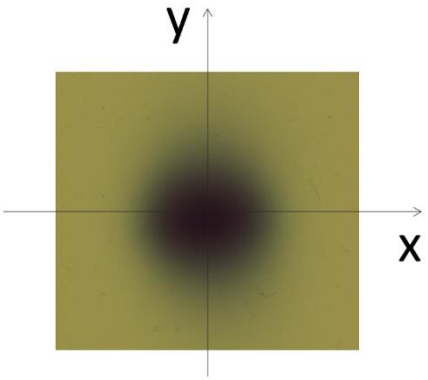


Figure 4-3. GAFchromic film EBT3 impressed by proton beam [11]

Applying the calibration reported in [83], the dose profile of GAF shown in Fig. 4.4 is obtained. Being the proton beam monochromatic, the dose scales with fluence as follows

$$D \propto \Phi \cdot \frac{1}{\rho}\frac{dE}{dx} \tag{4.1}$$

Being the beam intensity profile proportional to dose profile in Fig. 4.4, it has been possible to evaluate that the beam intensity non-uniformity on the chip surface is below 10%.

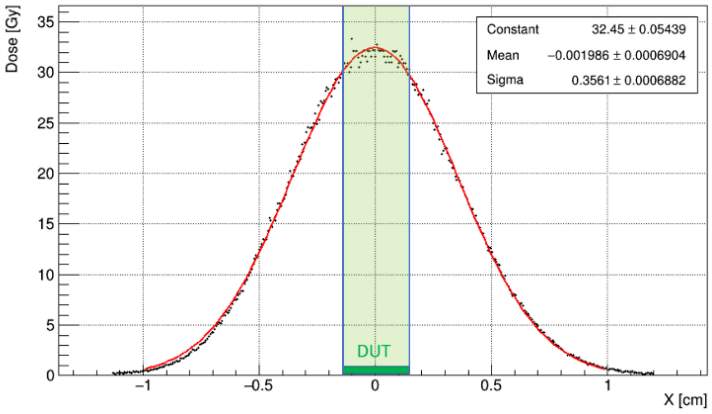


Figure 4-4. Dose profile of irradiated GAF EBT3 [11]

The fluence on SPADs chip is obtained by dividing the charge on DUT (Q_{DUT}) by its area (A_{DUT}) and by the elementary charge (q_e).

$$\Phi[p/cm^2] = \frac{Q_{DUT}}{A_{DUT} \cdot q_e} \tag{4.2}$$

24 MeV proton beam has been extracted in air through 50 μm kapton window assembled in the beam line. Taking into consideration the energy loss in 50 μm kapton window, the amount of air, the ionization chamber and the quartz cover of the chip, the mean energy on DUT has been evaluated 20.49 MeV by both SRIM and FLUKA packages [11].

The irradiation tests have been performed in two runs for chip 5, as reported in Table 4.1, and one run for chip 4.

	Charge $[C]$	**Fluence** $[p/cm^2]$
***RUN* 1**	$2.46 \cdot 10^{-9}$	$1.80 \cdot 10^{10}$
***RUN* 2**	$5.05 \cdot 10^{-9}$	$5.63 \cdot 10^{10}$

Table 4-1. Chip 5 proton irradiation runs

The Total Ionizing Dose (TID) has been evaluated as

$$TID\ [Gy] = 1.6 \cdot 10^{-10} LET \cdot \Phi \tag{4.3}$$

where LET has been obtained by means of SRIM evaluations considering $20.49\ MeV$ proton beam in silicon.

The Displacement Damage Dose (DDD) has been evaluated as

$$DDD = NIEL \cdot \Phi \tag{4.4}$$

where NIEL has been evaluated by a web-tool NIEL calculator [84].

The chip 10, 15 and N2 have been irradiated at Cyclotron accelerator with $62\ MeV$ proton beam extracted in air (Fig. 4.5). Taking into consideration the energy loss along the beam line, the proton beam energy on the chip 10 and N2 has been estimated around $60\ MeV$. The test performed on chip 15 has been carried out with $32\ MeV$ protons by degrading the primary beam by means of an aluminum absorber.

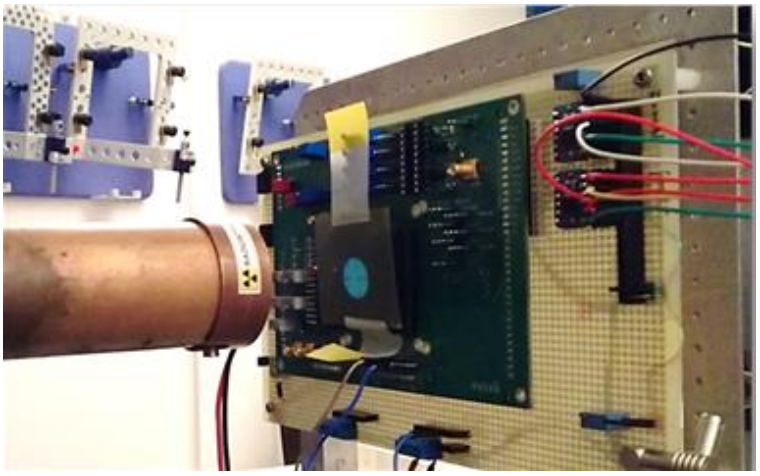


Figure 4-5. Proton irradiation test at Cyclotron accelerator

The irradiation tests have been performed in three runs for chip 10 and one run for chip 15 and N2.

TID and DDD evaluated for all chips are reported in Table 4.2.

Sample	Run	Reached Fluence $[p/cm^2]$	TID [krad]	DDD [Tev/g]
***Chip* 4**		$9.10 \cdot 10^{10}$	30.5	608.1
***Chip* 5**	1	$1.80 \cdot 10^{10}$	5.6	120.3
	2	$5.63 \cdot 10^{10}$	17.5	376.2
***Chip* 10**	1	$2.52 \cdot 10^{10}$	3.5	101.4
	2	$5.04 \cdot 10^{10}$	6.9	202.8
	3	$7.56 \cdot 10^{10}$	10.4	304.2
***Chip* 15**		$5.63 \cdot 10^{10}$	12.5	303.6
Chip N2		$2.90 \cdot 10^{10}$	5	115

Table 4-2. Total Ionizing Dose (TID) and Displacement Damage Dose (DDD) for analysed pixels

4.2 DCR characterization post irradiation

The Dark Count Rate as a function of Displacement Damage Dose has been evaluated on 10 μm active region SPADs of all irradiated chips. Fig. 4.6 reports DCR as a function of DDD of chip 4, 5, 10 e 15, showing the proportionality of damage effects in silicon with DDD.

The chip 5 has been characterized between and after each proton irradiation runs. The Fig. 4.7 shows the Dark Count Rate cumulative distribution for 25 SPADs with 10 μm active region at $V_{ov} = 3.4\ V$ before irradiation, after each run and one and

two months after irradiation. After the second irradiation run, an average DCR increase of about one order of magnitude has been measured. However, after a month, a natural DCR recovery has been observed, indicating that some defects annealing occur at room temperature. No further DCR reduction has been observed after two months with respect to the measurements performed after one month. This indicates that room temperature annealing ends its effect.

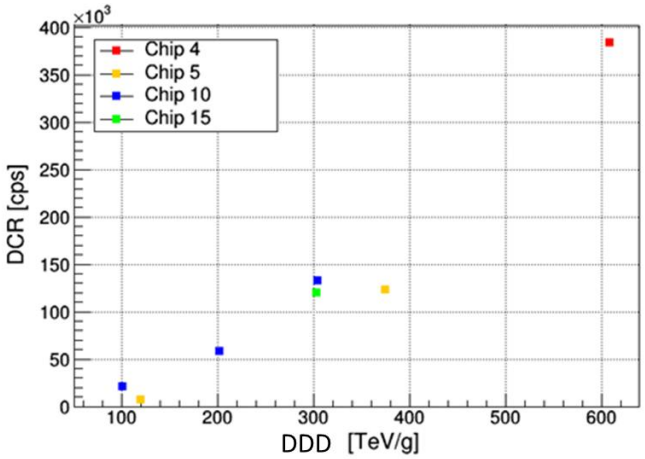


Figure 4-6. Mean DCR as a function of Displacement Damage Dose on several protons irradiated chips [85]

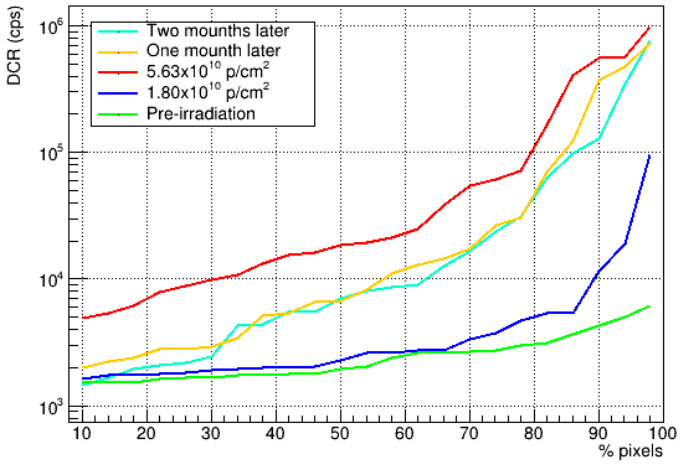


Figure 4-7. DCR cumulative distribution for 25 SPADs with 10 μm active region at $V_{ov} = 3.4\ V$ [85]

4.3 RTS in time and frequency domain

After proton irradiation RTS has been evaluated on SPADs under test in frequency and time domain.

As explained in Section 2.6.2, in frequency domain the power spectral density can give more information about the signal nature. Indeed, if DCR is due respectively to Flicker noise or RTS, the slope of $1/f$ or $1/f^2$ can be recognized in PSD. However, RTS pixels under study have shown a slope much closer to $1/f$ than $1/f^2$ (Figure 4.8). The reason for which Flicker noise dominates on $1/f^2$ slope is still under investigation.

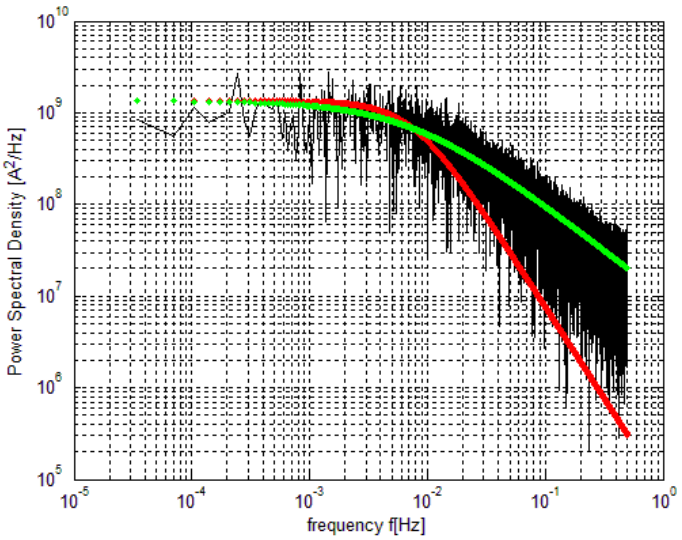


Figure 4-8. Power Spectral Density of RTS pixel with 1/f (green) and 1/f^2 slope (red)

As in the frequency domain RTS event is defined by the corner frequency (f_c) and the plateau value (P), RTS can be also described in time domain by three parameters: τ_{up}, τ_{down} and the amplitude A_{RTS}, as introduced in Section 2.6.1 [48]. RTS analysis consists mainly in the evaluation of RTS parameters above described, since they allow to know the mechanism involved in RTS. However, if the dark current fluctuations between two dark discrete levels (bi-level RTS), can be easily analysed by evaluating the RTS characteristics, the analysis becomes more

complicated if the fluctuations have a composite structure (multi-level RTS). Unfortunately, bi-level RTS are less probable with respect to multi-level RTS [86]. In general, RTS events are due to superposition of several levels coming from multi-level sources, or independent bi-level sources, or combination of both [86, 87]. Several type of RTS observed in SPAD under test are shown in Fig. 4.9.

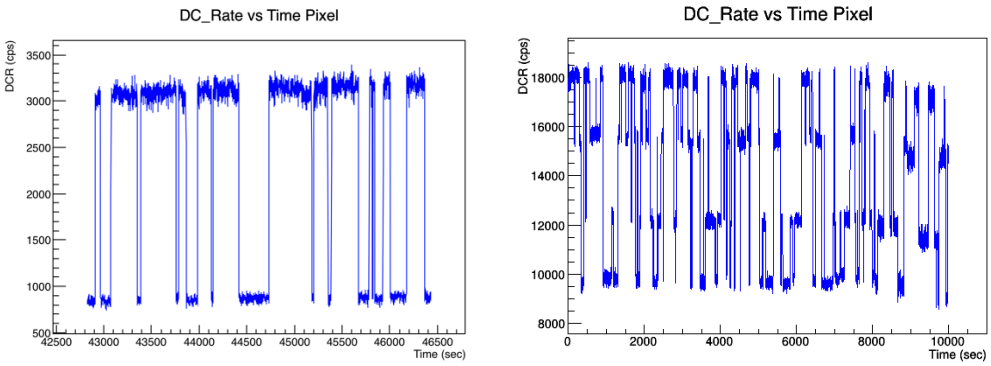


Figure 4-9. Bi-level RTS (left) and multi-level RTS behaviour (right)

The time distribution of high and low level shows an exponential behaviour according to the following law [51, 88]:

$$P_{up,down}(t) = \frac{1}{\tau_{up,down}} \cdot exp\left(\frac{-t}{\tau_{up,down}}\right) \tag{4.5}$$

with $P_{up,down}$ the probability of high or low level in a typical RTS [19].

Fig. 4.10 shows the dark count rate of a bi-level RTS pixel. The time distribution of this bi-level RTS pixel are reported in Fig. 4.11.

The time constants obtained are reported below

$$\lambda_{down} = 0.01880\ s^{-1} \qquad \lambda_{up} = 0.00544\ s^{-1}$$

$$\tau_{down} = \frac{1}{\lambda_{down}} = 53.19\ s \qquad \tau_{up} = \frac{1}{\lambda_{up}} = 183.82\ s$$

The values obtained by exponential fitting are in good agreement with the ones obtained by dividing the total up and down time by the number of transitions between the levels

$$\tau_{down} = 53.17\ s \qquad\qquad \tau_{up} = 184.4\ s$$

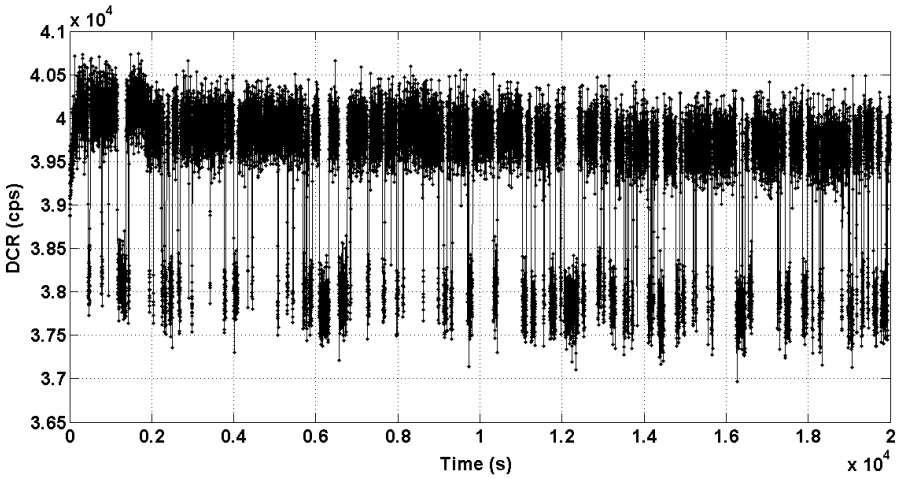


Figure 4.10. Dark Count Rate as a function of time in RTS pixel

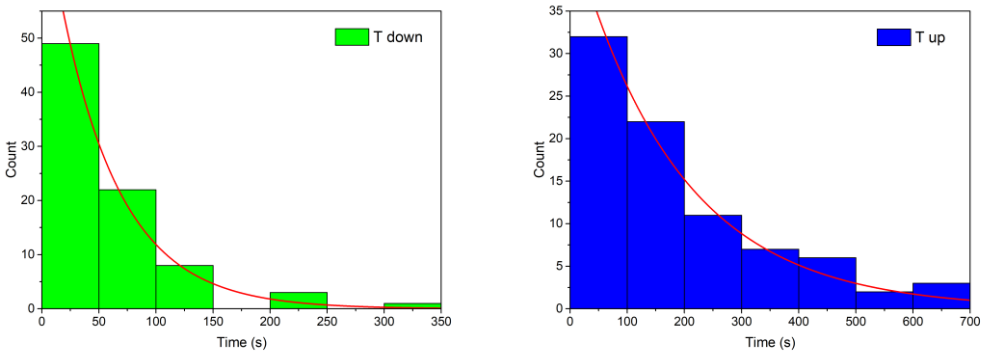


Figure 4-11. Time up and time down distribution of bi-level RTS pixel

The RTS characteristics, both time constant and RTS amplitude, vary according to temperature changes [71]. The dependence of time constants ($\tau_{up,down}$) by temperature follows the Arrhenius law, obtained by [54]:

$$\frac{1}{\tau_{up,down}} = A\ exp\left(-\frac{E_{act\ time}}{k_B T}\right) \tag{4.6}$$

with A is the rate constant, $E_{act\ time}$ the time constant activation energy, k_B is the Boltzmann's constant and T is the temperature in Kelvin. Therefore, as the temperature increases, not only RTS switches more rapidly [87], as deduced from Eq. 4.6, but also the transition amplitude between the levels becomes larger (Fig. 4.12) [67]. Plotting the natural logarithm of RTS amplitude as a function of $1/k_B T$, it is found experimentally that the RTS amplitude (A_{RTS}) follows also the Arrhenius law

$$\frac{1}{A_{RTS}} = C\ exp\left(-\frac{E_{act\ amp}}{k_B T}\right) \tag{4.7}$$

with $E_{act\ amp}$ the amplitude activation energy, C a non-thermal constant [67]. Arrhenius plot allows to extract the activation energy of the centers from the slope of the curve.

It is important to underline that the activation energy for time constants and RTS amplitude relates to different physical mechanisms. The time constants activation energy represents the energy barrier that a defect has to overcome to switch between different structural configurations [86]. The amplitude activation energy relates to changes in dark current generation due to the temperature [86] and suggests the DCR generation mechanism: if the activation energy is close to silicon energy bandgap ($E_G = 1.12\ eV$), the DCR generation mechanism is dominated by diffusion of minority carriers, while if the activation energy is close to silicon mid gap, SRH generation is due to the presence of mid gap defects [11].

Another way to extract RTS amplitude and time constants consists in the ranking of current by means of a histogram. Indeed, taking into account a simple bi-level signal, this results in two Gaussian distributions, in which the peak of each distribution indicates the high and low level (Fig. 4.13). Therefore, the difference

between the DCR values corresponding to the two peaks provides the RTS amplitude, while the ratio of the areas under two distributions gives the average time constant, τ_{up}/τ_{down} (or τ_{down}/τ_{up}) [51].

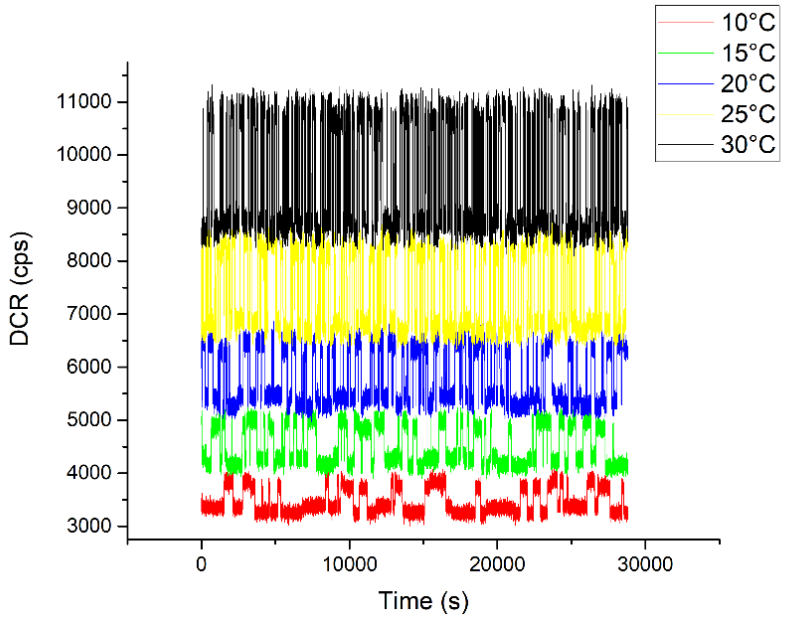


Figure 4-12. Variation of time constants and amplitude by changing the temperature

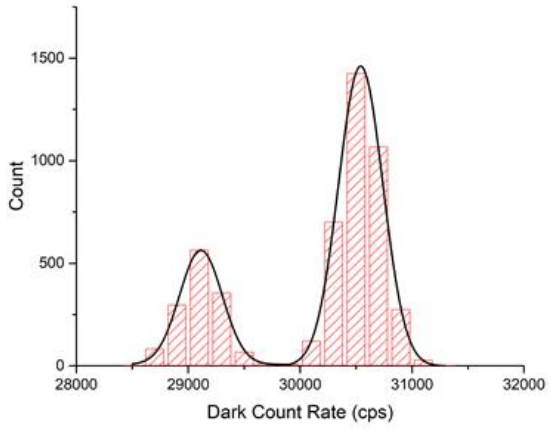


Figure 4-13. Bi-levels RTS Gaussian curve

Alternatively, taking in consideration the frequency domain, it is possible to combine the histogram with the current noise power spectral density to extract RTS parameters:

$$S = \frac{A_0}{1 + \left(\frac{f}{f_c}\right)^2} \tag{4.8}$$

with S the power spectral density (PSD), A_0 the plateau amplitude at low frequency f and f_c the corner frequency, the frequency above which the spectral density rolls off as $1/f^2$ [89]. The corner frequency can be obtained multiplying the PSD spectrum times f, obtaining a peak versus frequency with maximum at f_c.
The corner frequency is correlated to the time constants as follows:

$$2\pi f_c = \frac{1}{\tau_{up}} + \frac{1}{\tau_{down}} \tag{4.9}$$

Therefore, combining the time constant ratio obtained from the histogram and the Eq. 4.9, it is possible to extract the average RTS time constants. However, the most direct method to characterize RTS is based on measurements in the time domain rather than in the frequency domain [51].
Moreover, applying TLP, introduced in Section 2.6.3, RTS characteristics can be also evaluated. RTS amplitude can be obtained from the distance between the centers of data points clouds and the ratio between τ_{up} and τ_{down} can be extracted from the ratio of counts that are in clouds corresponding to level up and down. Combining TLP with noise spectrum or time measurements, RTS parameters can be simply extract [51].
Some example of bi-levels and multi-levels RTS observed in irradiated chips are reported respectively in Fig. 4.14 and Fig. 4.15 a, b.

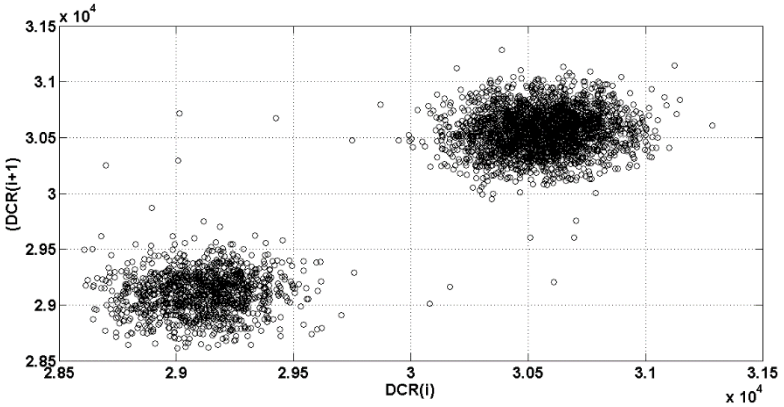
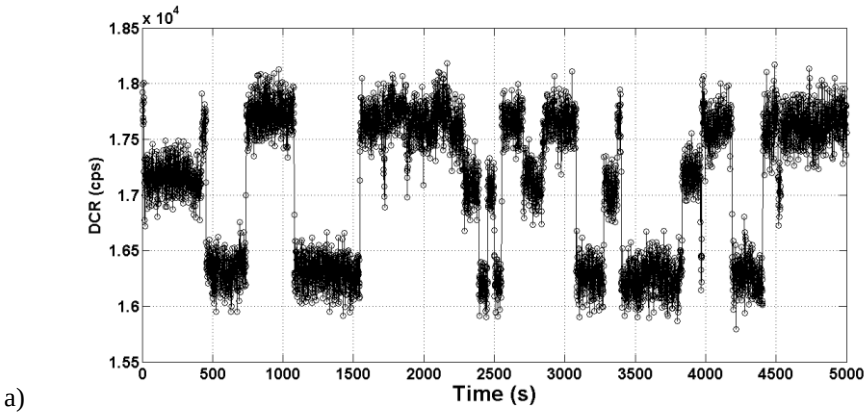
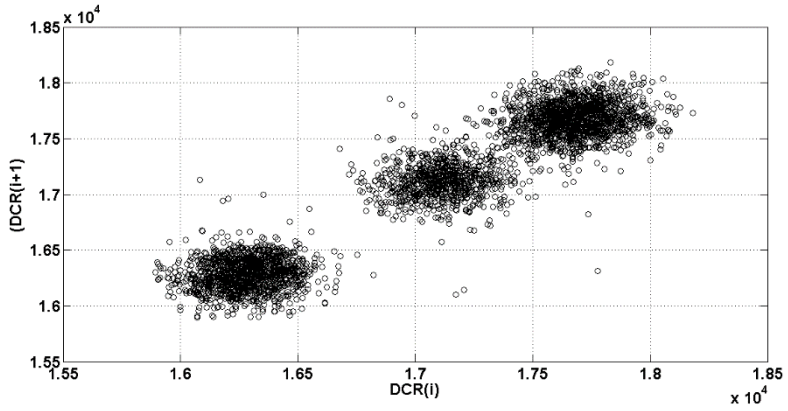


Figure 4-14. TLP of bi-level RTS in Fig. 4.10



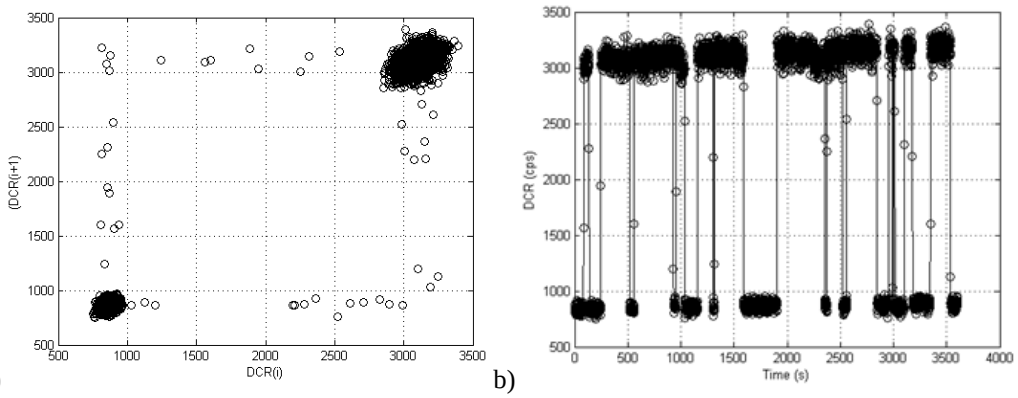
a)



b)

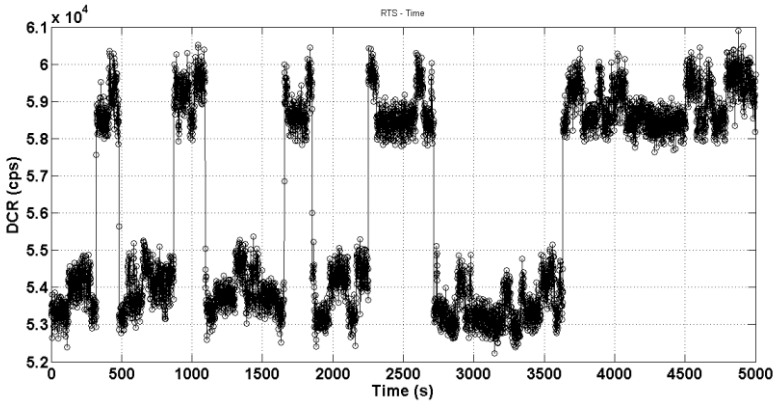
Figure 4-15. a) Three Levels RTS and b) the corresponding TLP

If a data is acquired during the transition between the levels, it will appear among the off-diagonal data points, shaping a kind of frame, as shown in Fig. 4.16a. Moreover, TLP can give important information even in case of additional noise sources or presence of multi-traps. As shown in Fig. 4.17b, TLP proves that each of two levels contains other two levels, resulting in four levels RTS. 2 clouds of data points in each cloud can be recognized. Indeed, RTS signal as a function of time (Fig. 4.17a) shows that the two levels in high and low levels are nearly overlapped.



a) b)

Figure 4-16. a) Bi-levels RTS and b) corresponding TLP



a)

b)

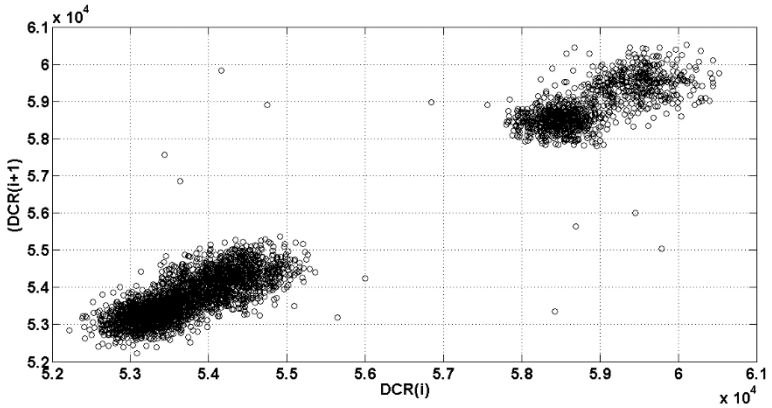


Figure 4-17. a) Bi-levels in bi-levels RTS and b) corresponding TLP

4.4 RTS measurements

The Random Telegraph Signal behaviour of Dark Current Rate has been investigated after proton beam irradiation in chip 5, 10 and N2. RTS behaviour has been analysed through measurements performed in climatic chamber at $20°C$ for one hour per pixel in order to clearly recognize RTS behaviour. Since data acquisition allows to analyse only one pixel per time, the analysis of 1 hour per SPAD required long measurements campaign to characterize all SPADs in three test-chips. DCR of each SPAD has been analysed to classify SPADs showing RTS behaviour. Moreover, among RTS SPADs, an accurate classification of the number of levels in which RTS fluctuates (two, three, four, five and more than five levels) has been performed. The results are reported in Table 4.3, 4.4 and 4.5, respectively for chip 5, 10 and N2. As mentioned in Section 4.3, the analysis proves that bi-levels RTS are less probable; the number of RTS pixels with more than two levels is greater than the number of bi-levels RTS pixels, as observed also in [67].

Layout	Analysed SPADs	RTS pixels	2 levels	3 levels	4 levels	≥5 levels	RTS fraction
PN	139	118	17	11	8	82	**85**%
PWNISO	321	186	34	15	8	129	**58**%

Table 4-3. Classification of RTS pixels and of the number of RTS levels in two layouts in chip 5

Layout	Analysed SPADs	RTS pixels	2 levels	3 levels	4 levels	≥5 levels	RTS fraction
PN	124	80	31	11	5	33	**65**%
PWNISO	334	190	51	19	16	104	**57**%

Table 4-4. Classification of RTS pixels and of the number of RTS levels in two layouts in chip 10

Layout	Analysed SPADs	RTS pixels	2 levels	3 levels	4 levels	≥5 levels	RTS fraction
PN	118	65	18	10	10	27	**55**%
PWNISO	334	131	34	9	13	75	**39**%

Table 4-5. Classification of RTS pixels and of the number of RTS levels in two layouts in chip N2

A higher RTS occurrence probability has been observed in PN with respect to PWNISO layout in all three chips. This behaviour suggests that more intense electric field in the junction can have a role not only in higher levels of DCR, but also in higher RTS occurrence. Indeed, the higher doping concentration at the junction causes a higher electric field magnitude in P+/Nwell than in Pwell/Niso junction. This results in the enhancement of RTS behaviour, making visible more RTS levels. Moreover, similar results have been obtained in chip 5 and 10, exposed to a similar DDD, but at different energy. Regarding the chip N2, RTS fraction results lower with respect to RTS fraction on other chips according to the lower DDD ($115\ TeV/g$). This means that the RTS occurrence depends on the accumulated DDD.

In order to investigate the correlation between DCR distribution and RTS occurrence, Fig. 4.18 shows the total DCR distribution of SPAD pixels and the DCR distribution of RTS pixel at $20\ °C$. The Figure proves that almost all high

DCR pixels show RTS behaviour, while only a fraction of pixels with lower DCR exhibits RTS.

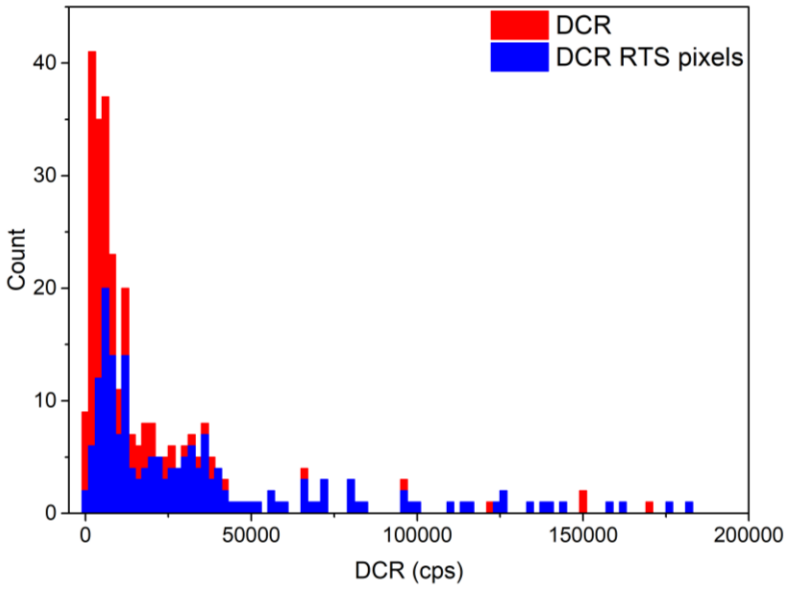
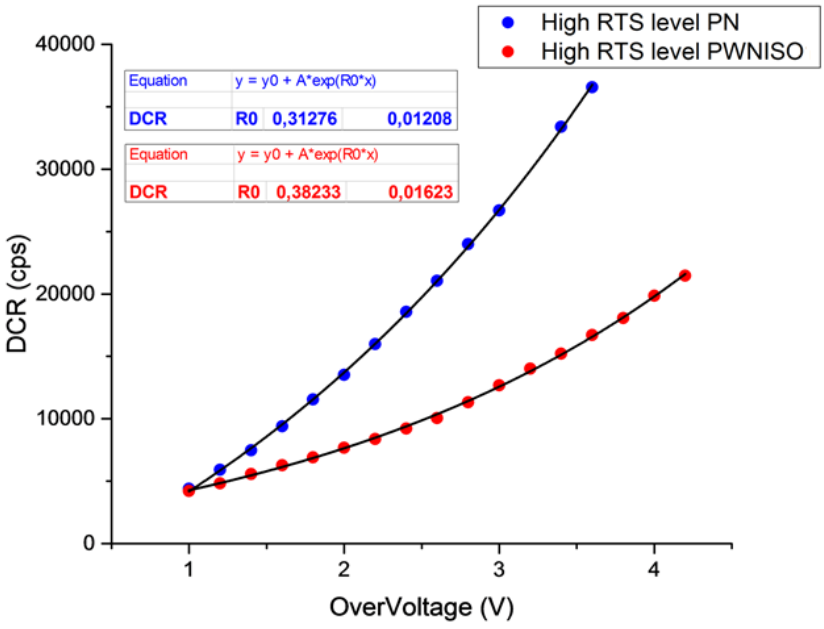


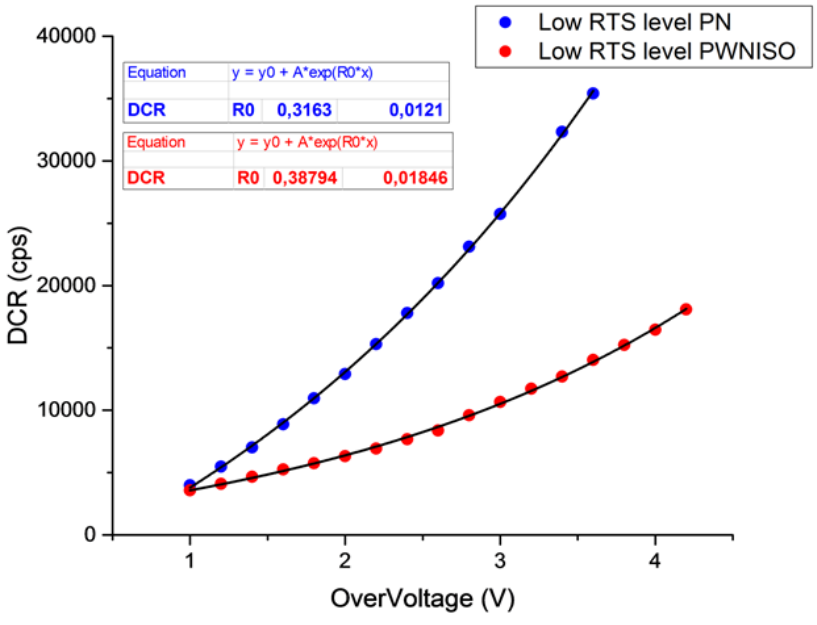
Figure 4-18. Dark Count Rate histogram for all pixel population (red) and for RTS pixel (blue)

4.5 RTS amplitudes

In order to better investigate the influence of electric field on RTS in two layouts, DCR in high and low level has been investigated as a function of overvoltage (Fig. 4.19a, b). The Figures 4.19a, b prove that DCR is strongly influenced by overvoltage. Both layouts show an increase of DCR as a function of overvoltage. DCR shows a greater increase in PN than in PWNISO layout, especially at high overvoltage.



a)



b)

Figure 4-19. Dark Count Rate vs. OverVoltage in PN and PWNISO pixel in High (a) and Low (b) RTS level

Fig. 4.20 shows also two-levels RTS PWNISO pixel as a function of bias voltage obtained by increasing the bias voltage by $0.2\,V$ step between $24.8\,V$ and $28.2\,V$.

The RTS amplitude results clearly bias dependent and it increases by increasing the bias voltage.

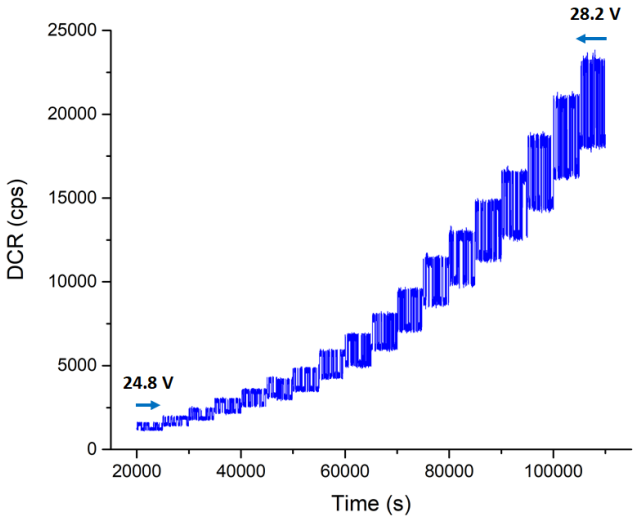


Figure 4-20. RTS behaviour at different SPAD reverse bias with 0.2 V increasing step.

Fig. 4.19 and 4.20 prove that RTS mechanism is electric field dependent, as found in [58]. From Fig. 4.19a, b it is clear that the electric field enhancement, involved in both layouts, is stronger in P+/Nwell junction with respect to Pwell/Niso one. The high electric field influence induces to assert that in both layouts, especially in P+/Nwell layout, as supposed in Section 3.3, there is a significant contribution in DCR increase due to tunneling mechanism.

RTS amplitude has been also investigated as a function of temperature. The investigation of RTS behaviour at different temperatures allowed to extract the activation energy for RTS amplitude ($E_{a\ amp}$).

Fig. 4.21 shows the mean RTS amplitude of PN and PWNISO pixel as a function of temperature. The extracted activation energies for RTS amplitude are $0.29 \pm 0.02\ eV$ in PN pixel and $0.40 \pm 0.01\ eV$ in PWNISO pixel. These values give a clear evidence that the centers responsible for RTS are located far from mid bandgap value.

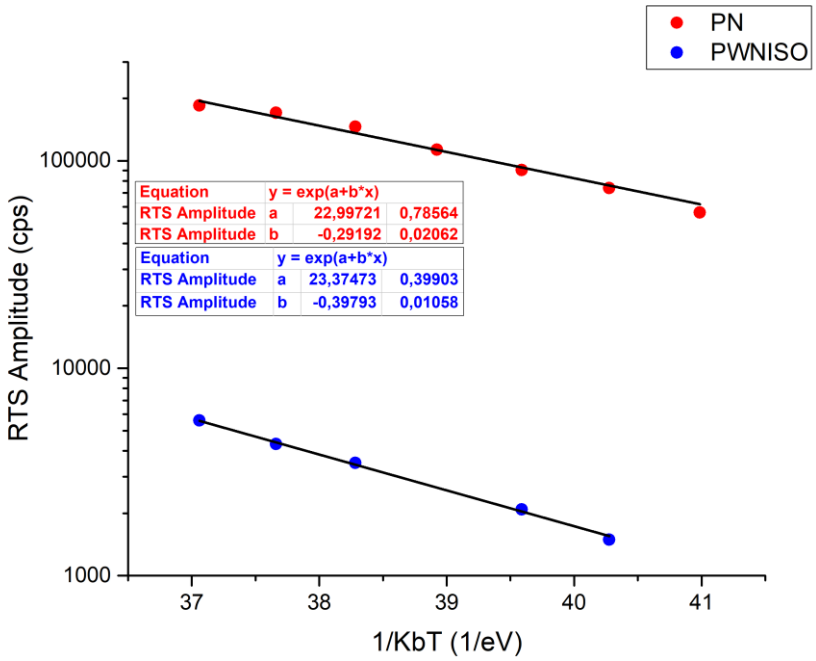


Figure 4-21. RTS amplitude as a function of temperature for PN and PWNISO pixel

Indeed, in both pixels the activation energy is lower than the mid bandgap value. This confirms that the electric field enhancement, such as Poole-Frenkel effect, occurs, resulting in the reduction of the potential energy barrier.

The mean RTS amplitudes as a function of temperature have been analysed in 4 pixels and the extracted activation energies are reported in Table 4.6.

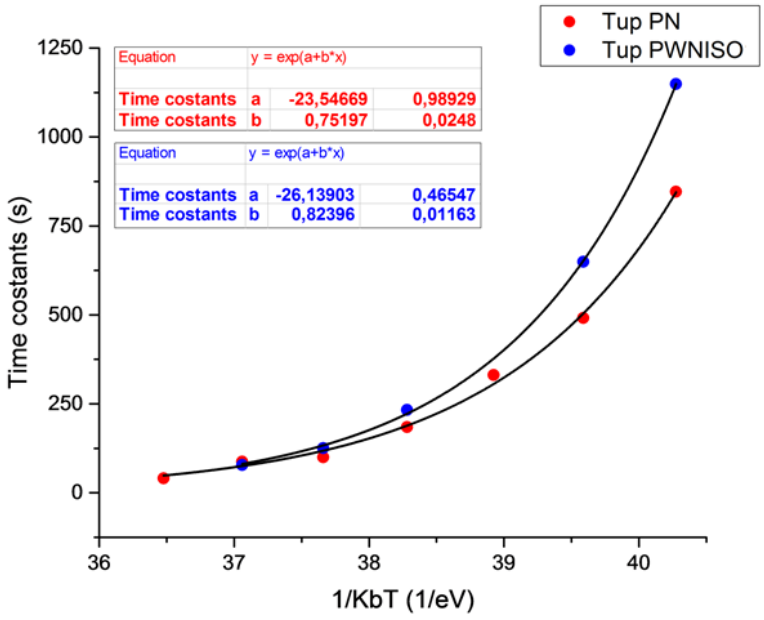
N. Pixel	$E_{a\ amp}$ PN (eV)	$E_{a\ amp}$ PWNISO (eV)
1	0.29 ± 0.02	0.40 ± 0.01
2	0.52 ± 0.01	0.27 ± 0.01
3	0.57 ± 0.01	0.53 ± 0.05
4	0.36 ± 0.05	0.35 ± 0.03
$E_{a\ amp\ mean}$	0.44 ± 0.02	0.39 ± 0.02

Table 4-6. Activation Energy for RTS amplitude in P+/Nwell and Pwell/Niso junction

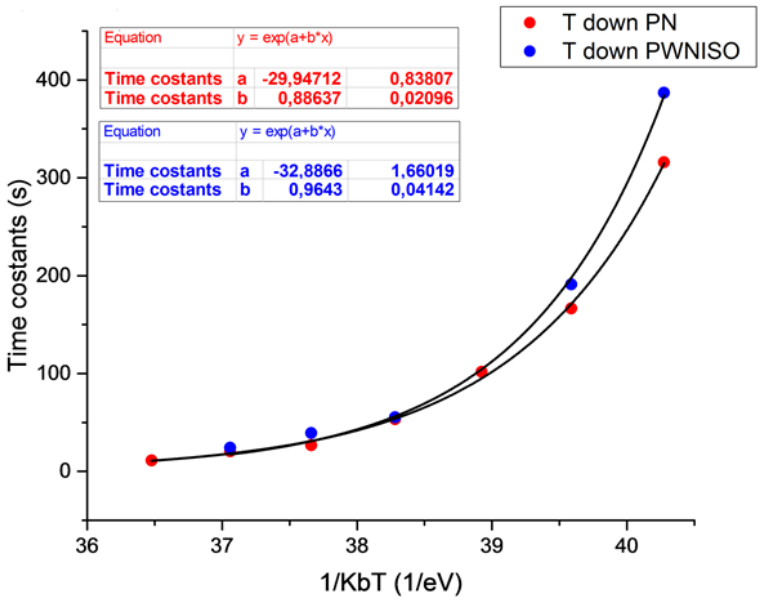
4.6 RTS Time Constants

A typical bi-level RTS, as introduced in Section 2.6.1, is characterized by the times spent in the high and in the low RTS level. By the investigation of RTS behaviour at different temperatures, the activation energies for τ_{up} and τ_{down} ($E_{a\,time}$) have been extracted. In order to obtain a reasonable evaluation of times, at each temperature, measurements of several hours have been carried out to define accurately the mean time constants.

Fig. 4.22a, b report the mean time spent respectively in the high and low RTS level in PN and PWNISO pixel. The extracted activation energies for τ_{up} are 0.75 ± 0.02 in PN pixel and 0.82 ± 0.01 in PWNISO pixel, while for τ_{down} 0.87 ± 0.02 in PN pixel and 0.96 ± 0.04 in PWNISO pixel [90].



a)



b)

Figure 4-22. Time constant in the high level τ_{up} (a) and in the low level τ_{down} (b) as a function of temperature in PN and in PWNISO layout [90]

Four bi-levels RTS pixels for each layout have been analysed in time constants. The activation energies for τ_{up} and τ_{down} have been extracted and the results are reported in Table 4.7 and 4.8.

N. Pixel	$E_{a\,\tau up}$ PN (eV)	$E_{a\,\tau up}$ PWNISO (eV)
1	0.75 ± 0.02	0.82 ± 0.01
2	0.70 ± 0.02	0.82 ± 0.08
3	0.88 ± 0.03	0.78 ± 0.03
4	0.85 ± 0.02	1.03 ± 0.01
$E_{a\,\tau up\,mean}$	$\mathbf{0.80 \pm 0.02}$	$\mathbf{0.86 \pm 0.03}$

Table 4-7. Activation energies for τ_{up} in PN and PWNISO layout

N. Pixel	$E_{a\ \tau down}$ PN (eV)	$E_{a\ \tau down}$ PWNISO (eV)
1	0.89 ± 0.02	0.96 ± 0.04
2	0.62 ± 0.02	1.27 ± 0.10
3	0.85 ± 0.05	0.86 ± 0.01
4	0.89 ± 0.05	1.06 ± 0.07
$E_{a\ \tau down\ mean}$	$\mathbf{0.81 \pm 0.04}$	$\mathbf{1.04 \pm 0.06}$

Table 4-8. Activation energies for τ_{down} in PN and PWNISO layout

The values of activation energy for time constants are on average in the range $0.8 - 1.0\ eV$. Since the activation energy for time constants is related to the barrier height in potential energy to go from one configuration to another [87], the analysed bi-level RTS could be explained with bi-stable defect requiring energy between $0.8 - 1.0\ eV$ for structural re-configuration. Among the possible explanation of the causes of RTS origin explained in Section 2.6.5, there is the reorientation of the vacancy defects relative to the phosphorus atoms, eventually presents in the junction as dopant. The kinetics of P-V dipole moment with respect to electric field vector predicts a time-constant of 0.93, as calculated by Watkins and Corbett (Section 2.6.5) [66]. Therefore, the origin of RTS in SPAD devices could be motivated by the presence of P-V complex defects, as also reported in [54, 61] for proton irradiated charged coupled devices.

4.7 Annealing

The annealing process is an important tool in identifying the defect responsible for RTS, since each defect anneals at different temperature. The annealing temperature of different defects in silicon has been evaluated by [70]. Both the defects leading to DCR and to RTS can be investigated by annealing.

The possible correlation between RTS and P-V center reorientation, suggested by the agreement between time constants activation energy and the kinetics of

reorientation of P-V center, has been further investigated by means of annealing process. Indeed, if P-V center were the main defect involved in RTS, a significant decrease of RTS should be observed at the annealing temperature of P-V center.
An isochronal annealing has been performed on the devices under test up to $250°C$ for temperature step of $50°C$. For each step DCR and RTS occurrence has been measured.

4.7.1 DCR and RTS annealing

The isochronal annealing consists in annealing steps with increasing temperature maintained constant for a time interval. The annealing steps have been performed with increasing steps of $50°C$ up to $250°C$ in an oven. At the end of each step, the device has been taken out the oven, and measurements have been performed at room temperature. For each annealing step, the measurements of DCR and RTS occurrence have been performed. The average DCR of all pixels and RTS pixels occurrence have been evaluated for each annealing step in PN and PWNISO layout.
The Fig. 4.23 shows DCR distribution normalized at the average DCR at $20°C$ before the annealing process. The unannealed factor represents the fraction of DCR after each annealing step. The average DCR decreases as the annealing temperature increases, but a strong decrease of DCR appears in the range between $100°C$ and $200°C$. After the annealing, the overall DCR reaches roughly its original pre-irradiation value.
Similarly, in Fig. 4.24, the number of RTS pixels normalized at the number of RTS pixels before annealing is reported for each annealing step. As for DCR annealing, the unannealed factor for RTS is the fraction of RTS pixels remaining after each annealing step. The number of RTS pixels decreases by increasing the temperature. The annealing behaviour is very similar for both PN and PWNISO layouts.

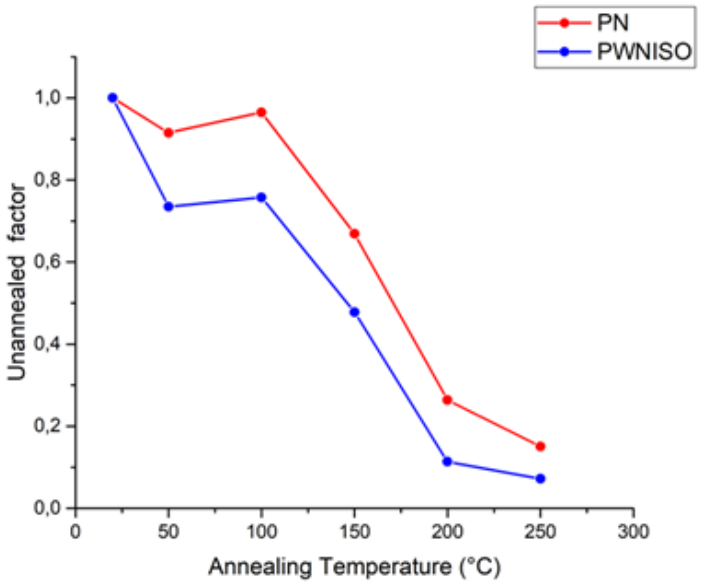


Figure 4-23. Evolution of DCR annealing at different temperatures for PN and PWNISO layout [91]

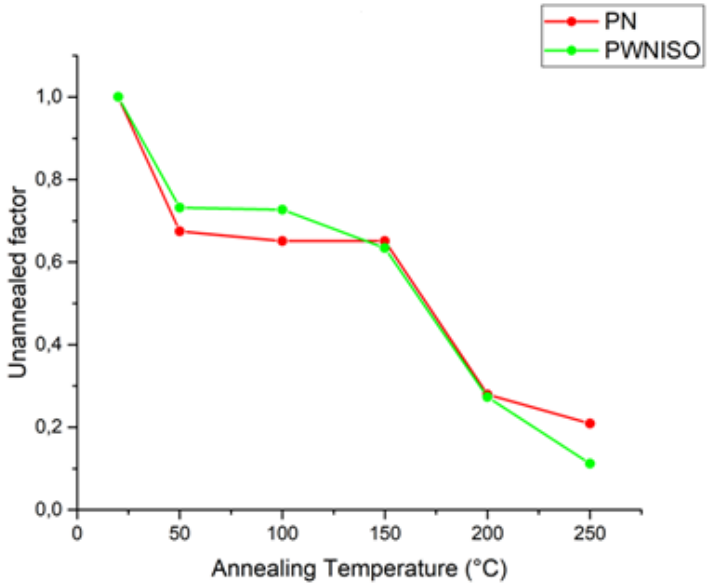


Figure 4-24. Evolution of RTS pixels annealing at different temperatures for PN and PWNISO layout [91]

Focusing on the evolution of RTS-levels during the annealing procedure, Table 4.9 and Fig. 4.25 report the number of levels of RTS pixel for each annealing step in PWNISO layout. If the distribution of 5 levels pixels results decreasing by

increasing annealing temperature, 2, 3 and 4 levels pixels show non - monotonic decreasing behaviour. This is due to 2, 3, 4 RTS levels in which the annealed fractions are compensated by the higher RTS levels which pass from an intermediate number of levels before to completely anneal. For example, it can occur that between 50 $°C$ and 100$°C$, the great contribution to 2 levels pixels comes from 3, 4 or 5 levels pixels that after 50 $°C$ convert in 2 levels pixels before to become a no-RTS pixel at the next annealing temperature.

$T_{annealing}$ [$°C$]	2 levels	3 levels	4 levels	5 levels	RTS Total
20	34	15	8	129	186
50	25	14	6	105	150
100	35	7	8	99	149
150	31	10	8	81	130
200	21	8	2	25	56
250	14	3	1	5	23

Table 4-9. Levels classification of RTS PWNISO pixels at different annealing temperatures

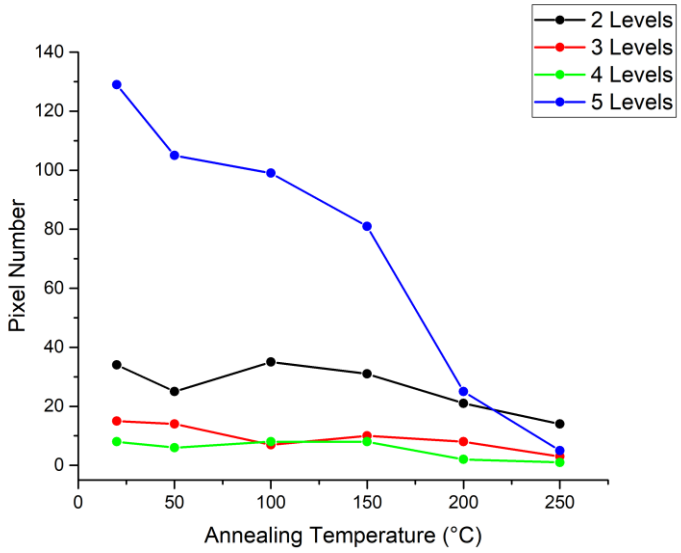


Figure 4-25. Distribution of RTS PWNISO pixels at different annealing temperatures

Moreover, looking Fig. 4.23 and 4.24, RTS annealing distribution seems similar to DCR annealing distribution, showing a significant decrease of the number of RTS

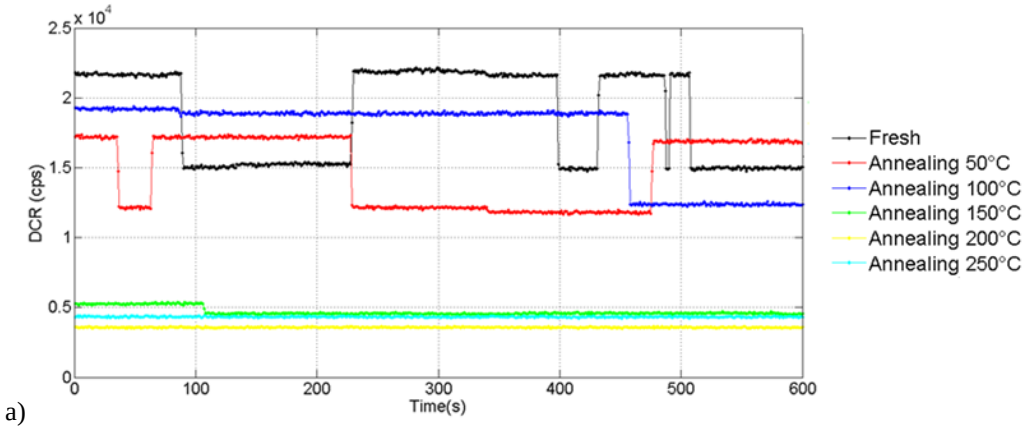
pixel in the range between $100°C$ and $200°C$. This could mean that the defects involved both in DCR increase and in RTS occurrence can have the same nature, as observed in [61]. Taking into consideration the annealing temperatures of each defect reported in Fig. 2.17, the annealing temperature of P-V centers ($\sim 140°C$) results compatible to the temperature range in which DCR, as well as RTS occurrence, decrease significantly.

This strengthens the hypothesis that P-V could be one of the defects involved in RTS, as reported in [54, 61], since P-V center is the first defect that anneals over the room temperature (Fig. 2.17). The next defect that anneals at $180\ °C$ is As-V center, while the divacancy anneals at $290\ °C$ [61].

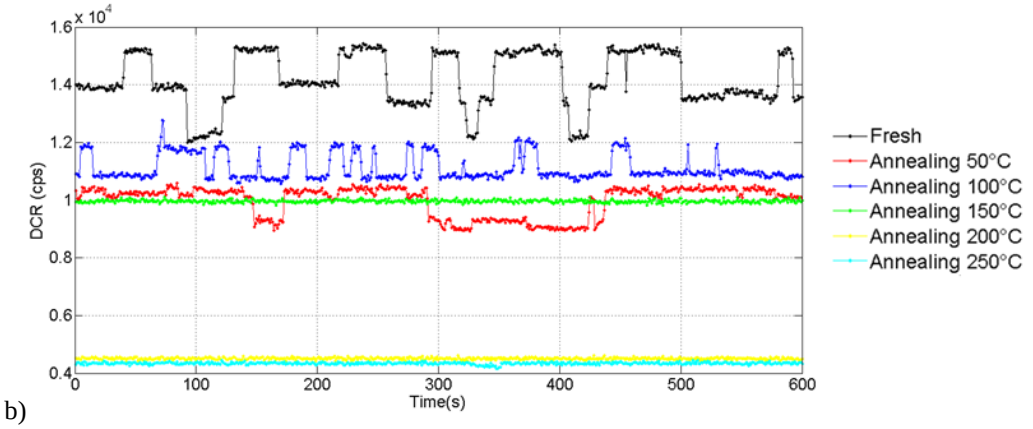
However, the recent literature [92] assumed that the clusters of defects could be also involved in RTS phenomenon. This theory is supported to the smooth annealing behaviour observed in the experimental analysis, since, as explained in Section 2.6.6, first the defects around cluster are annealed, and after the defects in the middle, resulting in the spread of the annealing temperature [59], as observed in Fig. 4.23 and 4.24. The single point defect annealing, as P-V center, should show a sharp annealing behaviour at $140\ °C$.

Regarding RTS investigated in this thesis, the evolution of several pixels at each annealing step has been investigated. Most of pixels shows a behaviour similar to the one reported in Fig. 4.26a, b in which after $150°C$ RTS is completely annealed. However, in some pixels, RTS annealing distribution similar to Fig. 4.27 has been observed: some pixels still shows RTS behaviour at $250°C$. Indeed, in Fig. 4.23 and 4.24 it is evident that at $150\ °C$, the unannealed factor decreases but without reaching zero. This means that some defects with higher annealing temperature occurs in the devices. Therefore, different types of defects are involved in DCR increase and in RTS occurrence and more complex defects configuration has to be taken into account in addition to point defect P-V. By investigating among defects with higher annealing temperature in Fig. 2.17, it could be possible that clusters of divacancies could contribute to DCR increase and RTS mechanism in silicon,

according to [59]. This is another hypothesis to take into consideration in addition to P-V center. However, more investigation is necessary to fully explain this phenomenon.



a)



b)

Figure 4-26. Evolution of a bi-level (a) and multilevel RTS during annealing. No RTS behaviour occurs at $150\ °C$

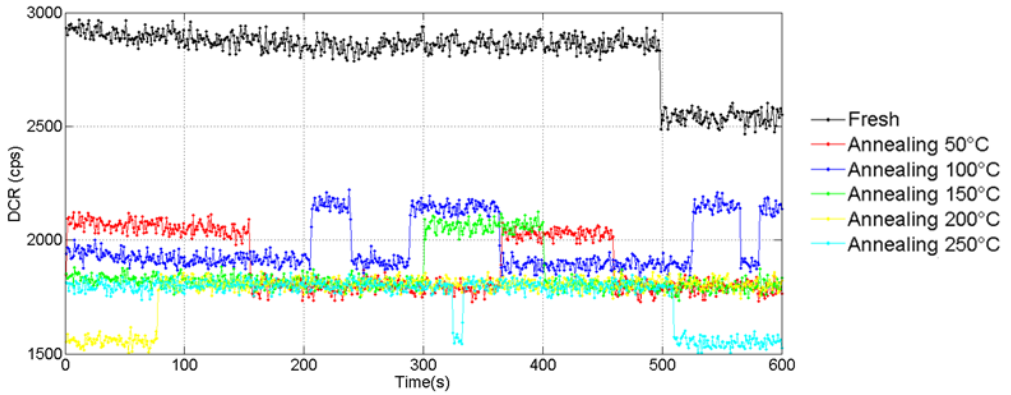


Figure 4-27. Evolution of a bi-level RTS during annealing. RTS behaviour persists at $250\ °C$

Conclusion

This thesis investigates RTS phenomenon in proton irradiation environment on two different SPAD layouts implemented in $150nm$ CMOS technology. The devices feature two different junction types: P+/Nwell and Pwell/Niso. These layouts have been analysed in Dark Count Rate and in Random Telegraph Signal before and after irradiation with proton beam. The measurements of main RTS properties allowed to propose a hypothesis for the defect types that cause RTS. The performed experiment proved that RTS occurrence represents one of major limitation for the application of SPAD devices in a radiation environments with more than $5 \cdot 10^{10}\ protons/cm^2$. Indeed, more than 50% of SPADs shows RTS behaviour.

The identification of defects responsible for RTS and the understanding of its evolution in different conditions of temperature and bias voltage, are useful to understand RTS origin and to limit this effect on devices operating in radiation environment.

The characterization of DCR in two layouts exhibited DCR level twice higher in P+/Nwell than in Pwell/Niso junction both in circular than in square configuration. Moreover, in order to investigate the DCR distribution at different temperatures, measurements in climatic chamber have been performed. The study of DCR in temperature allowed to extract the values of activation energy from the slope of Arrhenius plots of two different junctions. The distribution of activation energy value showed a decreasing distribution by increasing DCR, resulting in the mean value of $0.35\ eV$ for P+/Nwell and $0.5\ eV$ for Pwell/Niso junction. Since the activation energy distribution decreases by increasing DCR and both activation energy values are lower than the mid bandgap value, electric field enhancement factors are clearly involved in the process.

The devices have been irradiated with proton beam at Tandem accelerator and Cyclotron accelerator at LNS INFN (Catania). Measurements performed after irradiation showed an increase of DCR followed by a natural room temperature

annealing with a partial DCR recovery. The overall result is an increase of DCR of about one order of magnitude. Moreover, most pixels in both junctions exhibited RTS mechanism, but P+/Nwell junction showed a higher RTS occurrence probability with respect to Pwell/Niso junction. The high doping profile of P+/Nwell junction contributes to enhance the electric field with respect to Pwell/Niso. This could suggest a correlation between the high electric field, the high DCR and the increased RTS occurrence. In order to better investigate the influence of the electric field on RTS, a classical bi-level RTS has been studied as a function of overvoltage in high and low level in both junctions. The layouts show an increase of DCR by increasing overvoltage, especially at high overvoltage. In particular, P+/Nwell shows a higher increase than Pwell/Niso. This strong dependence of RTS by overvoltage is a clear evidence that an important contribution to DCR is given by tunneling mechanism.

RTS time constants have been studied as a function of temperature. The extracted activation energies for time constants showed value around $0.8 - 1.0\ eV$. These values are in good agreement with the kinetics of reorientation of P-V center, calculated as $0.93\ eV$ by Watkins and Corbett. Therefore, RTS measurements reported in this work could support the hypothesis that attributes RTS behaviour to the reorientation of the phosphor-vacancy (P-V) center.

Moreover, annealing process has been performed on DCR distribution and on the number of RTS pixels. The annealing is an important tool to understand the defects responsible for RTS, since each defect anneals at different temperature. Both DCR and the number of RTS pixels exhibits a significant decrease around $150°C$. Being the annealing temperature of P-V center at $150°C$, the hypothesis of P-V center reorientation at the basis of RTS mechanism seems to be strengthened by annealing process. However, the unannealed factor both for DCR and RTS does not decrease sharply at $150\ °C$, and not reach zero at $250°C$. This means that other defects are involved in RTS mechanism. The cluster of intrinsic defects could be taken in consideration since the spread of annealing temperature observed in the analysis

seems to be typical to the annealing of cluster of defects. This is only the first step in understanding of RTS behaviour in CMOS SPADs devices. Further investigations are certainly necessary to enlarge the knowledge on RTS and to recognize each defects or cluster of defects involved in this mechanism.

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A chi…

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