UNIVERSITÀ DELLA CALABRIA

Dipartimento di Elettronica,
Informatica e Sistemistica

Dottorato di Ricerca in
Ingegneria dei Sistemi e Informatica
Ciclo XXIV

Tesi di Dottorato

Modulation techniques and synchronization methods for DC/AC conversion systems

Andrea Ferrise

Coordinatore
Prof. Luigi Palopoli

Supervisore
Prof. Alfredo Eisinberg

DEIS

DEIS- DIPARTIMENTO DI ELETTRONICA, INFORMATICA E SISTEMISTICA
Novembre

Settore Scientifico Disciplinare: ING-INF/04

To my parents.
To the people that have always played an important role in my life.
"The end of wisdom is to dream high enough to lose the dream in the seeking of it" (William Faulkner)

Contents

1

Introduction

Current trends in energy supply and use are patently unsustainable regarding the whole set of current economical, environmental and social aspects in energy demand. Without decisive actions, as reported by the International Energy Agency (**IEA**) [70], energy-related emissions of CO_2 will more than double by 2050 and increased oil demand will heighten concerns over the security of supplies. Energy efficiency, many types of renewable energy, carbon capture-storage (CCS) and nuclear power require widespread deployment to achieve the prefigured green-energy targets. The development of a correct energy policy is a nodal point if we want to make possible that the current investment decisions do not saddle us with sub-optimal technologies in the long term. There is a growing awareness of the urgent need of turn political statements and analytical work into concrete action. To spark this movement, at the request of the *G*8, the IEA is developing a series of road-maps for some of the most important technologies. As reported by the United States Department of Energy,

"Energy supply and demand plays an increasingly vital role in our national security and the economic output of our nation."

Annually 2584 kilowatt hours of electricity were produced for every person living on earth in 2002. Moreover, it is important to note that the distribution of production is not uniform - Benin and Togo only produce 10 and 11 kilowatt hours per person per year, respectively. Norway and Iceland produce almost 3000 times more per person per year. To better clarify the present situation, the web-site **Worldmapper** (website www.worldmapper.org) makes available very interesting maps where the territory size is proportional to the percentage of world electricity production that occurs there. In Fig. 1.1 is reported the World as far as energy demand and production is concerned.

The current world situation is increasing the need of the development of advanced clean energy technologies in order to address the global challenges of energy security, climate change and sustainable development. This challenge was acknowledged by the Ministers from G8 countries, China, India and South

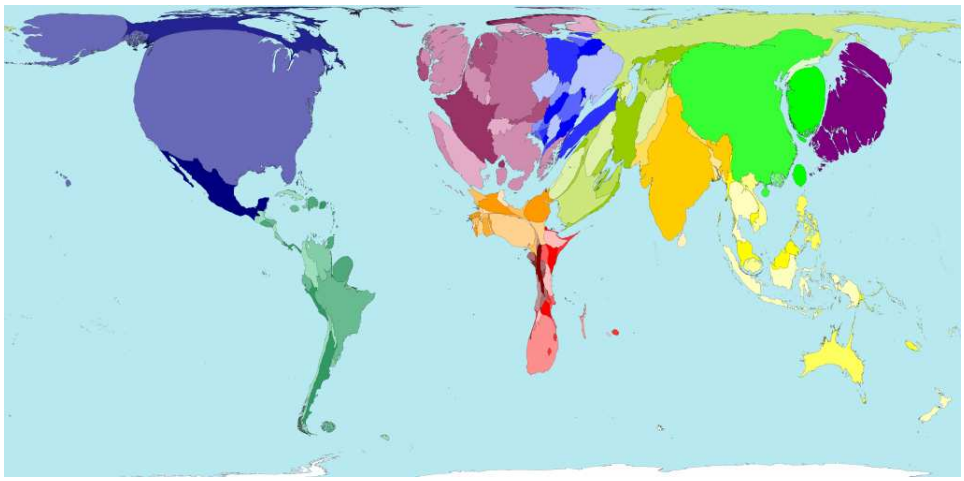

Fig. 1.1. World Energy demand - WorldMapper

Korea, in their meeting in June 2008 in Aomori (Japan) where they declared the wish to have IEA prepare road-maps to advance innovative energy technology.
"We will establish an international initiative with the support of the IEA to develop road-maps for innovative technologies and co-operate upon existing and new partnerships, including CSS and advanced energy technologies. Reaffirming our Heiligendamm commitment to urgently develop, deploy and foster clean energy technologies, we recognise and encourage a wide range of policy instruments such as transparent regulatory frameworks, economic and fiscal incentives, and public/private partnerships to foster private sector investments in new technologies...."
The IEA has defined its global technology roadmap accordingly:
*"... a dynamic set of technical, policy, legal, financial, market and organisational requirements identified by the stakeholders involved in it development. The effort shall lead to improved and enhanced sharing and collaboration of all related technology-specific RDD&D (**R**esearch, **D**evelopment, **D**emonstration and **D**eployment) information among participants. The goal is to accelerate the overall RDD&D process in order to deliver an earlier uptake of the specific technology into the marketplace."*

It is worth to underline that, at the current date, there exist major barriers, opportunities, and policy measures for policy makers and industry and financial partners to accelerate RDD&D efforts for specific clean technologies on both a national and international level. The guidelines for the research in this area suggest the need of improvements in terms of efficiency, robustness and cheapness of the modern power conversion systems. A first target of this thesis is the design of a more efficient conversion system that is highly competitive with respect to the standard technologies. Indeed, it is known

that, in conventional power conversion from a continuous power source to an alternate load, the input to inverters is a stiff dc voltage supply and the power switches operate in a switch mode. Therefore, the power devices are subjected to high switching stresses and switching power losses that increase linearly with the switching frequency of the implemented inversion technology. High switching power losses not only restrict switching frequency, but affects also the efficiency by dissipating a large amount of the produced energy inside the inverter. An increased volume and weight of the system are consequences of such losses too. In addition to these limitations, the system suffers from other shortcoming such as electromagnetic interferences and acoustic noise (see [67]). A different inverter output signal is proposed that consists in a $T-$periodic, three-level signal with a single centred adjustable zero-level. In Chapter 3, the properties of this particular signal are investigated. Interestingly, the particular structure of the proposed signal permits to obtain an analytical expression for the relative total harmonic distortion (**THD**) in terms of the zero-level duration. The obtained THD expression can be so tuned to assume values that are less than 1 unlike the standard pulse-width modulation (**PWM**) techniques presented in Chapter 2. An immediate result is that, by presenting only three-level, the inverter switches have to switch at a frequency equal to $3f_{ref}$ if f_{ref} is the desired output frequency and so the corresponding switching stress, which the switches are subject to, is much smaller than standard devices that require very greater switching frequencies. An explicit tuning for a LC filter and a control algorithm are also presented in Chapter 3: the tuning permits to make the system insensitive with respect to filter variations and the control algorithm maintains the output sinusoidal amplitude at a desired level. The second problem, related to power conversion system and discussed in Chapter 4, is the synchronization of the generated signals. The synchronization between the grid voltage and the voltage or current synthesized by the converter is a central task: phase, amplitude and frequency of the utility voltage are critical information for the operation of the grid-connected inverter systems. In almost all power electronic equipment connected to the grid, a phase-locked loop (**PLL**) is used to obtain an accurate synchronisation to the grid. More in general, any implemented synchronisation algorithm must cope with the existing electrical environment (see [25]), e.g. with harmonics, voltage sags and commutation notches. Another aspect that must be taken into account is represented by grid frequency variations [80, 89]. In robust grids, the frequency variations are usually small, but larger frequency variations may occur in small interconnected grids. Furthermore, the synchronisation must handle measurement noise and, in general, an accurate zero voltage crossing detection is essential for the control of grid-commutated converters, otherwise the converter system can suffer from poor performance or even instability [32]. The zero voltage crossing therefore must be accurately detected each half period of the grid even if it is well known that zero-cross detectors performance is very low in the presence of electromagnetic disturbances occurring in electrical network in various conditions and affecting electrical

equipments designed to operate in non polluted environment [68, 90]. A more demanding application is the grid connection of a forced-commutated voltage source converter when vector current control is used. The synchronization must be update not just at zero voltage crossings but continuously under the whole period. In this case, a flux-based transformation angle detector is used to obtain the rotating dq-coordinate system [86]. Two classical solutions were proposed in the late $60's$ as synchronisator devices: Phase-Locked Oscillator (**PLO**) system and analogue PLL. The PLO system was proposed by J.D. Ainsworth to deal with the novel, at that time, harmonic instability problem in connected grids. The key idea was to place a Voltage Controlled Oscillator (**VCO**) inside the controller of the thyristor based rectifier of a HVDC by providing good noise rejection and frequency adaptation. The main drawback is the high complexity in the tuning of this kind of controller. The VCO scheme was therefore applied in analogue phase locked loops. The main novelty of the PLL proposal is the fact that the VCO is not a part of the main control algorithm but it is employed within a measurement circuit (estimation). The analogue PLLs provide robustness in the presence of grid frequency deviations and high frequency noise. However they perform bad in the presence of harmonics and unbalance [32]. Today, by using a software solution to the PLL, a flexible and cost effective solution is obtained: digital filters and controller have increased performances and made new methods feasible. Moreover, if the input signal is noisy, a predictive digital filter can be used to find the zero voltage crossing for the PLL. The calculation time is critical for a real time control system, which results in a demand for fast algorithms. The synchronization problem can be posed as a stochastic filter too, such as Kalman and Recursive Least Square algorithms where the best feature of stochastic filters is their potential very fast transient even under distorted conditions. In [83] a smart and simple stochastic filter approach is provided, based on a recursive least square algorithm, named Weighted Least Squares Estimation (**WLSE**), both for single-phase and three-phase systems. The main advantage of the WLSE is that its speed versus filtering is mainly set by the only forgetting factor.

Following the international standard criteria, any other synchronization algorithm should have:

- high stability margin;
- a fast transient response;
- zero steady-state average phase error and
- low phase jittering

in order to be considered a high performance system. Algorithms based on FIR and stochastic filtering provide a better filtering/transient trade-off than PLLs. However, this assertion should be reconsidered in the presence of grid-frequency deviations. Different standards such as EN 50160, IEC61000 and European Grid Codes consider frequency deviations higher than $\pm 2Hz$ inside a normal operation range (isolated systems). Therefore, the performances of

advanced filtering techniques should be revised. Techniques that are proposed to improve the frequency adaptation can be classified as

- On-line update of filter implementation: using the frequency estimation the filter coefficients (generalized integrators, notch) are updated in real time.
- Hybrid systems: using a PLL to provide the frequency estimation, the performance of stochastic filters can be improved.
- Frequency loops: similar to the previous technique, by means of a frequency loop, the main algorithm is adapted to the input frequency.
- Variable sampling rate systems: in a general manner, an update of the discrete device switching frequency to be an integer multiple of the input frequency.
- Phase-offset correction techniques: the steady-state phase-error can be estimation from the outputs.

A qualitative comparative summarizes the performance of the difference techniques is reported in Fig. 1.2 (see [32]). The digital breakthrough resulted in a higher performance.

Technique	Freq. Adapt.	Har/Unb Filtering	Trans. Response	Amp. InDep.	Comple-xity
Zero-cross Det	−	−	+	+	+++
PLO	+	+	−	−	− − −
Low-Gain PLL	+	+	−	−	+
High BW PLL	+	− −	+++	−	++
SRF-MAF	−	++	+	+	+
WLSE (Big $\mathbf{H}$, small λ)	−	++	++	+	−
WLSE (Small $\mathbf{H}$)	−	− −(small λ) +(big λ)	++(small λ) −(big λ)	+	+

Fig. 1.2. Comparative analysis

In this thesis a frequency-locked system is presented that is based on a second-order generalized integrator (**SOGI**). SOGI have been widely investigated in the literature. Adaptive and non-adaptive schemes are reported in Chapter 5 to track an input sinusoidal signal in a satisfactory manner. It has to be remarked that SOGI schemes can be easily adapted to a large variety of practical scenarios. Thanks to its flexibility, SOGI approach permits to deal with such a problem showing performances better than PLL and adaptive filters ones. The behaviour of the SOGI as second-order filter leads to fast transient response and a very good noise rejection as shown in numerical simulation. In Chapter 5 numerical simulations are shown to confirm the obtained results.

2

DC-AC Power Conversion

2.1 Introduction

DC-AC power conversion problem consists in the manipulation of a dc power source in order to obtain an alternative power signal at a desired output voltage or current amplitude and frequency through a static semiconductor device that is defined inverter (see [3, 26]). From 1980s, semiconductor manufacture development brought power devices, such as gate turn-off thryristor, Triac, bipolar transistor, insulated gate bipolar transistor and metal-oxide semiconductor field effected transistor (GTO, Triac, BT, IGBT, MOSFET, respectively) and so on, in higher switching frequency. In those equipments, devices as thyristors, GTOs and Triacs could be in low-frequency switching operation. High-frequency/high-power devices such as power BTs and IGBTs were also produced. Nowadays, most DC/AC inverters are DC/AC PWM inverters in different typologies. They are generally used in following applications:

- variable voltage/frequency AC supplies in adjustable speed drives (ASDs), such as induction motor drives, synchronous machine drives and so on;
- constant regulated voltage AC power supplies, such as uninterruptible power supplies (UPSs);
- static var compensations;
- flexible AC transmission systems (FACTSs);
- voltage compensations.

Adjustable speed induction motor drive systems are widely applied in industrial applications. These systems request the DC-AC power supply with variable frequency usually from 0 to 400 Hz, in fractional horsepower (HP) to hundreds of HP. The power devices used for ASD were thyristors, Triacs and GTOS in the 1970s and early 1980s. Power IGBT greatly changed the manufacturing of DC/AC inverters. Nowadays, two main families of power inverter can be identified: voltage- and current-fed respectively. The terms voltage-fed and current-fed are used in connection with the output from inverter circuits, that can be single-phase, three-phase or multi-phase. A *voltage-source inverter*

(VSI) is one in which the dc input voltage is essentially constant and independent of the load current drawn. The inverter specifies the load voltage while the drawn current shape is dictated by the load. A *current-source inverter (CSI)* is one in which the load current is predetermined and the load impedance determines the output voltage. The supply current cannot change quickly but it is controlled by series dc supply inductance which prevents sudden changes. The load current magnitude is controlled by varying the input dc voltage to the large inductance, hence inverter response to load changes is slow. Voltage control may be required to maintain a fixed output voltage when the dc input voltage regulation is poor or to control power to a load. Due to the particular generation process, harmonics which may lead to reduced load efficiency and they may affect the inverter output signals. Load harmonic reduction can be achieved by either filtering, selected harmonics reduction, chopping or pulse-width modulation as will be investigated below and a large range of quality indexes exist to evaluate the output signal in terms of their harmonic content. Since middle 1990s, the power quality problem has assumed a growing interest (as widely remarked in [77, 34, 91]) . There are different reasons for this enormous increase in the interest in power quality:

- Electronic systems are more sensitive of voltage quality disturbances. These aspects are translated into a much higher costs than before associated with even a very short-duration disturbance.
- Equipment produces more current disturbances than it used to do. Both low- and high-power equipment is more powered by simple power electronic converters which produce a broad spectrum of distortion.
- The liberalization of the electricity industry has let to an increased need for quality indicators.
- Embedded generation and renewable sources of energy create new power quality problems, such as voltage variations, flicker, and waveform distortion. Most interfaces with renewable sources of energy are sensitive to voltage disturbances, especially voltage dips.
- Energy-efficient equipment is an important source of power quality disturbances. Adjustable-speed drives and energy-saving lamps are both important sources of waveform distortion and are also sensitive to certain types of power quality disturbances.

Generally, a difference between voltage and current distortion must be made. Voltage quality is related in fact to the effects of the network with respect to customer or load; current quality takes into account how the customer or the load affects the network. In the waveform distortion framework, it can be noted that distorted voltages affect the customer equipment while distorted currents affect the network components. In the case of voltage distortion the following problems are reported to arise

- inadvertent trip of circuit breaker or fuse;
- transformer overheating;

- capacitor problems;
- malfunctioning of electronic equipment;
- overheating of neutral conductors.

It has been referred with the term *waveform distortion* to all the deviations of the voltage and current signals with respect to the ideal sine wave. With respect to this definition, a number of different forms of waveform distortion can be distinguished: harmonic, interharmonic, and nonperiodic distortion. Harmonic distortion dominates in most the cases. When a signal is T-periodic, an analysis in terms of its Fourier series can be conducted. For a voltage waveform, it can be written

$$v(t) = V_0 + \sum_{j=1}^{H} V_j \sin(j\omega t) \tag{2.1}$$

where H is infinite in the case of continuous signal while it is determined by the sample frequency in the case of discrete signals. The same remains true for the current waveform. Within harmonic distortion, a further distinction can be made into *dc components*, *even-harmonic distortion*, and *odd-harmonic distortion*, that is the dominating case in the generality of applications. DC components need of different measurement or estimation techniques. It is important to remark that often the voltage or current waveform contains components that are not a multiple integer of the power system frequency and the presence of inter-harmonics can be interpreted in the time domain as the signal being periodic but with a period of more than one cycle. A further distinction is so provided between rational and irrational inter-harmonics. The former lead to periodic signals whereas the latter signals are aperiodic. Finally, some signals contain no periodicity at all. Examples are the voltage during ferro-resonance and the current taken by an arc furnace. In such scenarios, noise or chaotic behaviour can occur. In terms of the spectrum of the signal, harmonic distortion corresponds to frequency components at integer multiples of the power system frequency, inter-harmonic distortion to non-integer multiples, and noise to a continuous spectrum in between the harmonic and inter-harmonic spectral lines. Two particular indices assume a key role in the treatment of power quality for conversion systems: the total harmonic distortion and the **crest factor**. Eq. (2.1) shows as a periodic signal can be decomposed into a number of harmonics and so the signal can be totally characterized by the magnitude and phase of these harmonics. In power system applications, the fundamental component will normally dominate. The total harmonic distortion indicates the deviation of voltages or currents from ideal and desired sine waves and it is expressed as

$$THD = \frac{\sqrt{\sum_{j=2}^{H} V_j^2}}{V_1}. \tag{2.2}$$

The crest factor is a time-domain property indicating the distortion of the actual amplitude. It is defined as the ratio between the amplitude of a signal

and its rms value:

$$C_r = \frac{V_{max}}{V_{rms}} \tag{2.3}$$

with

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)d(t)}. \tag{2.4}$$

For a perfect sine wave the crest factor is equal to $\sqrt{2}$ so that is makes sense to introduce a *relative crest factor* which is unity for a perfect sine wave:

$$c_r = \frac{1}{\sqrt{2}}\frac{V_{max}}{V_{rms}}. \tag{2.5}$$

This index takes into account how much a signal deviates from a dc signal, whereas the relative crest factor indicates how much a signal deviates from a sine wave. In the following sections the generality of the inverter topologies will be investigated and in particular their frequency behaviour will be highlighted. The main standard results regarding the state of art of the power switching conversion systems are below reported. For an exhaustive overview, the considered bibliography (see for example [41, 92, 60, 63, 72, 73, 7, 65]) is highly recommended.

2.2 VSI bridge topologies

2.2.1 Single-phase inverter

The structure of an H-bridge voltage-source inverter (VSI) is reported in Fig. 2.1 that makes use of switches which may be transistors (MOSFET or IGBT), or thyristors (GTO or GCT) at high power. Device conduction patterns are also shown in the same figure. With inductive loads (not purely resistive), stored energy at turn-off is fed through the bridge reactive feedback or freewheel diodes D_1 to D_4.

In Fig. 2.1, the generated waveforms for a square-wave output ($2t_1 = t_2$) are shown. It is an immediate result that the load current i_L grows exponentially through T_1 and T_2 according to the differential law

$$V_s = L\frac{d}{dt}i_L + i_L R. \tag{2.6}$$

Such equation is obtained by turning off T_1 and T_2, turning on T_3 and T_4, and thereby reversing the load voltage polarity. Instantaneous changes of polarity for the load current are not permitted by the inductive topology of the load and load reactive energy flows back into the supply via diodes D_3 and D_4 (which are in parallel with T_3 and T_4 respectively) according to

$$-V_s = L\frac{d}{dt}i_L + i_L R. \tag{2.7}$$

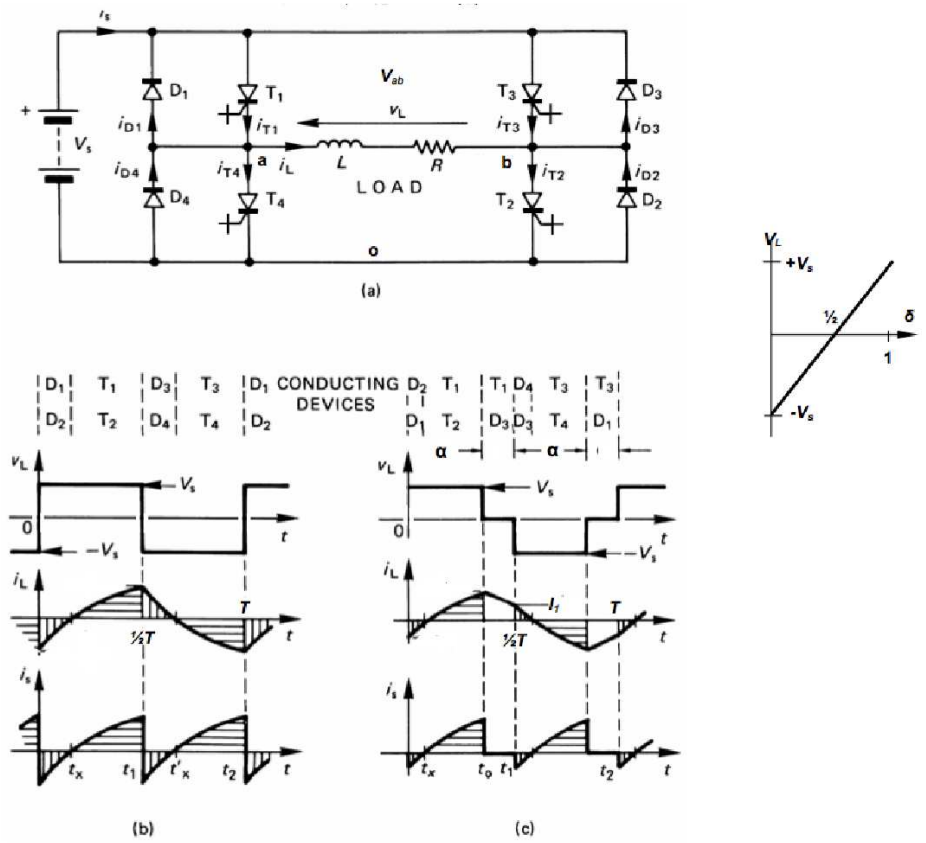

Fig. 2.1. GCT thyristor single-phase inverter: (a) circuit (b) square-wave output (c) quasi-square-wave output

The load current goes exponentially fast to zero. As it can be noticed, the output voltage is a square wave of magnitude $\pm V_s$. For a resistive-inductive load, characterized by resistor R and inductor L, with time constant $\tau = \frac{L}{R}$, during the first cycle, the load current is (with no initial load current)

$$i_L(t) = \frac{V_s}{R}\left(1 - e^{-\frac{t}{\tau}}\right). \tag{2.8}$$

where Eq. (2.6) is taken into account. Under steady-state conditions, Eq. (2.6) yields

$$i_L(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - I_0\right) e^{-\frac{t}{\tau}} \quad 0 \le t \le \frac{T}{2}. \tag{2.9}$$

where I_0 stands for the initial current. During the second half-cycle ($t_1 \le t \le t_2$) when the supply is effectively reversed across the load, Eq. (2.7) yields

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} - I_0\right) e^{-\frac{t}{\tau}} \quad 0 \leq t \leq \frac{T}{2}. \tag{2.10}$$

In steady-state conditions, Eq. (2.9) permits to obtain the initial current I_0 by imposing that at $t = t_1$, $i_L = I_0$. The zero current cross-over point t_x can be found by solving Eq (2.9) for $t = t_x$ when $i_L = 0$ which yields

$$t_x = \tau \log\left(1 + I_0 \frac{R}{V_s}\right). \tag{2.11}$$

There are other signals of interest in the analysed circuit and, in particular, an estimate of thyristor, average diode and mean source currents, namely $\overline{I}_t$, $\overline{I}_d$ and $\overline{I}_s$ respectively, are often needed. Such currents can be obtained via integration of the load current over the appropriated bounds. In particular

$$\overline{I}_t = \frac{1}{t_2}\left[\frac{V_s}{R}(t_1 - t_0) + \tau\left(\frac{V_s}{R} + I_0\right)\left(e^{-\frac{t_1}{\tau}} - e^{-\frac{t_0}{\tau}}\right)\right], \tag{2.12}$$

and

$$\overline{I}_D = \frac{1}{t_2}\left[-\frac{V_s}{R}t_x - \tau\left(\frac{V_s}{R} + I_0\right)\left(e^{-\frac{t_x}{\tau}} - 1\right)\right]. \tag{2.13}$$

The average DC voltage source current is related to the average semiconductor device currents by

$$\overline{I}_s = \frac{1}{t_2}\left[-\frac{V_s}{R}t_1 + \tau\left(\frac{V_s}{R} + I_0\right)\left(e^{-\frac{t_1}{\tau}} - 1\right)\right]. \tag{2.14}$$

In steady-state conditions, the averaged power delivered by the DC supply and absorbed by the resistive load component R is equal to

$$P_L = V_s \overline{I}_s. \tag{2.15}$$

Fourier series expression of the instantaneous output voltage is the following

$$V_L = \frac{4}{\pi} V_s \sum_{n \text{ odd}}^{\infty} \frac{1}{n} \sin n\omega_0 t \tag{2.16}$$

where $\omega_0 = 2\pi f_0$ is the fundamental frequency and for $n = 1$ the magnitude of the fundamental frequency is $\frac{4}{\pi}V_s$. Even load current can be expressed in terms of the Fourier voltage waveform series, leading to

$$i_L(\omega t) = \sum_{n=1,3,5}^{\infty} I_n \sin(n\omega_0 t - \phi_n), \tag{2.17}$$

where $I_n = \frac{4}{n}\frac{V_s}{nZ_n}$ whence $I_{n,rms} = \frac{I_n}{\sqrt{2}}$,

$$Z_n = \sqrt{R^2 + (n\omega_0 L)^2} \tag{2.18}$$

and

$$\phi_n = \tan^{-1} \frac{n\omega_0 L}{R} \tag{2.19}$$

such that $\cos\phi_1 = \frac{R}{Z_1}$. The fundamental output power is

$$P_1 = \frac{V_s^2}{R}\frac{8}{\pi^2}\cos^2\phi_1. \tag{2.20}$$

The load power is given by the sum of each harmonic power component, that is

$$P_L = \sum_{n=1,3,5}^{\infty} I_{n,rms}^2 R. \tag{2.21}$$

Alternately, after integrating Eq. (2.15), with the load current from Eq. (2.17), one can obtain

$$P_L = \frac{V_s^2}{R}\left(1 - \frac{2\tau}{t_1}\frac{1 - e^{-\frac{t_1}{\tau}}}{1 + e^{-\frac{t_1}{\tau}}}\right). \tag{2.22}$$

The rms output voltage from a H-bridge can be varied by producing a quasi-square output voltage ($2t_1 = t_2, t_0 < t_1$) as shown in Fig. 2.1(c). Moreover, according to Fig. 2.1(c), the load current i_L for an applied quasi square-wave voltage is derived in the following manner. For $v_L > 0$, it can be derived that

$$i'_L(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - \tilde{I}\right)e^{-\frac{t}{\tau}} \quad 0 \le t \le t_0. \tag{2.23}$$

where

$$\tilde{I} = -\frac{V_s}{R}\frac{e^{-\frac{t_1 - t_0}{\tau}} - e^{-\frac{t_1}{\tau}}}{1 + e^{-\frac{t_1}{\tau}}}. \tag{2.24}$$

For $v_L = 0$, the following expression is obtained

$$i''_L(t) = \hat{I}e^{-\frac{t}{\tau}} \quad 0 \le t \le t_1 - t_0, \tag{2.25}$$

with

$$\hat{I} = -\frac{V_s}{R}\frac{1 - e^{\frac{t_0}{\tau}}}{1 + e^{-\frac{t_1}{\tau}}}. \tag{2.26}$$

Lastly, for $v_L < 0$

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + I_1\right)e^{-\frac{t}{\tau}} \quad 0 \le t \le t_0 \tag{2.27}$$

and $I_1 = -\tilde{I}$. The zero current cross-over instant represents the solution of Eq. (2.23) for t when i_L is equal to zero, i.e.,

$$t_x = \tau \log\left(1 - \frac{\tilde{I}R}{V_s}\right). \tag{2.28}$$

The average thyristor current, namely $\overline{I}_t$, average diode current, $\overline{I}_d$, and mean source current, $\overline{I}_s$, can be found by integration of the load current over the appropriated bounds (assuming alternating zero volt loops)

$$\overline{I}_t = \frac{1}{t_1}\int_{t_x}^{t_1} i'_L dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i''_L(t)dt, \tag{2.29}$$

where the currents are the same in Eqs. (2.23)-(2.27), and

$$\overline{I}_d = -\frac{1}{t_2}\int_0^{tx} i'_L dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i''_L(t)dt. \tag{2.30}$$

The average source current is related to the average semiconductor device currents by

$$\overline{I}_s = 2\left(\overline{I}_T - \overline{I}_D\right). \tag{2.31}$$

The Fourier series of the output voltage V_L is the following

$$V_L = \frac{4}{n}V_s \sum_{n\ \text{odd}}^{\infty} \frac{cos\frac{1}{2}n\alpha}{n} \sin n\omega_0 t, \tag{2.32}$$

and for $n = 1$, the rms fundamental of the output voltage v_{o1} is given by $0.90 \times V_s \times \cos\frac{1}{2}\alpha$. The characteristics of these load voltage harmonics are shown in Fig. 2.2.

The current load can be expressed in Fourier series as

$$i_L(\omega t) = \sum_{n=1,3,5,\ldots}^{\infty} I_n \sin(n\omega_0 t - \phi_n) \tag{2.33}$$

where $I_n = \frac{4}{n}\frac{V_s}{nZ_n}\cos\frac{1}{2}n\alpha$ whence

$$I_{n,rms} = \frac{1}{\sqrt{2}}I_n \qquad Z_n = \sqrt{R^2 + (n\omega_0 L)^2} \qquad \phi_n = \tan^{-1}\frac{n\omega_0 L}{R}. \tag{2.34}$$

The load power is given by the sum of each harmonic power component. A variation of the basic four-switch dc to ac single-phase H-bridge is the half-bridge version where two series switches (one pole or leg) and diodes are replaced by a split two-capacitor voltage source. This reduces the number of semiconductors and gate circuit requirements, but at the expense of halving the maximum output voltage.

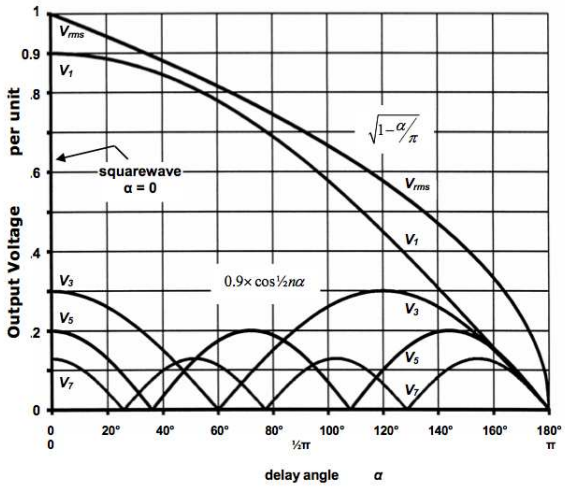

Fig. 2.2. Full bridge inverter output voltage harmonics normalised with respect to square rms output voltage $V_{rms} = V_s$.

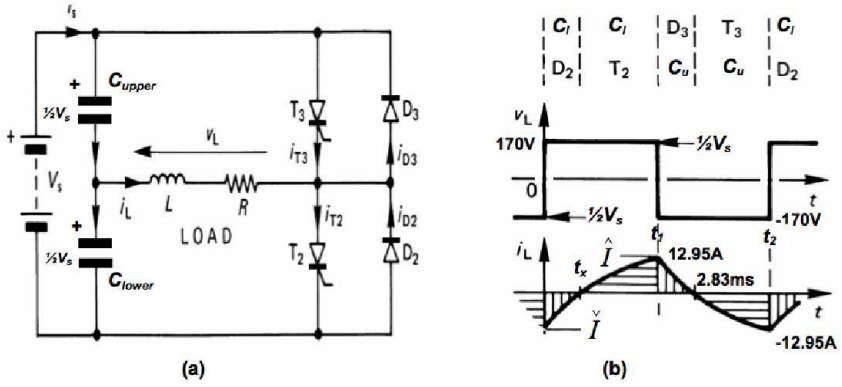

Fig. 2.3. GCT thyristor single-phase half-bridge inverter: (a) circuit diagram; (b) square-wave output voltage

2.2.2 Pulse width modulation technique

The standard pulse-width modulation techniques, (references [41, 49, 82, 42, 5, 53] and the bibliography therein) that are normally implemented to obtain desired output voltage amplitude and frequency, can de divided into

- bipolar pulse width modulation, and
- multi-polar pulse width modulation.

The main voltage output difference between the two methods is the harmonic content near the carrier frequency and its harmonics. Three-phase

PWM is a naturally extension to the single-phase case, except for the fact that single-phase PWM offers more degrees of flexibility than its application to three phase inverters, although three-phase PWM does have the attribute of triplen harmonic cancellation, due to the use of one (co-phasal) triangular carrier.

2.2.3 Bipolar pulse width modulation

Bipolar modulation is the simplest PWM method that requires a comparison between a fixed-frequency, magnitude triangular carrier and the desired AC waveform, called the modulation waveform. The modulation is usually a sinusoid of magnitude (modulation index) M such that $0 \leq M \leq 1$. The waveforms in Fig. 2.4 underline how the load voltage V_L takes values between the two voltage levels, $+V_s$ and $-V_s$ (hence the term bipolar output voltage), according to

- T_1 and T_2 are on when $v_{ref} > v_d$ (T_3 and T_4 are off) such that $V_L = +V_s$.
- T_3 and T_4 are on when $v_{ref} < v_d$ (T_1 and T_2 are off) such that $V_L = -V_s$

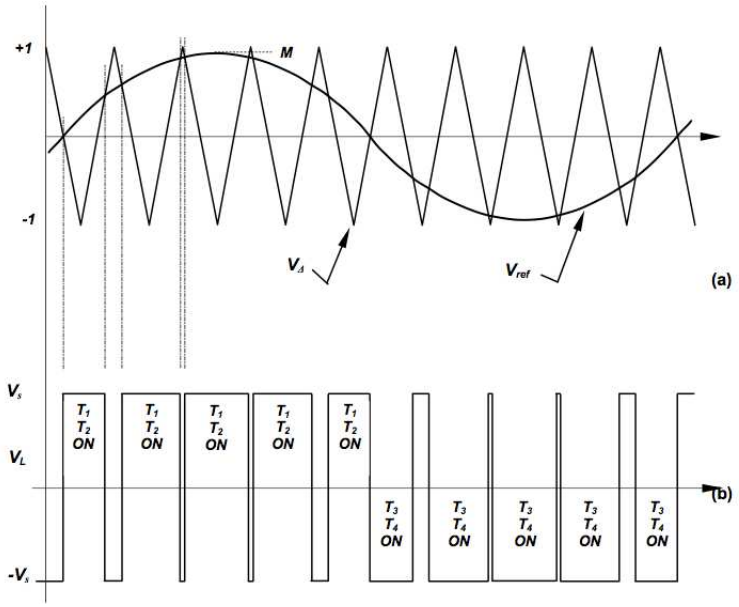

Fig. 2.4. Bipolar pulse width modulation: (a) carrier and modulation waveforms and (b) resultant load pwm waveform

2.2.4 Multi-polar pulse width modulation

There exists two multi-polar output voltage techniques with single-phase voltage-fed bridges. In both cases, two triangular carries displaced by π radiant provide the same output for the same switching frequency. The waveform in Fig. 2.5 shows that the load voltage V_L takes values between the two voltage levels ($+V_s$ and $-V_s$ respectively) with inter-spaced zero periods, hence the term multilevel, specifically three-level in this case, 0, $+V_s$ and $-V_s$, according to

- T_1 is on when $v_{ref} > v_d$ such that $V_{a0} = +V_s$;
- T_4 is on when $v_{ref} < v_d$ such that $V_{a0} = 0$;
- T_3 is on when $v_{ref} < -v_d$ such that $V_{b0} = V_s$;
- T_2 is on when $v_{ref} > -v_d$ such that $V_{b0} = 0$.

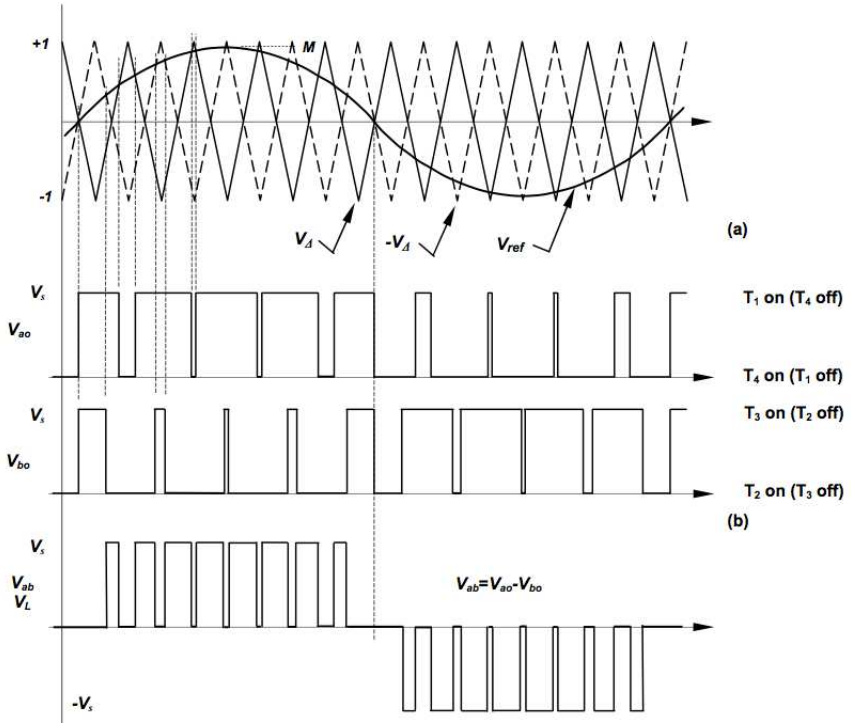

Fig. 2.5. Multilevel (3 level) pulse width modulation: (a) carrier and modulation waveforms and (b) resultant load pwm waveform

The multilevel load output voltage is the difference between the two leg voltage defines as:

- T_1 and T_2 are on such that $V_{ao} = +V_s$, $V_{bo} = 0$, $V_{ab} = +V_s$;

- T_2 and T_3 are on such that $V_{ao} = 0$, $V_{bo} = +V_s$, $V_{ab} = -V_s$;
- T_1 and T_3 are on such that $V_{ao} = +V_s$, $V_{bo} = +V_s$, $V_{ab} = 0$;
- T_2 and T_4 are on such that $V_{ao} = 0$, $V_{bo} = 0$, $V_{ab} = 0$.

The two zero output states are interleaved to balance switching losses between all four bridge switches. Device switching is at the carrier frequency, but the bridge load voltage (hence load current) experiences twice the leg switching frequency since the two carriers are displaced by π radiants. In Fig. 2.5 is reported another typology of unipolar approach, where the triangular carriers are not only displaced by π radiants, but are also vertically displaced. The upper triangle modulates reference values greater than zero, while the lower triangle modulates when the reference is less than zero.

2.2.5 Spectral comparison between bipolar and multilevel pwm waveforms

The main characteristics of the H-bridges inverter output voltage with bipolar pwm are:

- a triangular carrier has only odd Fourier components, so the output spectrum only has carrier components at odd harmonics of the carrier frequency;
- the first carrier components occur at the carrier frequency f_c;
- side-band components occur spaced by $2f_0$, where f_0 is the fundamental frequency, from other components, around all multiples of the carrier frequency f_c.

The principal properties of the H-bridges inverter output voltage with multilevel pwm are (as reported in Figure 2.6):

- the output switching frequency is double $2f_c$ each leg switching frequency f_c since the switching of each leg is time-shifted (by π radiants) hence the first carrier related components in the output occur at $2f_c$ and then at multiples of $2f_c$;
- no triangular carrier Fourier components exist in the output voltage since the two carriers are in anti-phase (π apart) effectively cancelling one another in spectrum terms;
- side-band components occur spaced by $2f_0$ from other components around each multiple of the carrier frequency $2f_c$.

2.2.6 Three-phase inverter

The classical scheme of a three-phase voltage-source inverter (VSI) bridge is reported in Fig 2.8. As it can be easily noted, the scheme involves six power switches together with six reactive energy feedback diodes. The three inverter legs are active at a time displacement, or phase, equal to $\frac{2}{3}\pi$.

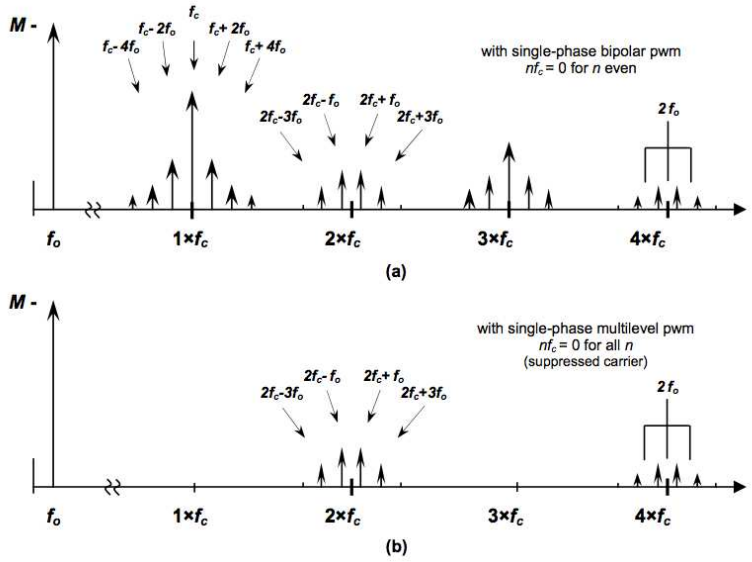

Fig. 2.6. Typical phase output frequency spectrum, at a give switch commutation frequency, for: (a) bipolar pmw and (b) multilevel pwm

Each switch conducts for π radiants, in order to avoid that two series connected (leg or arm) semiconductor switches across the voltage rail conduct simultaneously. There are six different patterns for one output cycle and the rate of sequencing these patterns, $6f_0$, specifies the bridge output frequency f_o.

The three output voltage waveforms can be derived by analysing a balanced resistive star load and considering each of the six connection patterns (see Fig. 2.12 for better explanation).

Rotating voltage space vector technique [13, 52, 10] can be adopted to analyse the three-phase output voltages. This technique is based on encoding the three voltage states of the output voltages from each of the three inverter legs (or poles), where a bit equal to the unity means the upper switch in the leg is on, while a bit equals to zero means the lower switch is on in that leg. The resultant binary number (one bit fro each of the three inverter legs) represents the output voltage vector number.

The rotational stepping sequence has been created in order to change only one leg state per time when rotating, that is only one device turns off and then the complementary switch of that leg turns on, at each step. Such aspect permits to obtain minimum inverter switching losses. The dwell time of the created rotating vector at each of the six vector positions is $\frac{T}{6}$ of the cycle period T. Note that the line-to-line zero voltage states 000 and 111 are not used due to the fact that these configurations represent when either all the upper

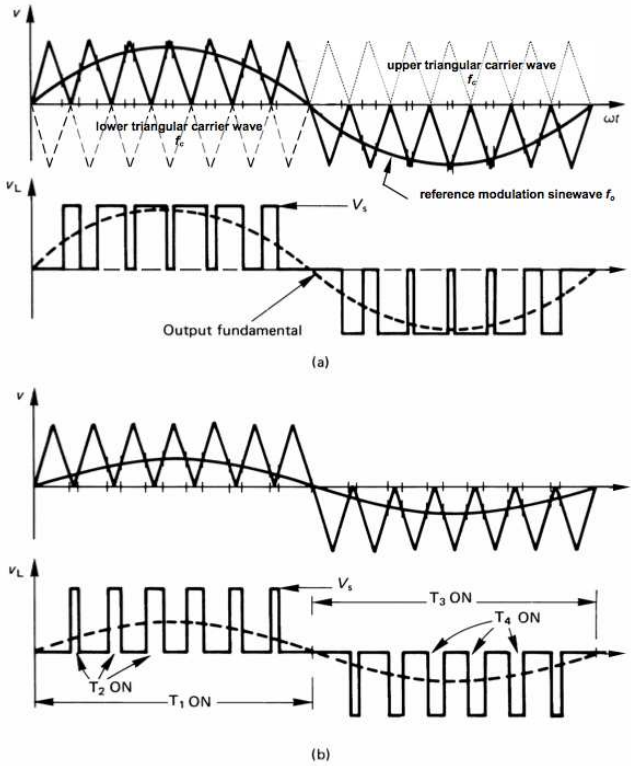

Fig. 2.7. Derivation of trigger signals for multi-level naturally sampled pulse-width modulation waveforms: (a) for high fundamental output voltage and (b) for a lower output voltage, with conduction devices shown.

switches (T_1, T_3, T_5) are on or all the lower switches (T_2, T_4, T_6) are switched on. Phase reversal can be obtained by interchanging two phase outputs or, as it is the preferred method, the direction of the rotating vector sequence is reversed. Reversing is therefore effectively achieved by back-tracking along each output waveform. It is straightforward to obtain that the line-to-load neutral voltage, in its Fourier series representation, is given by

$$V_{n_{L-N}} = \frac{2}{\pi} V_s \sum_{n=1,6r\pm1}^{\infty} \frac{\sin n\omega t}{n} \quad r = 1, 2, 3, \ldots \tag{2.35}$$

that is

$$v_{RN} = \frac{2}{\pi} V_s \left[\sin \omega t + \frac{1}{5} \sin 5\omega t + \frac{1}{7} \sin 7\omega t + \frac{1}{11} \sin 11\omega t + \ldots \right]. \tag{2.36}$$

The same structure is still valid for voltages v_{YN} and v_{BN} by substituting the ωt with the corresponding $\omega t + \frac{2}{3}\pi$ and $\omega t - \frac{2}{3}\pi$ respectively. The line-to-line voltage is so expressed as

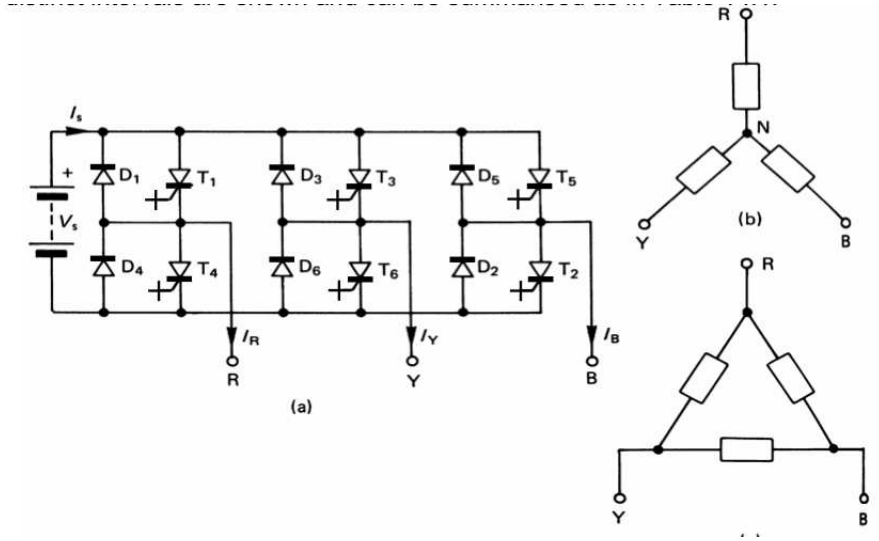

Fig. 2.8. Three-phase VSI inverter circuit: (a) GCT thyristor bridge inverter; (b) start-type and delta-type load

$$V_{n_{L-L}} = \frac{2\sqrt{3}}{\pi} V_s \sum_{n=1,6r\pm1}^{\infty} sign(\cos\frac{n\pi}{6}) \frac{\sin n\omega t}{n} \quad r = 1, 2, 3, \ldots, \tag{2.37}$$

that is

$$v_{RB} = \frac{2\sqrt{3}}{\pi} V_s \left[\sin\omega t - \frac{1}{5}\sin 5\omega t - \frac{1}{7}\sin 7\omega t + \frac{1}{11}\sin 11\omega t + \ldots\right], \tag{2.38}$$

and similarly for v_{BY} and v_{YR}. In Fig. 2.9(b) it is evident as v_{RB} is shifted by $\frac{1}{6}\pi$ with respect to v_{RN} hence to obtain the three line voltages, while maintaining a v_{RN} reference, ωt should be substituted with $\omega t + \frac{1}{6}\pi$, $\omega t - \frac{1}{2}\pi$ and $\omega t - \frac{5}{6}\pi$, respectively. Since the inter-phase voltages consist of two square waves displaced by $\frac{2}{3}\pi$, no triplen harmonics exist. The outputs comprise harmonics given by the series $n = 6r \pm 1$ with an integer $r \geq 0$. The n^{th} harmonic has a magnitude of $\frac{1}{n}$ relative to the fundamental. In Fig. 2.13 are indicated the main properties for a three-phase inverter output voltage.

Another technique to control the inverter scheme presented in Fig. 2.8 consists in a conduction phase for each switch equal to $\frac{2}{3}\pi$ [63]. As a result, at any instant, only two switches (one upper and one non-a complementary lower) conduct and the resultant quasi-square output voltage waveforms are shown in Fig. 2.15.

A $\frac{\pi}{3}$ radiants dead-time exists between two series switches conducting that implies providing a safety margin against simultaneous conduction of the two series devices across the dc supply. However, a lower semi-conductor device utilisation and less rms output voltage are present.

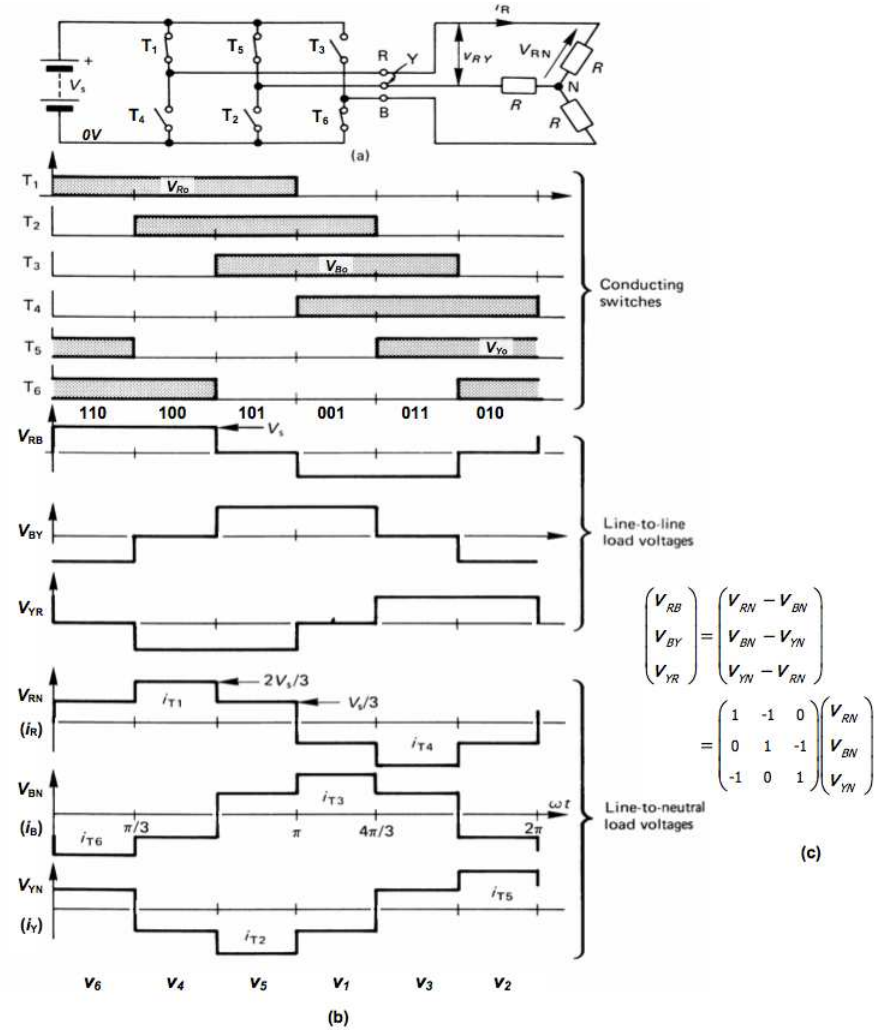

Fig. 2.9. A three-phase bridge inverter employing π switch conduction with a resistive load: (a) the bridge circuit (b) circuit voltage and current waveforms.

By an analysis of the results above exposed it is easy to verify that the line to neutral voltage of one conduction pattern is proportional to the line-to-line voltage of the other.

2.3 Common inverter control techniques

In the most of the applications cases it is required to set up both the amplitude and frequency of the load voltage and current or, in the case of an induction

Interval	***Three** conducting switches*								*leg state*	*voltage vector*
1	T_1	T_2	T_3						101	v_5
2		T_2	T_3	T_4					001	v_1
3			T_3	T_4	T_5				011	v_3
4				T_4	T_5	T_6			010	v_2
5					T_5	T_6	T_1		110	v_6
6						T_6	T_1	T_2	100	v_4

Fig. 2.10. Quasi-square-wave six conduction states - π radiants

motor, to control the shaft speed and torque by maintaining a constant V/f ratio. The main VSI modulation control techniques are the following:

- Variable voltage dc link;
- Single-pulse width modulation;
- Multi-pulse width modulation;
- Multi-pulse, selected notching modulation;
- Sinusoidal pulse width modulation;
- Triple injection
  - Triplens injected into the modulation waveform;
  - Voltage space vector modulation;

2.3.1 Variable voltage dc link

The rms voltage of a square-wave can be changed and controlled by varying the dc link source voltage. A variable dc link voltage can be achieved with a dc chopper or an ac phase-controlled thyristor bridge. A dc link $L-C$ smoothing filter may be necessary.

2.3.2 Single-pulse width modulation

Simple pulse-width control can be employed where a single-phase bridge is used to produce a quasi-square-wave output voltage as shown in Fig. 2.16. By phase-shifting the output by α, a quasi-square sum results as shown in Fig. 2.16 (b).

The output voltage can be described by the following expression

$$V_o = \sum_{\text{n odd}}^{\infty} v_{an} \sin n\omega t, \tag{2.39}$$

where

$$v_{an} = \frac{4}{n\pi} V_s \cos \frac{1}{2} n\alpha. \tag{2.40}$$

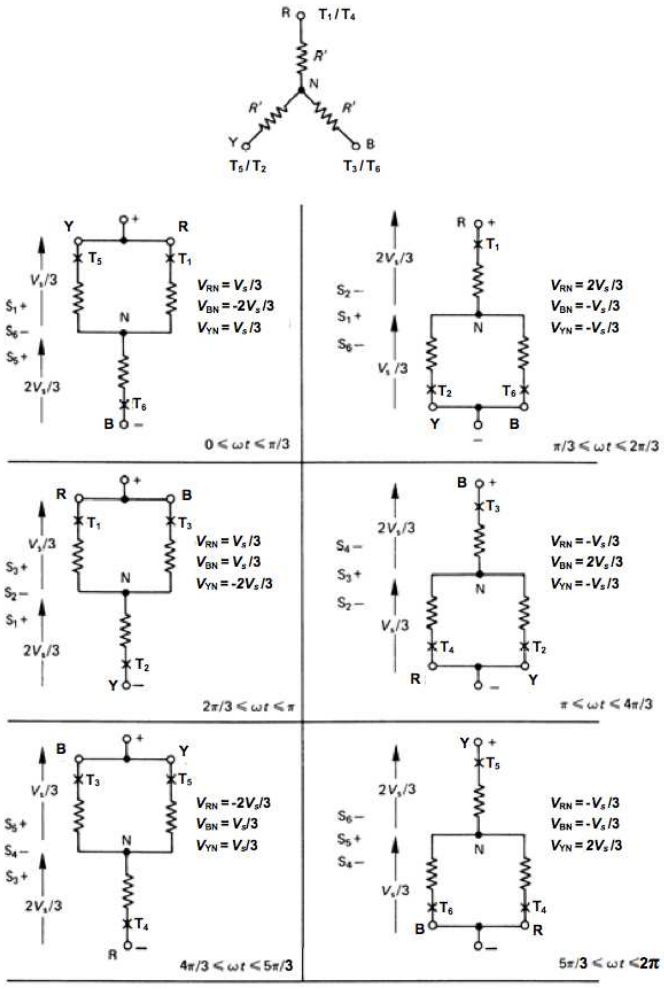

Fig. 2.11. Determination of the line-to-neutral voltage waveforms for a balanced resistive load and π radiants conduction.

The rms output voltage is $V_r = V_s\sqrt{1-\frac{\alpha}{\pi}}$ and the rms value of the fundamental is

$$V_1 = \frac{2\sqrt{2}}{\pi}V_s \cos\frac{1}{2}\alpha. \tag{2.41}$$

The amplitude of the harmonics increases as parameter α increases and in the meanwhile becoming comparable with the fundamental magnitude. This type of control may be used in high power applications.

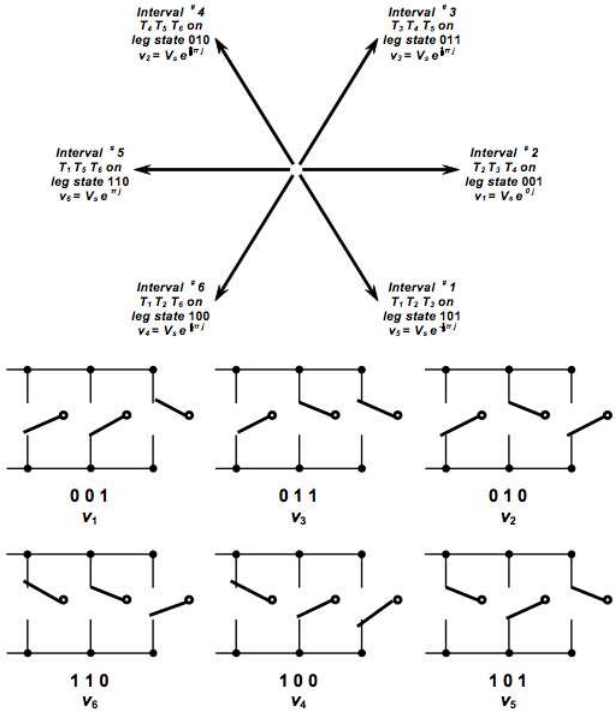

Fig. 2.12. Generation and arrangement of the six quasi-square inverter output voltage states.

2.3.3 Multi-pulse width modulation

An extension of the single-pulse modulation technique is multiple-notching as shown in Fig. 2.17. The bridge switches are controlled in order to vary the **on** to **off** time of each notch, namely δ, thereby varying the output rms voltage which is given by $V_{rms} = \sqrt{\delta} V_s$. Alternatively, the number of notches can be varied. The harmonic content at lower output voltages is significantly lower than the one obtained with single-pulse modulation. The increased switching frequency does increase the magnitude of higher order harmonics and the switching losses. The Fourier coefficients of the output voltage are given by

$$V_n = \frac{4}{n\pi} \sum_{j=1,2,3,\ldots}^{\frac{f_c}{f_0}} \left[\cos 2\pi \frac{f_o}{f_c} n(2j - 1 + \delta) - \cos 2\pi n \frac{f_o}{f_c} (2j - 1 - \delta) \right], \quad (2.42)$$

where $0 \leq \delta \leq 1$ is the duty cycle.

Conduction period	Fundamental voltage		Characteristic		
	peak	rms	Total rms	Distortion Factor	THD
	$\hat{V}_1$	V_1	V_{rms}	μ	thd
180°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{2}{\pi}V_s = 0.637V_s$	$\frac{\sqrt{2}}{\pi}V_s = 0.450\,V_s$	$\frac{\sqrt{2}}{3}V_s = 0.471V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{2\sqrt{3}}{\pi}V_s = 1.10\,V_s$	$\frac{\sqrt{6}}{\pi}V_s = 0.78\,V_s$	$\sqrt{\frac{2}{3}}V_s = 0.816V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
120°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{\sqrt{3}}{\pi}V_s = 0.551\,V_s$	$\frac{\sqrt{6}}{2\pi}V_s = 0.390\,V_s$	$\frac{1}{\sqrt{6}}V_s = 0.408V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{3}{\pi}V_s = 0.955V_s$	$\frac{3}{\sqrt{2}\pi}V_s = 0.673\,V_s$	$\frac{1}{\sqrt{2}}V_s = 0.707V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$

Fig. 2.13. Quasi-squarewave voltage properties.

2.3.4 Multi-pulse, selected notching modulation

A multi-level waveform $(\pm V_s, 0)$ can be used with quarter wave symmetry, as shown in Figure 2.17, to control both the harmonics and total rms output voltage. If only one pulse is chosen per quarter wave, the k^{th} harmonic can be annihilated from the output voltage if the centre of the pulse is located such that

$$\sin(k\lambda) = 0 \qquad \text{i.e. } \lambda = \frac{\pi}{k}. \tag{2.43}$$

The output voltage total rms depends only on the pulse width δ and is given by $V_s\sqrt{\frac{2}{\pi}\delta}$. On the other hand, the bipolar waveform $(\pm V_s)$ has an rms value of V_s, independent of the harmonics eliminated. The exact switching points are calculated off-line so as to eliminate the required harmonics. It has to be remarked that the more notches, the lower is the output fundamental. The multi-pulse selected notching modulation technique can be translated into a *optimal pulse-width modulation problem control*, where harmonics may not be eliminated, but minimized according to a specific cost function. In this framework, the switching angles that are present in the quarter wave output are tuned to eliminate certain harmonics, minimizing the rms of the ripple current or any other desired performance index. The resultant non-linear equations are solved using numerical methods off-line. A set of angles

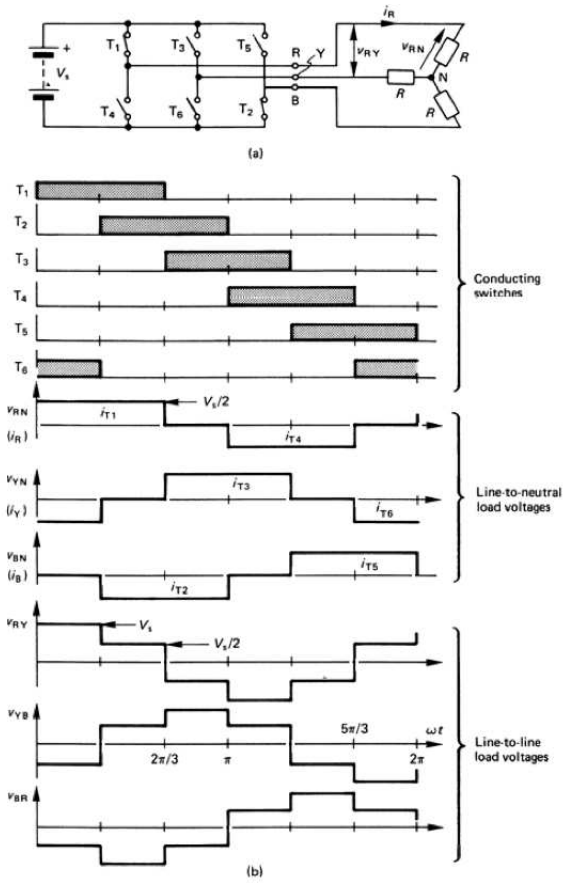

Fig. 2.14. A three-phase bridge inverter employing $\frac{2}{3}\pi$ switch conduction with a resistive load: (a) the circuit with T_1 and T_2 conducing and (b) voltage and current waveforms

Interval	***Two** conducting devices*						
1	T_1	T_2					
2		T_2	T_3				
3			T_3	T_4			
4				T_4	T_5		
5					T_5	T_6	
6						T_6	T_1

Fig. 2.15. Quasi-squarewave conduction states - $\frac{\pi}{3}$ radiants conduction.

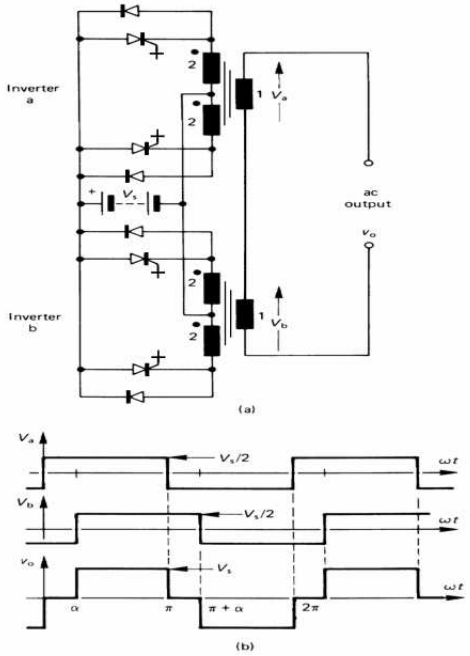

Fig. 2.16. Voltage control by combining phase-shifted push-pull inverters: (a) two inverters scheme and (b) circuit voltage waveforms for a phase displacement α

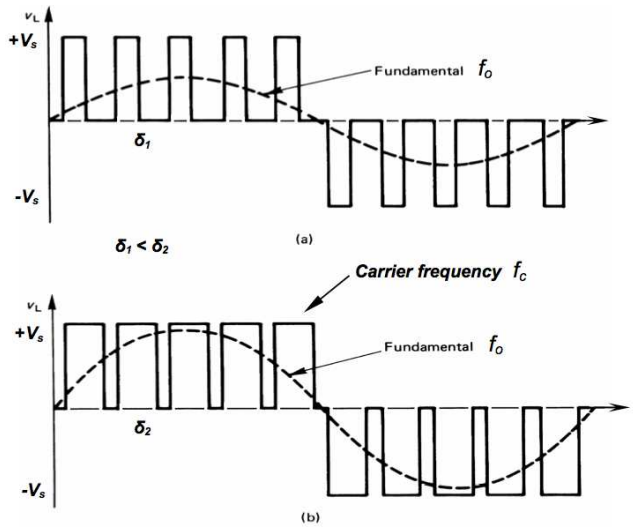

Fig. 2.17. Inverter control giving variable duty cycle of five notches per half cycle: (a) low and (b) higher duty cycle

must be computed and stored for each desired level of the voltage fundamental and output frequency. The optimal pwm approach is particularly useful for high-power, high-voltage GCT thyristor inverters which tend to be limited in switching frequency by device switching losses.

2.3.5 Sinusoidal pulse-width modulation

The sinusoidal pulse-width modulation can be furthermore classified in

- natural sampling modulation, or
- regular sampling modulation.

Both the methodologies can be split also into modulation with synchronous carrier and modulation with asynchronous carrier. The output voltage waveform generated by synchronous carrier, natural sampling sinusoidal pwm are illustrated in Figure 2.7. The switching points are determined by the intersection of the triangular carrier wave and the reference modulation sine wave. The output frequency is at the sine-wave frequency f_o and the output voltage is proportional to the magnitude of the sine wave. The parameter M, with $(0 \leq M \leq 1)$, is called the modulation index. If the frequency of the modulation sine wave, namely f_o, is an integer multiple of the triangular wave carrier-frequency, indicated as f_c that is, $f_c = nf_o$ where n is integer, then the modulation is synchronous, as shown in Figure 2.7. If n is odd then the positive and negative output half cycles are symmetrical and the output voltage contains no even harmonics. In a three-phase system if n is a multiple of 3 (and odd), the carrier is a triplen of the modulating frequency and the spectrum does not contain the carrier or its harmonics,

$$f_c = (6q + 3)f_o = nf_o \quad q = 1, 2, 3, \ldots. \tag{2.44}$$

The Fourier harmonic coefficients of the line to line voltages are given by

$$a_n = V_l \cos\left(\frac{n}{1}\pi\right) \cos\left(\frac{n}{3}\pi\right), \tag{2.45}$$

$$b_n = V_l \sin\left(\frac{n}{1}\pi\right) \sin\left(\frac{n}{3}\pi\right) \tag{2.46}$$

where V_l is proportional to the dc supply voltage V_s and the modulation index M. The carrier frequency must be much higher than the modulation frequency. The generated output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave. If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics. Rather than using two offset triangular carriers, as shown in Figure 2.7, a triangular carrier without offset can be used. To better clarify such a technique, Figure 2.18

shows the pwm generation scheme and the voltage bipolar output waveform, when applied to the three-phase VSI inverter. Only one switch in the inverter leg must always be on.

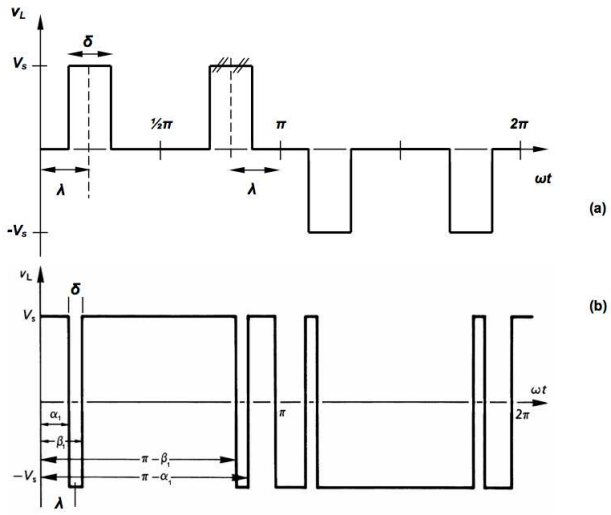

Fig. 2.18. Output voltage harmonic reduction for a single-phase bridge using selected notching: (a) multilevel output voltage and (b) bipolar output voltage

Unlike the waveforms reported in Figure 2.17, no zero voltage output periods exist. This has the effect that, in the case of GCT thyristor bridges, a large number of commutation cycles is required. In the presence of zero output periods, in fact, one GCT thyristos is commutated and the complementary device in that leg is turned off. The previously commutated device can be turned back on without the need to commutate the complementary device, as would be required in other cases. Commutation losses are reduced, control circuitry simplified and the likelihood of simultaneous conduction of two series leg devices is reduced. When the carrier is not an integer multiple of the modulation waveform, asynchronous modulation results. Because the output frequency f_o is usually variable over a wide range, it is difficult to ensure $f_c = nf_o$. To achieve synchronism, the carrier frequency must vary with frequency f_o. Simpler generating systems are obtained if a fixed carrier frequency is used, resulting in asynchronism between f_o and f_c at most output frequencies. When a fixed carrier frequency is used, usually no attempt is made to synchronize the modulation frequency. The output waveforms do not have quarter-wave symmetry which produces sub-harmonics. Such subharmonics can be neglected if $f_c \gg f_o$, usually, $f_c > 20f_o$. The implementation of sinusoidal pwm with microprocessors or digital signal processors is common because of flexibility and the elimination of analogue circuity associated prob-

lems. The digital pwm generation process involves scaling, by multiplication, of the per unit sine-wave samples stored in ROM. The multiplication process is time-consuming [63, 65], hence natural sampling is not possible. In order to minimize the multiplication rate, the sinusoidal sine-wave reference is replaced by a quantised stepped representation of the sine-wave. Figure 2.19 shows two methods where sampling is synchronized to the carrier frequency and the multiplication process is performed at twice the sampling rate for three-phase pwm generation (the third phase can be expressed in terms of two phases).

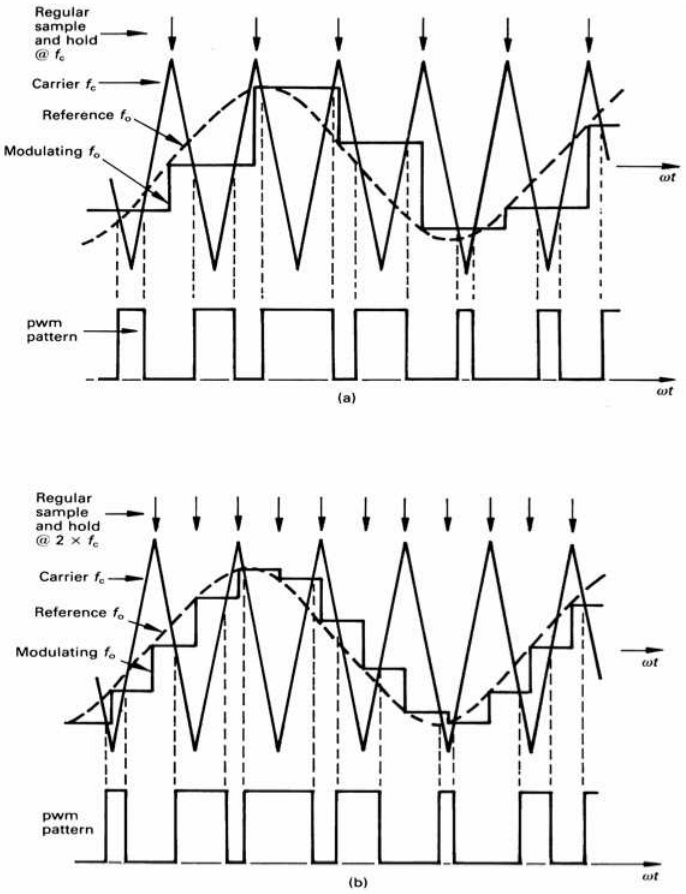

Fig. 2.19. Regular sampling, asynchronous, sinusoidal pulse-widt-modulation: (a) symmetrical and (b) asymmetrical modulation

In the (a) part of Figure 2.19 there is illustrated the process of symmetrical modulation, where sampling is at the carrier frequency. The quantized

sine-wave is stepped and held at each sample point. The triangular carrier is then compared with the step sine-wave sample and the modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier with the stepped sine-wave, about the non-sampled carrier peak, are equidistant about the carrier peak. The pulse width, independently of the modulation index M, is symmetrical about the triangular carrier peak not associated with sampling, as illustrated by the upper pulse in Figure 2.20.

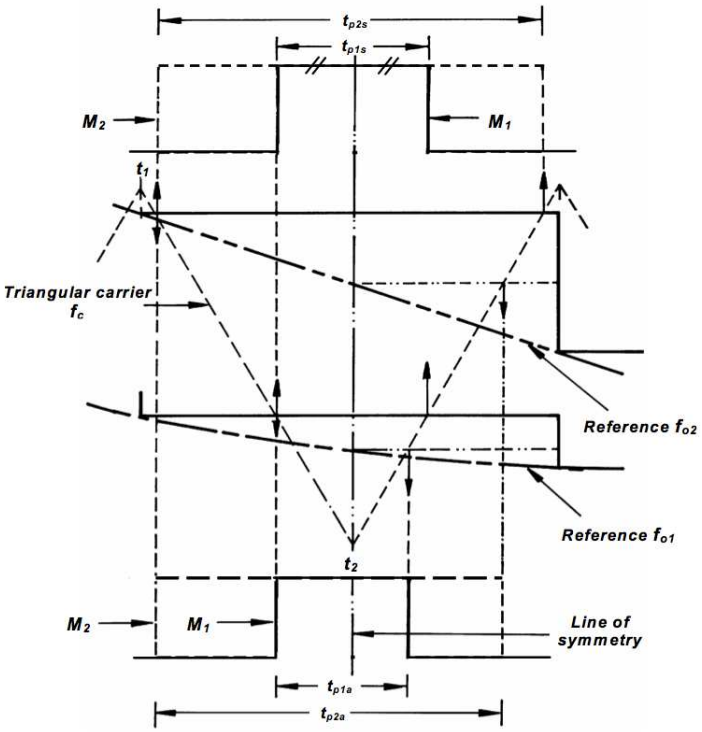

Fig. 2.20. Regular sampling, asynchronous, sinusoidal pulse-widt-modulation

The pulse width can be expressed as follows

$$t_{ps} = \frac{1}{2f_c}(1 - M \sin 2\pi f_o t_1) \tag{2.47}$$

where t_1 is the time of sampling. Asymmetrical modulation is produced when the carrier is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency, as shown in Figure 2.19(b). Each side of the triangular carrier about a sampling point intersects the stepped waveform at different step levels. The resultant pulse width is asymmetrical about the

sampling point. The pulse width can be now expressed as

$$t_{pa} = \frac{1}{2f_c}\left[1 - \frac{1}{2}M\left(\sin 2\pi f_o t_1 + \sin 2\pi f_o t_2\right)\right] \tag{2.48}$$

where t_1 and t_2 are the times at sampling such that $t_2 = t_1 + \frac{1}{2f_c}$. Figure 2.20 shows that a change in the modulation index M varies the pulse width on each edge, termed double edge modulation. A triangular carrier produces double edge modulation, while a sawtooth carrier produces single edge modulation, independent of the sampling technique.

Frequency spectra comparison

The most common technique of sinusoidal modulation for three-phase inverters is represented by the regular-sampling, asynchronous, fixed frequency carrier pulse width modulation. If $f_c > 20f_o$, low frequency sub-harmonics can be neglected. The output spectra consists of the modulation frequency f_o with magnitude M. Other spectra components are also present associated with the triangular carrier, f_c. For any sampling, these are f_c and the off harmonics of f_c. These decrease in magnitude with increasing frequency. About the frequency nf_c there exist components of f_o spaced at $\pm 2f_o$ which generally decrease in magnitude when further away from nf_c, i.e., at f_c the no-zero harmonics are f_c, $f_c \pm 2f_o$, $f_c \pm 4f_o$, ..., while about $2f_c$ the present harmonics are $2f_c \pm f_0$, $2f_c \pm 3f_o$, ..., but $2f_c$ is not present. The typical output spectrum is shown in Figure 2.21. The relative magnitudes of the side-bands vary with modulation depth and the carrier related frequencies present f_h are given by

$$f_k = \frac{1}{2}\left(1 + (-1)^{n+1}\right) nf_c \pm \left(2k - \frac{1}{2}\left(1 - (-1)^n\right)\right) f_c, \tag{2.49}$$

where $k = 1, 2, 3, \ldots$ (side-bands) and $n = 1, 2, 3, \ldots$ (carrier).

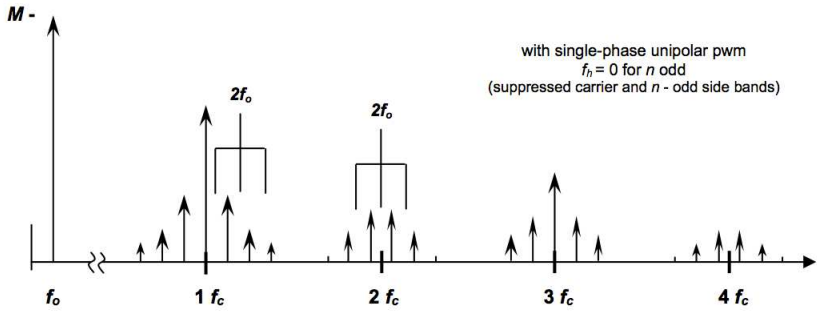

Fig. 2.21. Location of carrier harmonics and modulation frequency sidebands

The main difference between the proposed technique with respect to other various PWM techniques consists in the magnitude of the carrier harmonics and side-bands. The magnitude increase as the PWM type changes from naturally sampling to regular sampling, then from asymmetrical to symmetrical modulation, and finally from double edge to single edge. With a three-phase inverter, the carrier f_c and its harmonics do not appear in the line-to-line voltages since the carrier f_c and in particular its harmonics, are co-phasal to the three modulation waveforms. The magnitude of the fundamental when using standard pulse width modulation can be increased without introducing output voltage distortion, by the injection of triplen components, which are co-phasal in a three-phase system, and therefore do not appear in the line currents. Two basic approaches can be used to affect this undistorted output voltage magnitude increase

- triplen injection into the modulation waveform, or
- voltage space vector modulation.

2.3.6 Triplen injection modulation

Triplens injected into the modulation waveform

The third harmonic voltage injection permits to obtain higher magnitude of the output three-phase generated voltage with respect to the standard techniques. If over-modulation ($M > 1$) is not allowed, then the modulation wave $M \sin \omega t$ is restricted in magnitude to $M = 1$, as shown in Figure 2.22. In a three-phase pwm generator, to increase possible values of parameter M, it can be used the propriety of harmonics cancellation at $3f_o$ (and off multiplies of $3f_o$), yet ensuring modulation occurs for every carrier frequency cycle. The voltage V_{RN} has a maximum instantaneous value equal to the unity, at $\omega t = \pm\frac{1}{3}\pi$.

The fundamental of the phase voltage is $M' = 1.155M$. The increased fundamental has been reported in Figure 2.22(b). The spatial voltage vector technique injects the triplens in according to the following expression

$$V_{RN} = M' \left\{ \sin \omega t + \frac{1}{\sqrt{3}} \sum_{r=0}^{\infty} \frac{(-1)^r}{\left[(2r+1) - \frac{1}{3}\right]\left[(2r+1) + \frac{1}{3}\right]} \right\}. \tag{2.50}$$

Therefore, the spatial voltage vector waveform is defined as

$$\overline{v} = \begin{cases} \frac{3}{2}\sin(\omega t) & 0 \leq \omega t \leq \frac{1}{6}\pi \\ , \frac{\sqrt{3}}{2}\sin(\omega t + \frac{1}{6}\pi) & \frac{1}{6}\pi \; leq\omega t \leq \frac{1}{2}\pi. \end{cases} \tag{2.51}$$

The use of this reference increases the duration for the zero volt loops, thereby decreasing inverter output current ripple. The maximum modulation index is 1.155. Third harmonic injection, yielding $M = 1.155$ is a satisfactory approximation to spatial voltage vector injection.

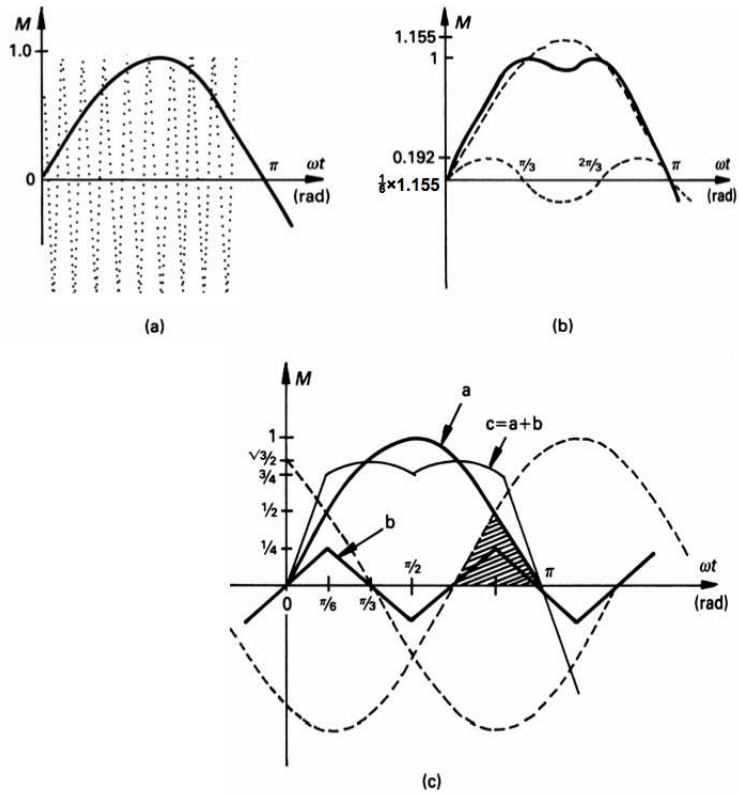

Fig. 2.22. Modulation reference waveforms: (a) sinusoidal reference; (b) third harmonic injection reference, and (c) triplen injection reference

2.3.7 Voltage space vector PWM

When generating three-phase quasi-square output voltages, the inverter switches step progressively to each of the six switch output possibilities (states). In Figure 2.12 when producing the quasi-square output, each of these six states is represented by an output voltage space vector that has a delay equal to $\frac{\pi}{3}$ from its two adjacent states, with the same length V_s. Therefore, the quasi-square three-phase output is generated by a rotating vector of length V_s, jumping successively from one output state to the next in the sequence, and creating six voltage output sectors. The speed of rotation, in particular the time for one rotation, determines the inverter output frequency. The sequence of voltage vectors $\{v_i, i = 1 \ldots, 5\}$ is arranged such that stepping from one state to the next involves only one of the three poles changing state. Thus the number of inverter devices, needing to change states (switch) at each transition, is minimised. The speed of rotation can be naturally changed: from one voltage space vector position to the next, producing a six-step quasi-square fixed mag-

nitude voltage output, the rotating vector is rotated in smaller steps based on the position being updated at a constant rate(carrier frequency). Furthermore, the vector length can be varied, modulating it, to a magnitude less than V_s. To incorporate a variable rotating vector length (modulation depth), it is necessary to vary the average voltage in each carrier period. Hence pulse width modulation is used in the period between each finite step of the rotating vector. Pulse width modulation requires the introduction of zero voltage output states, namely all the top switches on (state 111, v_7), or all the lower switches on (state 000,v_0) (see Figure 2.23).

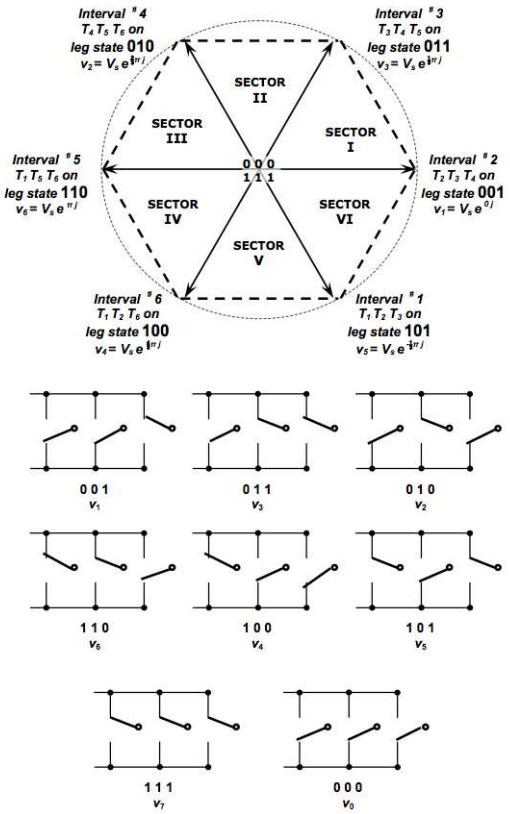

Fig. 2.23. Instantaneous output voltage states for the three legs of an inverter

The pole-to-pole output voltage can be annihilated, which allows duty cycle variation to achieve variable average output voltage for each phase, within carrier period, proportional to the magnitude of the position vector. There can exist vector configurations (or angles) that can be expressed as one of the six quasi-square output vector. To overcome such drawbacks, an intermediate vector $V_{o/p}e^{j\theta}$ is resolved into the vector sum of the two quasi- square vectors

adjacent to the rotating vector. This process is shown in Figure 2.24 for a voltage vector $V_{o/p}$ that lies in sector I, between output states $v_1(001)$ and $v_3(011)$. It is easy to observe that such vector has been resolved as sum of the two components V_a and V_b.

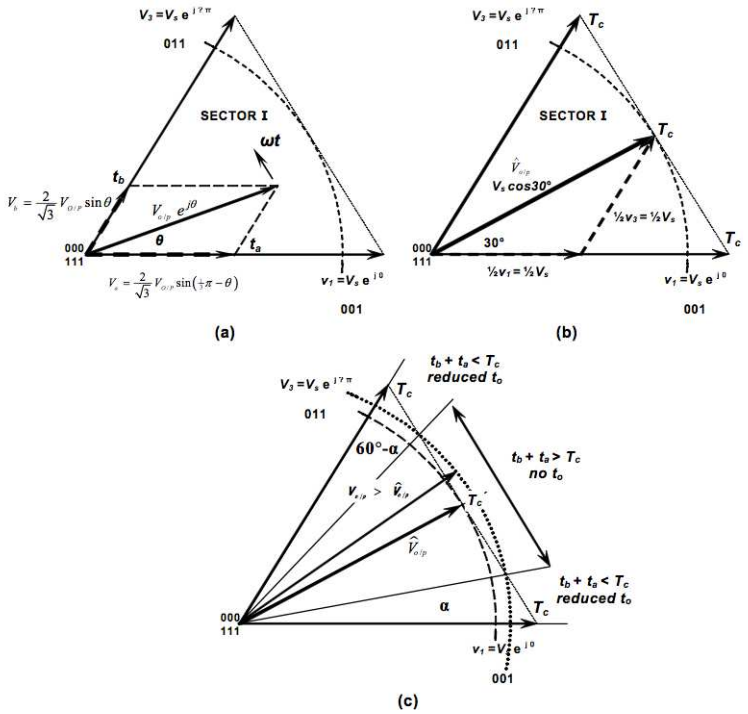

Fig. 2.24. First sector of inverter operational area: (a) general rotating voltage vector (b) maximum allowable voltage vector length (c) over modulation.

The time represented by quasi-square vectors v_1 and v_3 is the carrier period T_c, in each case. Therefore the portion of T_c associated with v_a and v_b is scaled proportionally to v_1 and v_3, giving t_a and t_b. The sum of such times cannot be greater than the carrier period T_c, by providing

$$t_a + t_b \leq T_c \tag{2.52}$$

and

$$t_o + t_a + t_b = T_c, \tag{2.53}$$

where the variable t_o represents a slack variable that is used to obtain an equality. Eq. (2.53) shows that the vector v_1 is used for a period t_a, whereas v_3 is used for a period t_b, and during period t_o, the null vector is used, v_0 and v_7 at the centre of the hexagon, which do not affect the average voltage

during the carrier interval T_c. A further constraint is imposed in the time domain. The rotating voltage vector is a fixed length for all the rotating angles, for a given inverter output voltage. Its length is restricted in both time and space. Obviously the resolved component lengths cannot exceed the pole vector length, V_s. Additionally, the two vector magnitudes are each a portion of the carrier period, where t_a and t_b could be both equal to T_c, that is, they both have a maximum length V_s. The shortest vector to the boundary is when both resolving vectors have a length $\frac{1}{2}V_s$. In this case, $t_a = t_b = \frac{1}{2}T_c$, that is $t_a + t_b = T_c$. Therefore for a constant inverter output voltage, when the rotating voltage vector has a constant length $\hat{V}_{o/p}$, the locus of allowable rotating reference voltage vectors must be within the circle described by the maximum length vector. This vector has length $v_1 \cos 30°$ and the full quasi-square vectors v_1,v_2 etc., which have a magnitude of V_s, cannot be used for generating a sinusoidal output voltage. The excess length of each quasi-square voltage (which represents time) is accounted for by using zero state voltage vectors for a period corresponding to that extra length ($1 - \cos 30°$ at maximum output voltage). Having calculated the necessary periods for the inverter poles (t_a, t_b and t_0), the carrier period switching pattern can be assigned in two ways:

- Minimised current ripple, and
- Minimised switching losses, using dead banding.

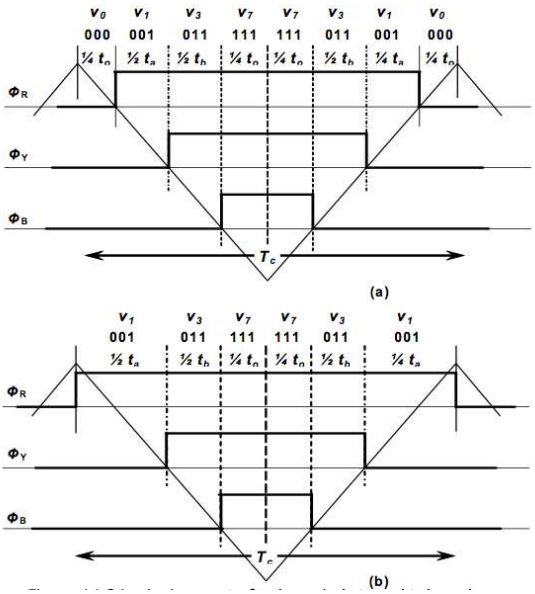

Fig. 2.25. Assignment of pole periods t_a and t_b: (a) minimum current ripple and (b) minimum switching transitions per carrier cycle.

Figure 2.25 reports both the scenarios. The waveforms are based on the equivalent of symmetrical modulation where the pulses are symmetrical about the carrier trough. Minimization of current ripple or switching transitions can be chosen. When dead banding, the zero voltage state v_0 is used in even numbered sextants and v_7 is used in odd numbered sextants. Side-band and harmonic component magnitudes can be decreased if double-edged modulation placement of the states is used, which requires recalculation of t_a, t_b and t_o at the carrier crest, as well as at the trough.

2.4 CSI bridge topologies

In the current source inverters (see [50, 21, 58, 18]), the dc supply presents high values of reactance, being inductive to maintain the required inverter output bidirectional current regardless the inverter load.

2.4.1 Single-phase inverter

A single-phase, controlled current-sourced bridge is shown in Fig 2.26 with its near square-wave output current.

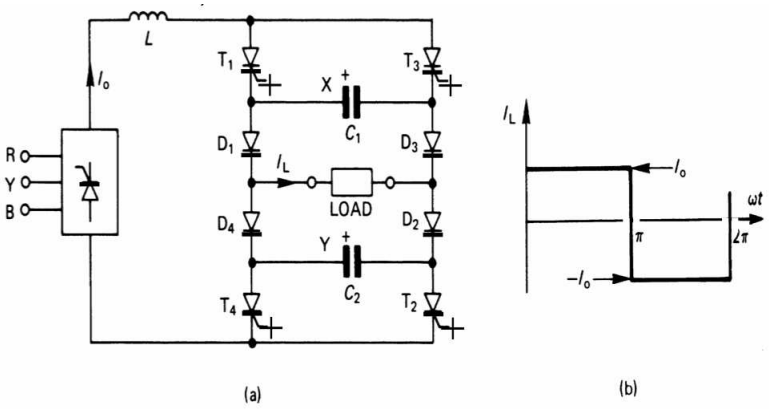

Fig. 2.26. Single-phase csi bridge inverter: (a) bridge circuit and (b) load current waveform

No free-wheel diodes are required and the thyristors required forced commutation and have to withstand reverse voltages. An inverter current path must be maintained at all times for the source controlled current. The circuit can be described by considering two phases. Firstly thyristors T_1 and T_2 are commutated by triggering thyristors T_3 and T_4. The capacitors impress negative voltages across the respective thyristors to be commutated off, as shown

in Figure 2.27. The load current is displaced from T_1 and T_2 via the path $T_3 - C_1 - D_1$, the load and $D_2 - C_2 - T_4$. The two capacitors discharge in series with the load, each capacitor reverse biasing the thyristor to be commutated, T_1 and T_2 as well as diodes D_3 to D_4. The capacitors discharge linearly (due to the constant current source).

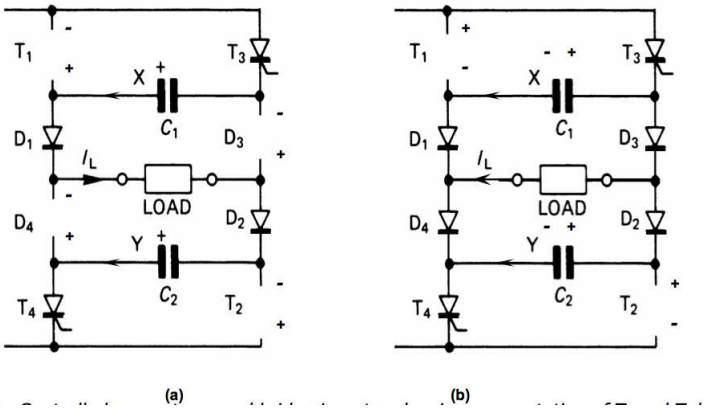

Fig. 2.27. Controlled-current source bridge inverter.

After that both capacitors are discharged, the load current transfers from D_1 to D_2 and from D_3 to D_4 which connects the capacitors in parallel with the load via diodes D_1 to D_2. The plates X and Y now charge negative, ready for the next commutation cycle, as shown in Figure 2.27(b). Thyristors T_1 and T_2 are now forward biased and must have attained forward blocking ability before the start of the second phase. The on-going thyristor automatically commutates the outgoing thyristor. This repeated commutation sequencing is a processed termed auto-sequential thyristor commutation. The load voltage is load dependent and usually has controlled voltage spikes during commutation.

2.4.2 Three-phase current source inverter

A three-phase controlled current-source inverter is shown in Figure 2.28.

Only two thyristors can be in their state *on* at any instant. The result is a quasi-square line current results. There is a $\frac{\pi}{3}$ phase displacement between commutation of an upper device followed by commutation of a lower device. An upper device (T_1, T_2, T_5) is turned on to commutate another upper device, and a lower device (T_2, T_4, T_6) commutates another lower device. The three upper capacitors are all involved with each upper device commutation while the same constraint applies to the lower capacitors. Thyristor commutation occurs in two distinct phases. In Figure 2.30 (a), the capacitors C_{13}, C_{35}, C_{51} are charged with the shown polarities as a result of the earlier commutation

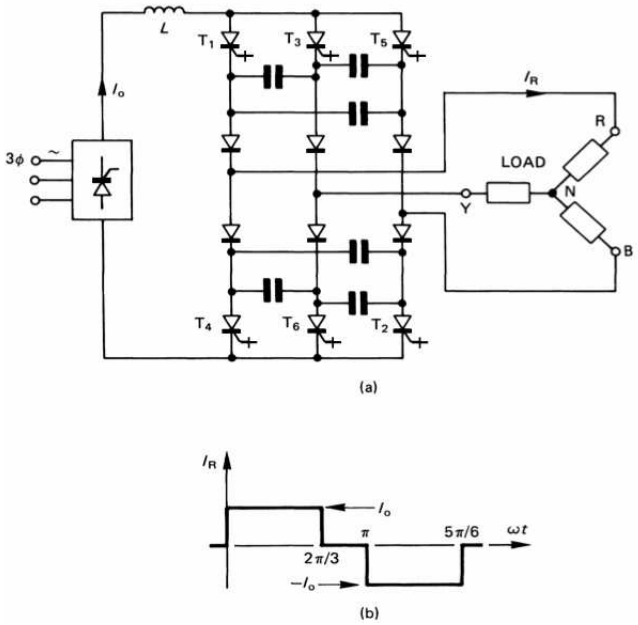

Fig. 2.28. Three-phase controlled-current sourced bridge inverter: (a) bridge circuit and (b) load current waveform

of T_5. T_1 is commutated by turning on T_3. During commutation, the capacitor between the two commutating switches is in parallel with the two remaining capacitors which are effectively connected in series. Capacitor C_{13} in series also provide t thyristor T_1 displacement current, thereby reverse biasing T_1. When the capacitors have discharged, T_1 becomes forward biased and must have regained forward blocking capability before the applied positive time derivative. The capacitor voltages reverse as shown in Figure 2.30 and when fully charged, diode D_1 ceases to conduct. Regardless of this commutation, lower thyristor T_2 is commutated by turning on T_4, $\frac{\pi}{3}$ radiants later.

Assisted capacitor commutation can greatly improve the capabilities of self-commutating thyristors, such as the GTO thyristors and GTC. A typical application for a three-phase current-sourced inverter would be to feed and control a three-phase induction motor. Varying load requirements are met by charging the source current level over a number of cycles by varying the link inductor input voltage. An important advantage of the controlled current source concept, as opposed to the constant voltage link, is good fault tolerance and protection. An output short circuit or simultaneous conduction in an inverter leg is controlled by the current source. Its time constant is usually longer than the one presented by the input converter, hence converter shut-down can be initiated before the link current can raise to critical levels. PWM techniques are applicable to current source inverters in order to reduce

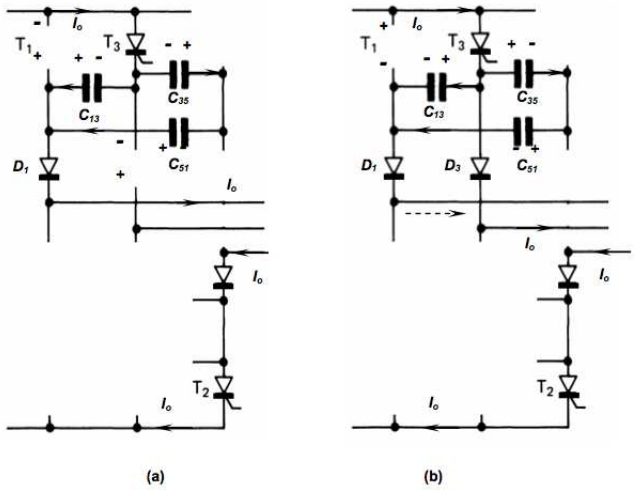

Fig. 2.29. Controlled-current sourced bridge inverter commutations

current harmonics, thereby reducing load losses and pulsating motor shaft torques. Since current source inverters are most attractive in very high-power applications, inverter switching is minimised by using optimal PWM. The central $\frac{\pi}{3}$ portion about the maxima of each phase cannot be modulated, since link current must flow and during such period both the order phases require the opposite current direction. Attempts to overcome such PWM restrictions include using a current sourced inverter with additional parallel current displacement paths. The auxiliary thyristors, T_{upper} and T_{lower} and capacitors, C_R, C_Y, and C_B, provide alternative current paths (extra control states) and temporary energy storage. The auxiliary thyristor can be commutated by the extra capacitors. Characteristics and features of current source inverters are the following

- The inverter is simple. The switching devices must have reverse blocking capability and experience high voltages (both forward and reverse) during commutation.
- Commutation capability is load current dependent and a minimum load is required. This limits the operating frequency and precludes uses in UPS systems. The limited operating frequency can result in torque pulsations.
- The inverter can recover from an output short-circuit hence the system becomes more reliable and fault tolerant.
- Current feed inverters tend to be larger in size and weight, because of the link inductor and filtering requirements.

2.5 Resonant inverters

The voltage source considered until now involve inductive loads. Moreover the switches experience simultaneous maximum voltage and current during turn-on and turn-off with an inductive load. On the other hand, CSI scheme devices require capacitive circuits to commutate the bridge switches. When self-commutable devices are used in current source inverters, hard switching occurs. Unlike standard topologies, the resonant inverters ([1, 33, 55, 56, 57, 88]) present load systems that enable commutation of the bridge switches with near zero voltage or current switch conditions, resulting in low switching losses. A characteristic of inductive-capacitive-resistive ($L-C-R$) resonant circuits is below presented:

- for a step load voltage, the series $L-C-R$ load current sinusoidally reverses or
- for a step load current, the parallel $L-C-R$ load voltage sinusoidally reverses.

If the load can be resonated, the switching stresses can be significantly reduced for a given power throughput, provided switching is synchronised to the voltage and current zero crossing. The principal family of resonant converters that makes use of zero voltage or current switching is the load-resonant converters category. Such resonant load converters are designed for an inductive-capacitive load, thereby providing load zero current or voltage intervals at which the converter switches can be commutated with minimal electrical stress. Two basic resonant-load single-phase inverters are used, depending on the load arrangement:

- current source inverter with a parallel $L-C$ resonant (tank) load circuit: switch turn-off at zero load voltage instants and turn-on with zero voltage switch overlap is essential (a continuous source current path is required)
- voltage source inverter with a series connected $L-C$ resonant load: switch turn-off at zero load current instants switch under lap is essential (to avoid dc voltage source short circuiting)

Each load circuit type can be fed form a single leg (or arm) circuit of H-bridge circuit depending on the load Q-factor. The Q factor is a widespread measure used to characterise resonators. It is defined as the peak energy stored in the circuit divided by the average energy dissipated in it per cycle at resonance. For a $R-L-C$ circuit it is equal to

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}. \tag{2.54}$$

Low Q circuits are therefore damped and lossy and high Q circuits are under-damped. The Q term is related to bandwidth; low Q circuits are wide-band and high Q circuits are narrow-band. Lastly, Q factor is directly proportional to selectivity, as Q factor depends inversely on bandwidth. Taking into account $Q-$factor definition, a possible classification is made according to

- symmetrical full bridge for low Q load circuits (class D) and
- single bridge circuit for a high Q load circuit (class E).

High Q circuits can also use bridge inverter configuration, if desired, for higher throughput power. Energy transfer control complication is usually associated with the fact that the resistance of the load work-piece changes as it heats up and melts, since resistivity is temperature-dependant. However control is essentially independent of the voltage and current levels and it is related to the resonant frequency which is L and C dependant. Inverter bridge operation is near the load resonant frequency so that the output waveform is essentially sinusoidal. The resultant leading current can be used to self commutate thyristor converters which may be used in high power resonant circuits. This same capacitive load commutation effect is obtained for parallel resonant circuits with thyristor current source inverters operating just above resonance. The output power is controlled by controlling the converter output frequency.

2.5.1 $L-C$ resonant circuits

$L-C-R$ resonant circuits, whether parallel or series connected, are characterized by the load impedance being capacitive at low frequency and inductive at high frequency for the series circuit, and visa versa for the parallel case. The transition frequency between being capacitive and inductive is the resonant frequency ω_o, at which the $L-C-R$ load circuit appears purely resistive and maximum power is transferred to the load R. $L-C-R$ circuits are classified according to circuit quality factor Q, resonant frequency ω_o and band-with BW, for both parallel and series circuits. The characteristics for the parallel and series resonant circuits are related since every practical series $L-C-R$ circuit has a parallel equivalent, and vice versa. The parallel circuit can be series $R-L$ in parallel with the capacitor C. As shown in Figure 2.30 each resonant half cycle is characterized by

- the series resonant circuit is zero at maximum capacitor stored energy, and
- the parallel resonant circuit voltage is zero at maximum inductor stored energy.

The capacitor in a series resonant circuit must have an external path through which to release its stored energy. The parallel resonant circuit can release its stored inductive energy within its parallel circuit, without an external circuit. The stored energy can be internally resonant, transferring energy back and forth between the L and C, gradually dissipating in the circuit R.

2.5.2 Series resonant $L-C-R$ circuit

The series $L-C-R$ circuit current for a step input voltage V_s, with initial capacitor voltage v_c and series inductor current i_o is given by

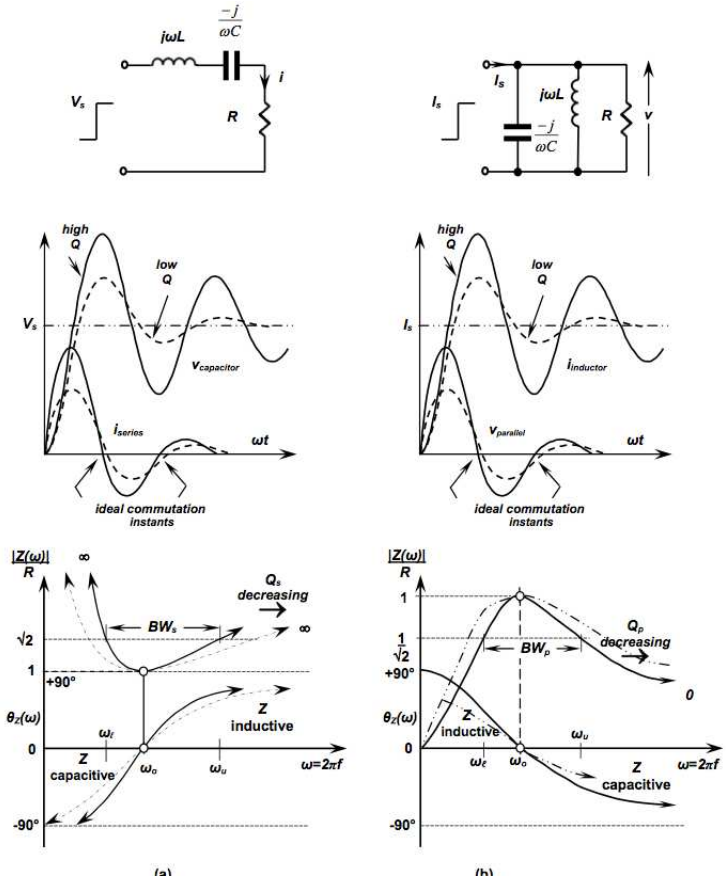

Fig. 2.30. Resonant circuits, step response, and frequency characteristics: (a) series $L-C-R$ circuit and (b) parallel $L-C-R$ circuit

$$i(\omega t) = \frac{V_s - v_o}{\omega L} e^{-\alpha t} \sin \omega t + i_o e^{-\alpha t} \frac{\omega_o}{\omega} \cos(\omega t + \phi), \tag{2.55}$$

where

$$\omega^2 = \omega_o^2(1-\xi^2) = \omega_o^2 - \alpha^2 \quad \omega_o = \frac{1}{\sqrt{LC}} \quad \alpha = \frac{R}{2L} \tag{2.56}$$

with

$$\xi = \frac{R}{2\omega_o L} \quad \text{and} \quad \tan\phi = \frac{\alpha}{\omega}. \tag{2.57}$$

The term ξ is the damping factor. The capacitor voltage is important because it specifies the energy retained in the $L-C-R$ circuit at the end of each half cycle. The expression for the voltage is reported below

$$v_c(\omega t) = V_s - (V_s - v_o)\,\frac{\omega_o}{\omega} e^{-\alpha t}\cos(\omega t - \phi) + \\ + \frac{i_o}{\omega C} e^{-\alpha t}\sin\omega t. \tag{2.58}$$

At the series circuit resonance frequency ω_o, the lowest possible circuit impedance results $Z = R$, hence it can be termed low-impedance resonance. The series circuit quality factor or figure of merit, Q_s is defined by

$$Q_s = \frac{\text{reactive power}}{\text{average power}} = \frac{Z_o}{R} \tag{2.59}$$

where the characteristic impedance is

$$Z_o = \sqrt{\frac{L}{C}}. \tag{2.60}$$

The series circuit half-power bandwidth BW_s is given by

$$BW_s = \frac{2\pi f_o}{Q_s}. \tag{2.61}$$

In the low Q case, to maintain and transfer sufficient energy to the load R, the circuit requires re-enforcement every half sine cycle, while with a high circuit Q, re-enforcement is only necessary once per sinusoidal cycle. Therefore for a high circuit Q, full bridge excitation is not necessary. The energy transferred to the load resistance R, per half cycle $\frac{1}{2f_r}$, is

$$W_{\frac{1}{2}} = \int_0^{\pi} i(\omega t)^2 R d\omega t. \tag{2.62}$$

The active power transferred to the load depends on the repetition rate of the excitation f_r, $P = W_{\frac{1}{2}} \times f_r$.

Parallel resonant $L - C - R$ circuit

The load for the parallel case is a parallel $L - C$ circuit, where the active load is represented by series resistance in the inductive path. For analysis, the series $L - R$ circuit is converted into its parallel $R - L$ equivalent circuit, thus forming the equivalent parallel $L - C - R$ circuit. A parallel resonant circuit is used in conjunction with a current source inverter, thus the parallel circuit is excited with a step input current. The voltage across a parallel $L - C - R$ circuit for a step input current I_s, with initial capacitor voltage v_o and initial inductor current i_o, is given by

$$v(\omega t) = v_c(\omega t) = \frac{I_s - i_o}{\omega C} e^{-\alpha t}\sin\omega t + \\ v_{co} e^{-\alpha t}\frac{\omega_o}{\omega}\cos(\omega t + \phi). \tag{2.63}$$

The inductor current is important since it specifies the tank circuit stored energy at the end of each half cycle

$$i_L(\omega t) = I_s - (I_s - i_o)\frac{\omega_o}{\omega}e^{-\alpha t}\cos(\omega t - \phi) + \\ + \frac{v_{co}}{\omega L}e^{-\alpha t}\sin(\omega t) \tag{2.64}$$

where

$$\alpha = \frac{1}{2CR}. \tag{2.65}$$

The parallel circuit Q for a parallel resonant circuit is

$$Q_p = \omega_o RC = \frac{1}{Q_s} \tag{2.66}$$

where ω_o is above defined and the triplet (L, C, R) refers to the parallel circuit values. The half-power bandwidth BW_p is given by $BW_p = \frac{\omega_o}{Q_p}$. At the parallel circuit resonance frequency ω_o, the highest possible circuit impedance results, i.e. $Z = R$, hence it can be termed high-impedance resonance. The energy transferred to the load resistance R, per half cycle $\frac{1}{2f_r}$, is

$$W_{\frac{1}{2}} = \int_0^{\pi} v(\omega t)^2/R d\omega t. \tag{2.67}$$

The active power to the load depends on the repetition rate of the excitation f_r.

Series-resonant voltage-source inverters

Series resonant circuits use a voltage source inverter (class D series). If the load Q is high, then the resonance of energy from the energy source V_s need only be re-enforced every second half-cycle, thereby simplifying converter and control requirements. A high Q circuit is characterized by successive half-cycle capacitor voltage peak magnitudes being of similar magnitude, that is the decay rate is

$$\frac{v_c}{v_{c_{n+1}}} = e^{\frac{2\pi}{Q}} \approx 1 \text{ for } Q \gg 1. \tag{2.68}$$

Without free-wheel diodes, the switches have to block high reverse voltages due to the energy stored by the capacitor. MOSFET and IGBTs require series diodes to achieve the reverse voltage blocking requirements. In high power resonant applications, the reverse blocking abilities of the GTO and GCT make them ideal converter switches. Better load resonant control is obtained if free-wheel diodes are not used.

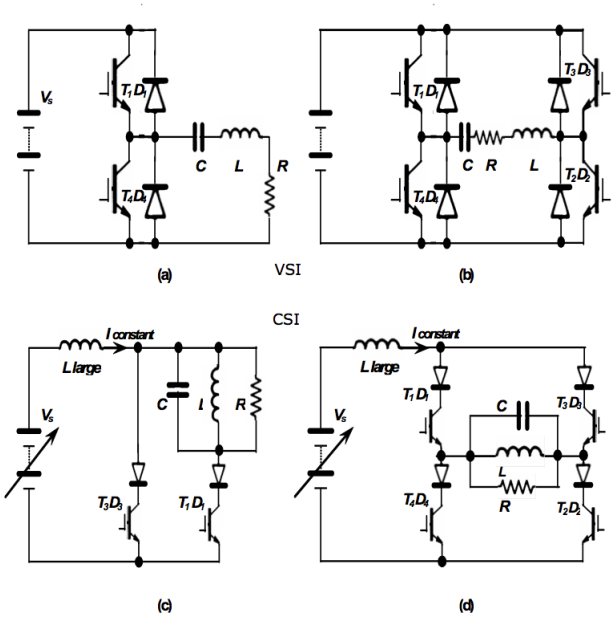

Fig. 2.31. Resonant circuits: (a) series $L-C-R$ with high Q; (b) series $L-C-R$ with low Q; (c) parallel $L-C-R$ with high Q and (d) parallel $L-C-R$ with low Q

Series-resonant inverter. The single leg case

Operations of the series load single-leg circuit in Figure 2.31 depend on the timing of the switches.

If the converter is operated at a frequency above resonance (effected by commutating the switches before the end of an oscillation cycle), the inductor reactance dominates and the load appears inductive. Therefore turn-on occurs at a low voltage (hence low switch turn-on loss and no need for fast recovery diodes). Operation and switch timing are as follows: the switch $T1$ is turned on while its anti-parallel diode is conducting and the current in the diode reaches zero, and begins to oscillate through the switch $T1$. The capacitor charges to a maximum voltage and, before the current reverses, the switch $T1$ is hard turned off. The current is diverted though diode $D4$. $T4$ is turned on which allows the oscillation to reverse. Before the current in $T4$ reaches zero, it is turned off and current is diverted to diode $D1$, which returns energy to the supply. The resonant cycle is repeated when $T1$ is turned on before the current in diode $D1$ reaches zero and the process continues. By operating the converter at a frequency below resonance (effectively by delaying switch turn-on until after the end of an oscillation cycle), the capacitor reactance dominates and the load appears capacitive. The load current leads the voltage. Switch output capacitance charging and discharges ($\frac{1}{2}CV^2$). Operation and

switch timing are as follows: the diode $D4$ is conducting when switch $T1$ is turned on, which provides a step input voltage V_s to the series $L-C-R$ load circuit, and the current continues to oscillate. The capacitor charges to a maximum voltage and the current reverses through $D1$, feeding energy back into the supply. $T1$ is then turned off with zero current. The switch $T4$ is turned on, commutating $D1$, and the current oscillates through the zero volt loop created through $T4$ and the load. The oscillation current reverses through diode $D4$, when $T4$ is turned off with zero current. $T1$ is turned on and the process continues. Without the free-wheel diodes the half oscillation cycles are controlled completely by the switches. On the other hand, with free-wheel diodes, the timing of switch turn-on and turn-off is determined by the load current zeros, is maximum energy transfer to the load is to be gained. For a square wave input voltage of magnitude $2\frac{V_s}{\pi}$ produces the dominant load current component, since higher frequency components are attenuated by second order $L-C$ filtering action. That is, the resonant circuit excitation voltage is $|V_i| = \frac{2V_s}{\pi}$. The series circuit steady-state current at resonance for the single-leg half-bridge can be approximated by assuming $\omega_o \approx \omega$, such that in Eq. (2.55) $i_o = 0$:

$$i(\omega t) = \frac{e^{-\alpha t}}{1 - e^{-\frac{\alpha\pi}{\omega}}} \frac{V_s}{\omega L} \sin \omega t \tag{2.69}$$

which is valid for $0 \leq \omega t \leq \pi$ and for the $+V_s$ loop (through T_1) and zero voltage loop (through T_4) modes for cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle. In steady-state the successive capacitor voltage absolute maxima are

$$\hat{V}_c = V_s \frac{1}{1 - e^{-\alpha\frac{\pi}{\omega}}} \quad \text{and } \tilde{V}_c = -V_s \frac{e^{-\alpha\frac{\pi}{\omega}}}{1 - e^{-\alpha\frac{\pi}{\omega}}}. \tag{2.70}$$

The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = \frac{1 + e^{-\alpha\frac{\pi}{\omega}}}{1 - e^{-\alpha\frac{\pi}{\omega}}} \times V_s. \tag{2.71}$$

The energy transferred to the load R, per half sine cycle (per current pulse) is

$$W = \frac{1}{2} C V_s^2 coth\left(\frac{\alpha\pi}{2\omega}\right). \tag{2.72}$$

From the series ac circuit, the voltage across the resistor, v_R, at a given frequency ω, is given by

$$V_r(\omega) = V_i \frac{R}{R + \jmath\left(\omega L - \frac{1}{\omega C}\right)} \tag{2.73}$$

and the magnitude of the resistor voltage is therefore

$$v_R(\omega) = V_i \frac{1}{\sqrt{1 + Q^2\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)^2}}. \tag{2.74}$$

Series-resonant inverter. The H-bridge case

When the load Q is not high, the capacitor voltage between successive absolute peaks decays significantly, leaving insufficient energy to maintain high efficiency energy transfer to the load R. In such cases the resonant circuit is re-enforced whit energy from the dc source V_s every half-resonant cycle, by using a full H-bridge. Operation is characterized by turning on switches T_1 and T_2 to provide energy from the source during one half of the cycle, then having turned T_1 and T_2 off, T_3 and T_4 are turned on for the second resonant half cycle. Energy is again drawn from the supply V_s and, when the current reaches zero, T_3 and T_4 are turned off. Without bridge free-wheel diodes, the switches support high reverse bias voltages, but the switches control the start of each oscillation half cycle. With free-wheel diodes the oscillations can continue independent of the switch states. The diodes return energy to the supply, hence reducing the energy transferred to the load. Correct timing of the switches minimises currents in the free-wheel diodes, hence minimizes the energy needlessly being returned to the supply. Energy to the load is maximised. As with the single-leg half-bridge, the switches can be used to control the effective load power factor. By advancing turn-off to before the switch current reaches zero, the load can appear to be inductive, while delaying switch turn-on produces a capacitive load effect. The series circuit steady-state current at resonance for the symmetrical H-bridge can be approximated by assuming $\omega_o \approx \omega$ such that in Eq.(2.73), $i_o = 0$:

$$i(\omega t) = 2\frac{e^{-\alpha t}}{1 - e^{-\frac{\alpha\pi}{\omega}}}\frac{V_s}{\omega L}\sin\omega t, \tag{2.75}$$

which is valid for the $\pm V_s$ voltage loops of cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle. In steady-state the capacitor voltage absolute maxima are $\hat{V}_c = -\tilde{V}_c$. The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = 2 \times \frac{1 + e^{-\frac{\alpha\pi}{\omega}}}{1 - e^{-\frac{\alpha\pi}{\omega}}}V_s. \tag{2.76}$$

The energy transferred to the load R per half sine cycle (per current pulse) is $W = 2CV_s^2 coth(\alpha\frac{\pi}{2\omega})$. Notice that the power delivered to the load is increased by a factor of four. From the series ac circuit, the voltage across the resistor v_R at a given frequency ω is given by

$$v_R(\omega) = V_i\frac{R}{R + \jmath\left(\omega L - \frac{1}{\omega C}\right)}. \tag{2.77}$$

The magnitude of the resistor voltage is therefore

$$v_R(\omega) = V_i\frac{1}{\sqrt{1 + Q^2\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)^2}}. \tag{2.78}$$

If the input voltage V_i is expressed as a Fourier series then the resistor current can be derived in terms of the summation of all the harmonic component according to

$$\sum_{n=1}^{\infty} i_R(n\omega) = \sum_{n=1}^{\infty} \frac{v_R(n\omega)}{R}. \tag{2.79}$$

For a square wave input voltage, $\pm V_s$, of frequency $\omega \approx \omega_o$, the input voltage fundamental of magnitude $4\frac{V_s}{\pi}$ produces the dominant load current component, since higher frequency components are attenuated by second order $L-C$ filtering action. That is $|V_i| = 4\frac{V_s}{\pi}$.

2.5.3 Parallel-resonant CSI inverters

Parallel resonant circuits use a current source inverter (class D, parallel). If the load Q is high, the resonance needs only to be re-enforced every second half cycle, thereby simplifying conversion and control requirements. A common feature of parallel resonant circuits fed from a current source is that commutation of the switches involves overlap where the output of the current source can be briefly shorted.

Single inverter leg case

In a single-leg half-bridge converter for high Q parallel load circuits, the energy is provided from the constant current source every second half cycle by turning on switch T_1 (see Figure 2.31(c)). When T_1 is turned on (and T_3 is then turned off) the voltage across the $L-C-R$ circuit resonates from zero to a maximum and back to zero volts. The energy in the inductor reaches a maximum at each zero voltage instant. T_3 is turned on (at zero volts) to divert current from T_1, which is then turned off with zero terminal voltage. The energy in the load inductor resonates within the load circuit, with the load in an open circuit state, since T_1 is off. The sequence continues when the load voltage resonates back to zero. The parallel circuit steady-state voltage at resonance for the single-leg half-bridge can be approximated by assuming $\omega_0 \approx \omega$ as

$$v(\omega t) = \frac{e^{-\alpha t}}{1 - e^{-\frac{\alpha\pi}{\omega}}} \frac{I_s}{\omega C} \sin(\omega t). \tag{2.80}$$

In steady-state the successive inductor current absolute maxima are

$$\hat{I}_L = I_s \frac{1}{1 - e^{-\frac{\alpha\pi}{\omega}}} \quad \text{and} \quad \tilde{I}_L = I_s \frac{-e^{-\frac{\alpha\pi}{\omega}}}{1 - e^{-\frac{\alpha\pi}{\omega}}}. \tag{2.81}$$

The energy transferred to the load R, per half sine cycle (per voltage pulse) is

$$W = \frac{1}{2} L I_s^2 coth\left(\frac{\alpha\pi}{2\omega}\right). \tag{2.82}$$

To drive a parallel circuit from a voltage source inverter leg, the resonant circuit inductance is series connected to the parallel $R-C$ circuit. For a voltage source inverter leg, from the series plus parallel ac circuit, the voltage across the resistor, v_R, at a given frequency ω, is given by

$$v_R(\omega) = V_i \frac{1}{1-\left(\frac{\omega}{\omega_o}\right)^2 + \jmath\frac{1}{Q_p}\frac{\omega}{\omega_o}}. \tag{2.83}$$

The magnitude of the resistor voltage is therefore

$$v_R(\omega) = V_i \frac{1}{\sqrt{\left[1-\left(\frac{\omega}{\omega_o}\right)^2\right]^2 + \frac{1}{Q_p^2}\left(\frac{\omega}{\omega_o}\right)^2}} \tag{2.84}$$

The H-bridge CSI inverter case

If the load Q is low, or maximum energy transfer to the load is required, the full bridge converter shown in Figure 2.31 is used. Operation involves T_1 and T_2 directing the constant source current to the load and when the load voltage falls to zero, T_3 and T_4 are turned on (and T_1 and T_2 then turned off). Overlapping the switching sequence ensures a path always exists for the source current. At the next half sinusoidal cycle voltage zero, T_1 and T_2 are turned on and then T_3 and T_4 are turned off. The parallel circuit steady-state voltage for the symmetrical H- bridge can be approximated by assuming $\omega_o \approx \omega$ such that:

$$v(\omega t) = 2\frac{e^{-\alpha t}}{1-e^{-\frac{\alpha\pi}{\omega}}}\frac{I_s}{\omega C} sin(\omega t) \tag{2.85}$$

which is valid for both the loops of cycle operation, provided the time reference is moved to the beginning of each half-cycle. In steady-state the successive inductor current absolute maxima are $\hat{I}_L = -\tilde{I}_L$. The energy transferred to the load R, per half sine cycle (per voltage pulse) is $W = 2LI_s^2 coth\left(\frac{\alpha\pi}{2\omega}\right)$. The full bridge delivers four times more power to the load than the single-leg half-bridge circuit. Similarly, the load power and power factor can be controlled by operating above or below the resonant frequency, by delaying or advancing the appropriate switching instances.

2.5.4 CSI series resonant inverter

The single switch inverter in Figure 2.32 is applicable to high Q load circuits such that the output is essentially sinusoidal, with zero average current. Based on the operating mechanisms, a sinusoidal current implies the switch has a 50% duty cycle. The switch turns on and off at zero volts so switch losses are low, so the operating frequency can be high. The input inductor L_{large} in conjunction with the input voltage source, during steady-state operation,

act as a current source input I_s, for the resonant circuit, such that $V_s I_s$ is equal to the power delivered to the load R. When the switch $T1$ is turned on, with zero terminal voltage, it conducts both the constant current I_s and the current i_o resonating in the output circuit. The resonating load current builds up. The switch T_1 which is in parallel with C_s, is turned off. Current from the switch is diverted to C_s, which charges from an initial voltage of zero. C_s thus forms a turn-off snubber in parallel with T_1. The charge on C_s eventually resonates back to zero at which instant the switch is turned on, again, with zero turn-on loss. The resonant frequency is $\omega_o = \frac{1}{\sqrt{L_o C_o}}$ and because of the high Q, a small change in the switching frequency significantly decreases the output current, hence output voltage. As with any current source inverter, the peak switch voltage is in excess of V_s. Since the current is sinusoidal, the average load voltage and inductor voltage are zero. Therefore the average voltage across C_o and C_s is the supply voltage V_s. If the load conditions change and the switch duty cycle is varied from $\delta = 1/2$ circuit voltages increase and capacitor C_s voltage discharges before the circuit current reaches zero. The capacitor and switch are bypassed with current flowing through the diode $D1$. This diode prevents the switch from experiencing a negative voltage and the capacitor from charging negatively. Although such resonant converters offer features such as low switching losses and low radiated EMI, optimal control and performance are difficult to maintain and extremely high circuit voltages occur at low duty cycles.

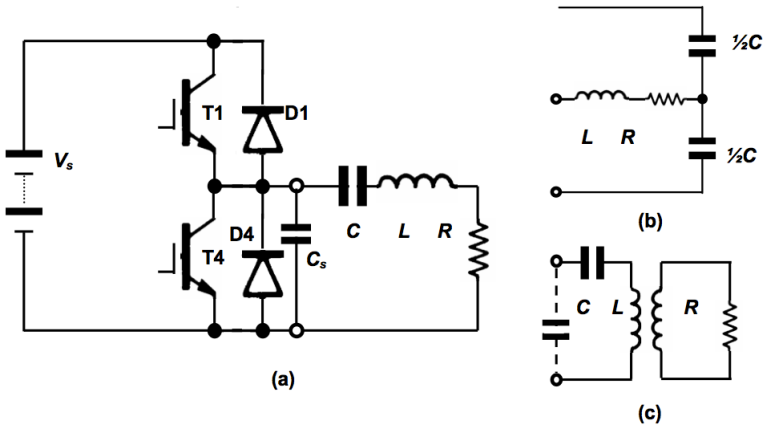

Fig. 2.32. Different resonant load arrangements: (a) switch turn-off snubber capacitor C_s; (b) split capacitor; and (c) series coupled circuit for induction heating

2.6 Multi-level voltage-source inverters

The conventional three-phase, six-switch voltage-source inverter is shown in Figure 2.33. Each of the three inverter legs has an output which can provide one of two voltage levels, V_s, when the upper switch (or diode) is on, and 0 when the lower switch (or diode) conducts. The quality of the output waveform is determined by the resolution and switching frequency of the PWM technique used. A multilevel inverter (directly or indirectly) divides the dc power, so that the output of the leg can be more than two discrete levels.

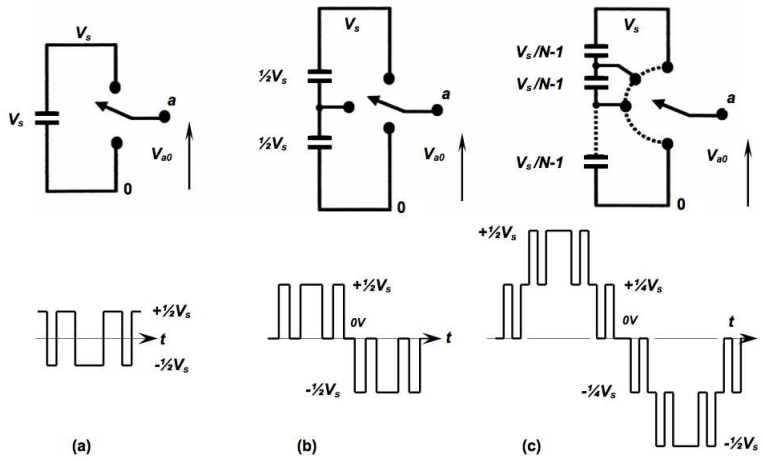

Fig. 2.33. One phase leg of a VSI bridge inverter with (a) two levels; (b) three levels; and (c) N-levels

In this way, the output quality is improved because both pulse width modulation and amplitude modulation can be used. The output pulse is made from than two series connected-clamped switches so the total dc voltage soure can be regarded as the sum of the voltage rating of the individual switches. Very high output voltages can be achieved, where each device does not experience a voltage in excess of its individual rating. A multilevel inverter allows higher output voltages with low distortion (due to the use of both pulse width and amplitude modulation) and reduced output dv/dt.

There are three main types of multilevel converters

- Diode clamped,
- Flying capacitor, and
- Cascaded H-bridge.

2.6.1 Diode clamped multilevel inverter

Figure 2.33 shows the basic principle of the diode clamped (or neutral point clamped, NPC) multilevel inverter, where only one dc supply, V_s, is used and N is the number levels present in the output voltage between the leg output and the inverter negative terminal. The capacitors split the dc source voltage into a number of lower voltage levels each of which is necessary for any number of output phase legs. The number of levels in the line-to-line voltage waveform will be $k = 2N - 1$ while the number of levels in the line to load neutral of a star (wye) load will be $p = 2k - 1$. The number of capacitors required, independent of the number of phase, is $N_{cap} = N - 1$ while the number of clamping diodes per phase is $D_{clamp} = 2(N - 1)$. The number of possible switch states is $n_{states} = N^{states}$ and the number of switches in each leg is $S_n = 2(N - 1)$. Some of the clamping diodes experience voltages in excess of that experienced by the main switches. Series connection of some of the clamping diodes avoids this limitation, but at the expense of increasing the number of clamping diodes from $2 \times (N - 1)$ to $(N - 1) \times (N - 2)$ per phase. Therefore depending on the diode position in the structure, two diodes have blocking requirements of

$$V_{RB} = \frac{N - 1 - k}{N - 1} V_s \tag{2.86}$$

where $1 \leq k \leq N - 2$. These diodes require series connection of diodes, if all devices in the structure are to support $V_s/(N - 1)$. For $N > 2$, capacitor imbalance occurs. The general output voltage, to the centre of the capacitor string is given by

$$V_{an} = \frac{V_s}{N - 1}(T_1 + T_2 + \ldots + T_{N-1} - \frac{N - 1}{2}) \tag{2.87}$$

2.6.2 Flying capacitor multilevel inverter

On leg of a fly-capacitor clamped five-level voltage source inverter is shown in Figure 2.34, where capacitors are used to clamp the switch voltages to $\frac{V_s}{4}$. The available output voltages are $\pm\frac{V_s}{2}$, $\pm\frac{V_s}{4}$, and 0, where the output is connected to the dc link (V_s and 0) indirectly via capacitors. In general, switches T_n and T_{n+1} connect to capacitor C_n. The configuration offers more usable switch states than the clamped diode inverter and this redundancy allows better flexible control of capacitor voltages. The number of levels in the line-to-line voltage waveform will be $k = 2N - 1$ while the number of levels in the line to load neutral of a star (wye) load will be $p = 2k - 1$. The number of capacitors required, which is dependent of the number of phase, is for each phase $N_{cap} = (N-1)(N-2)/2$. The number of possible switch states is $n_{states} = N^{phases}$ and the number of switches in each leg is $S_n = 2(N-1)$. A feature of the flying capacitor multilevel inverter is its ride through capability

due to the large capacitance used. On the other hand, the capacitors have a high voltage rating and suffer from high current ripple, since they conduct the full load current when connected into an active output voltage state. Capacitor initial charging is also problematic.

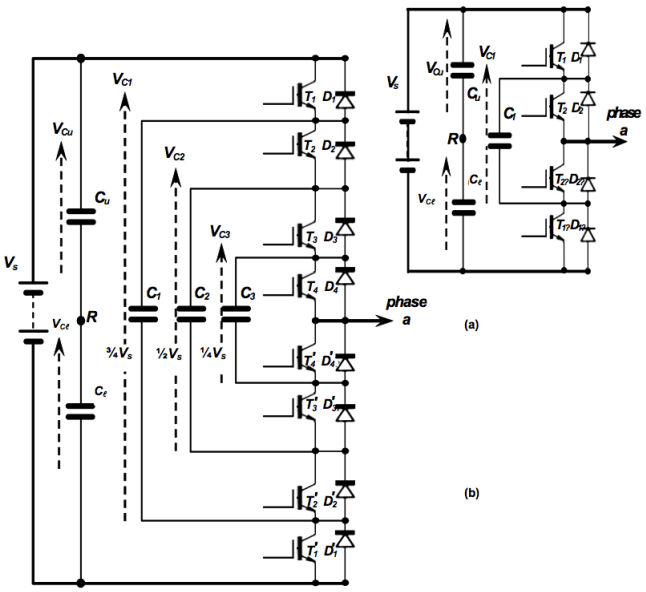

Fig. 2.34. One leg of a voltage-source: (a) three-level and (b) five-level, flying capacitor clamped bridge inverter.

Cascaded H-bridge multilevel inverter

The N-level cascade H-bridge multilevel inverter comprises $\frac{(N-1)}{2}$ series connected single-phase H-bridges per phase, for which each H-bridge has its own isolated dc voltage source. For each bridge, as shown in Table 2.35, three output voltages are possible, $\pm V_s$, and zero, giving a total number of states of $3^{\frac{1}{2}(N-1)}$, where N is odd. Figure 2.36 shows one phase of a seven-level cascaded H-bridge inverter.

The cascaded H-bridge multilevel inverter is based on multiple two-level inverter outputs (each H-bridge) with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches. Its main limitation lies in the need for isolated power sources for each H-bridge and for each phase, although for VA compensation. Its modular structure of identical H-bridges is a positive design feature. The number of levels in the line-to-line voltage waveform will be

V_ℓ	On switches	Bidirectional current paths	
		$+ i_L$	$- i_L$
V_s	T_2 T_3	T_2 T_3	D_2 D_3
0	none	D_4 D_1	D_2 D_3
$-V_s$	T_1 T_4	T_1 T_4	D_2 D_3

Fig. 2.35. Three output states of H-bridges and their current paths.

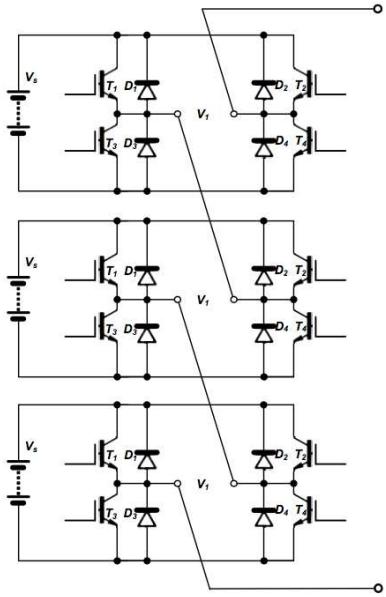

Fig. 2.36. One leg of a voltage-source, seven-level, cascaded H-bridge inverter.

$k = 2N - 1$ while the number of levels in the line to load neutral of a star (wye) load will be $p = 2k - 1$. The number of capacitors or isolated supplies required per phase is $N_{cap} = (N-1)/2$ and the number of switches in each leg is $S_n = 2(N-1)$. The diode clamped inverter requires many clamping diodes, the flying capacitor inverter requires many independent capacitors while the cascaded inventer requires many isolated dc voltage power supplies

2.6.3 Emerging Multilevel inverter topologies

Among the emerging multilevel topologies, a particular attention has been given to the mixed-level multilevel cells. For high-voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascaded inverter [40, 61, 59, 84, 85, 94, 95]. The reason for doing so is to reduce the amount of separate dc source.

The configuration can be considered as having mixed-level hybrid multilevel cells because it embeds multilevel cells as the building block of the cascaded inverter. It is obvious that a diode-clamped inverter can replace the capacitor-clamped inverter to be a mixed-level hybrid multilevel cell. In previous descriptions, the voltage levels of the cascade inverter cells equal each other. However, it is possible to have different voltage levels among the cells, and the circuit can be called as asymmetric hybrid multilevel inverter. Depending on the availability of dc sources, the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage, and thus reduces the harmonic contents with less cascaded cells required. Even with the same voltage level among them, it is also possible to use high-frequency PWM for one cell, while the other switches at a lower rate. Another interesting class of innovative topologies is represented by the soft-switched multilevel inverters (see [54, 81] and the reference therein). There are numerous ways of implementing soft-switching methods to reduce the switching loss and to increase efficiency for different multilevel inverters. For the cascaded inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not at all different from that of conventional two- level inverters. For capacitor- or diode-clamped inverters, the choices of soft-switching circuit can be found with different circuit combinations. Although zero-current switching is possible, most literatures proposed zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations. Figure 2.37 shows an example of combining the ARCP and coupled-inductor ZVT techniques for a capacitor-clamped three- level inverter. The auxiliary switches S_{x2}, S_{x3}, D_{x2} and D_{x3} are used to assist the inner main switches S_2 and S_3 to achieve soft switching. With L_{r23} as the coupled inductor, the bridge-type circuit formed by S_{x2}, S_{x3}, S_2 and S_3 forms a two-level coupled-inductor ZVT. The basic principle of a two-level ZVT can be found in literature. For the outer main switches, the soft switching relies on S_1 and S_4, S_{x1}, S_{x4}, D_{x1}, D_{x4} coupled inductor L_{r14} and split-capacitor pair C_2 to form an ARCP type soft-switching inverter.

2.6.4 Control and modulation strategies

The modulation methods used in multilevel inverters can be classified according to switching frequency. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the SVM strategy, which has been used in three-level inverters. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representa-

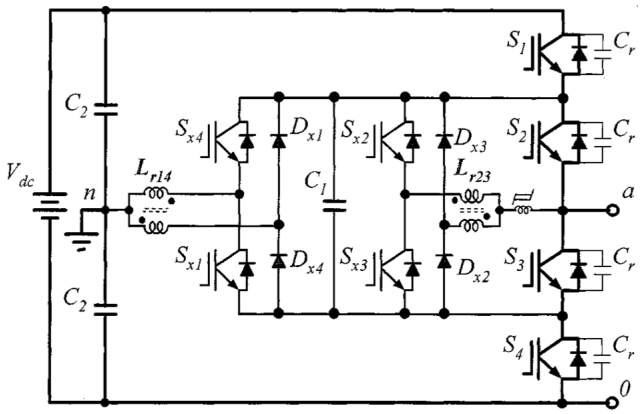

Fig. 2.37. Zero-voltage-switching capacitor-clamped inverter circuit.

tives of this family are the multilevel selective harmonic elimination, and the space-vector control (SVC).

Multilevel SPWM

Several multi-carrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. A number of N_c-cascaded cells in one phase with their carriers shifted by an angle $\theta_c = \frac{2\pi}{N_c}$ produce a load voltage with the smallest distortion. The smallest distortion is obtained when the carriers are shifted by an angle of $\theta_C = \frac{2}{3}\pi$. A very common practice in industrial applications for the multilevel inverter is the injection of a third harmonic in each cell to increase the output voltage. Another advantageous feature of multilevels SWPM is that the effective switching frequency of the load voltage is N_c times the switching frequency of each cell, as determined by its carrier signal. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses.

SVM

The SVM technique can be easily extended to all multilevel inverters. Figure 2.38 shows space vectors for the traditional two-,three-, and five-level inverters. These vector diagrams are universal regardless of the type of multilevel inverter. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle (T_j, T_{j+1}, and T_{j+2}) for each vector

$$V^* = \frac{1}{T}\left(T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2}\right). \tag{2.88}$$

Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. As the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically. Some authors have used decomposition of the five-level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify control. Additionally, a simple space-vector selection method was introduced without duty-cycle computation of the adjacent three vectors.

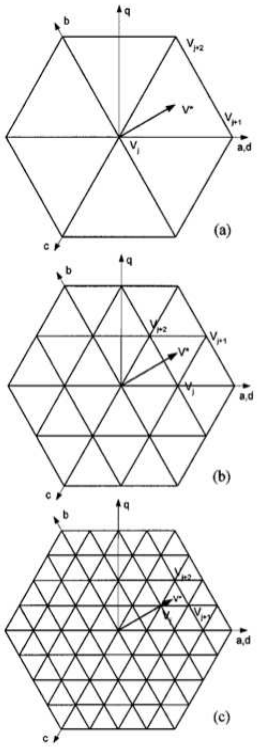

Fig. 2.38. Space-vector diagram: (a) two-level (b) three-level and (c) five-level inverter

Selective Harmonic Elimination

By considering a generalized quarter-wave symmetric stepped-voltage waveform synthesized by a $(2m+1)$-level inverter, where m is the number of switching angles, the amplitude of any odd n^{th} Fourier harmonic of the stepped

waveform can be expressed as follows whereas the amplitudes of all even harmonics are zero,

$$h_n = \frac{4}{n\pi} \sum_{k=1}^{m} V_k \cos(n\alpha_k) \tag{2.89}$$

where V_k is the k^{th} level of dc voltage, n is an odd harmonic order, m is the number of switching angles and α_k is the k^{th} switching angle. The switching angles must satisfy the following condition

$$\alpha_1 < \alpha_2 < \ldots < \alpha_m < \frac{\pi}{2}. \tag{2.90}$$

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $m-1$ harmonic contents can be removed form the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different-level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. According to Eq. (2.89), to keep the number of eliminated harmonics at a constant level, all switching angles must be less than $\frac{\pi}{2}$. However, if the switching angles do no satisfy the condition, this scheme no longer exists. As a result, this modulation strategy basically provides a narrow range of modulation index, which is its main disadvantage. At modulation indexes lower than 0.5, if this scheme is still applied, the allowable harmonic components to be eliminated will reduce from 2 to 1. The total harmonic distortion increases correspondingly. In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selected harmonic modulation scheme was proposed. In general, a stepped waveform, which comprises m switching angles, can be divided into m modulation index levels. By using this technique, low switching frequencies with minimized harmonics in the output waveforms can be achieved with wide modulation indexes. Through mathematical manipulation, a generalized harmonic expression for miltilevel stepped voltage has been derived and it is expressed as the following:

$$h_n = \frac{4}{n\pi} \left[V_1 \cos(n\alpha_1) \pm V_2 \cos(n\alpha_2) \pm \ldots \pm V_m \cos(n\alpha_m) \right]. \tag{2.91}$$

In this expression, the positive sign implies the rising edge, and the negative sign implies the falling edge.

SVC

A conceptually different control method for multilevel inverters, based on the space-vector theory, has been introduced. This control strategy, called SVC, works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as it is the principle of SVM. The main idea in SVC is to deliver to the load a voltage vector that

minimizes the space error or distance to the reference vector v_{ref}. The high density of vectors produced by the $m-$level inverter will generate only small errors in relation to the reference vector; it is, therefore, unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference. This method is simple and attractive for high number of levels. As the number of levels decreases, the error in terms of the generated vectors with respect to the reference will be higher; this will increases the load current ripple.

Capacitor Balancing Techniques

It has been demonstrated that the diode-clamped multilevel inverter could not have balanced voltages for real power conversion without sacrificing output voltage performance. Thus, it has been proposed that the diode-clamped multilevel inverter be applied to reactive and harmonic compensation without voltage balancing problem. The voltage unbalance problem could be solved by using a back-to-back rectifier/inverter system and proper voltage balancing control. For the capacitor-clamped multilevel inverter, voltage balancing is relatively complicated. It has been shown theoretically that the capacitor-clamped inverter cannot have self-balanced voltage when applied to power conversion in which no real power is involved, such as reactive power compensation. However, since each phase leg has its own floating capacitors that handle the phase current, the voltage balancing and ripple become troublesome. The cascade multilevel inverter was first introduced for motor driver applications, in which an isolated and separate dc source is needed for each H-bridge unit. Additional work further demonstrated that the cascaded inverter is suitable for universal power conditioning of power systems, especially for medium-voltage systems. The inverter provides lower costs, higher performances, less electromagnetic interference (EMI), and higher efficiency than the traditional PWM inverter for power line conditioning applications, both series and parallel compensation. Although the cascaded inverter has an inherent self-balancing characteristic, because of the circuit component losses and limited controller resolution, a slight voltage imbalance can occur. A simple control scheme, which ensures dc voltage balance, has been proposed for reactive and harmonic compensation.

2.7 Reversible dc link converters

Power inversion by phase angle control is attained with a fully controlled single-phase converters. Power regeneration is also possible with the fully controlled three-phase converters. If a fully controlled converter supplies a dc machine, two-quadrant control is possible motoring in one direction of rotation and generating in the other direction. Power regeneration into the

supply is achieved by reversing the dc output voltage by controlling the converter phase delay angle. The converter current is uni-directional, that is, the converter output current cannot reverse.

2.7.1 Simultaneous control

Simultaneous converter control, also called circulating current control, works with both converters always in operation which gives a faster dynamic response than when the converters are used mutually exclusively. To avoid supply short circuits requires that the output voltage of both converters be the same in order to minimise circulating currents that is that both converters operate with firing angles that sum to π. Each converter produces the opposite polarity output voltage, which is cancelled by reversing the relative output convections. Under such conditions the load current can be maintained continuous. To minimize any circulating current due to ripple voltage produced by instantaneous voltage differences between the two converters, inductance is usually inserted between each converter and the dc machine load. Adversely the cost and weight are increased and the supply power factor and drive efficiency are decreased, compared to that obtained with independently controlled converters.

2.7.2 Inverter regeneration

The bridge free-wheel diodes of a three-phase inverter restrict the dc link voltage from reversing. The dual or double converter circuit will allow inversion with a three-phase voltage source inverter. One converter rectifies, the other converter inverts, functioning as a self-commutated inverter, transferring power from the dc link to the ac supply. Complete 4-quadrant control of the three-phase ac machine on the inverter is achieved in conjunction with control of the dc to ac inverter. That is, motor reversal is achieved by effectively interchanging the pwm control signals associated with two phases. The real power flow back into the ac supply is controlled by the converter phase delay angle, while the reactive power flow is controlled by the voltage magnitude. The angle and voltage are not independent. In the case of a PWM controlled inverter fed ac machine, the ac to dc converter can be uncontrolled. The use of self-commutated switches (rather than mains commutated converter thyristors) offers the possibility to minimize the input current distortion and to reduce the inductor size improving the dynamic current response. The switch series diodes are essential since the shown IGBTs have no useable reverse blocking capability. The use of reverse blocking GCTs avoids the need for the series blocking diodes, which reduces the on-state voltage losses but increases gate rive complexity and power rating. Series connection of devices is necessary above a few kV, and above $1MVA$ the GCT dominates.

3

A new DC/AC conversion system

3.1 Introduction

The impressive demand of alternative energy solutions influences the search directions in new power electronics area in order to find more efficient technologies. The statistics of the International Energy Agency allow to figure out the dimensions of the present-day energy Market. At the period between 2002 and 2003, the total installed power of photovoltaic systems in the IEA countries increases with 35 % and reaches $1.809MW$. Simultaneously, centralized photovoltaic energy networks are also implemented, for example, in Germany and USA with power up to $5MW$. It is not only a solar revolution but, more in general, all the renewable energy source systems are becoming more and more attractive. Towards 1994 the total installed power in wind turbines, in fact, is about $3500MW$. According to data from Global Wind Energy Council, the total power has increased from $7976MW$ in 2004, and nowadays it is $47317MW$. Countries as Germany, Spanish, USA, Denmark, the Netherlands, India and so on, have the major contribution to the increase. The wind energy is the fastest developing source of energy and the development in wind energy usage is in two directions: the first is in small wind installations for an individual use and the second is in creation of centralized installations of turbines - wind generation farms with a high power. Sea areas closed to the main land are used for the centralized installations. Wind generators that operate without a change of the speed of their turbine have found a wide implementation because of their simplicity. These generators are made using an asynchronous generator with a short-circuit rotor and is directly connected to the electrical network using a transformer. In 2008 the ideas of distributed electrical energy generation and ecological use of energy sources unified the researchers in Future Renewable Electric Energy Delivery and Management (FREDM) System Center. The center research program purposes are orientated towards Energy Internet. Different trends in the study and practical applications of the use of water energy exists too.

It is not surprising, therefore, the absolutely central role that power electronics systems area is nowadays acquiring . Basically, the power electronics core area is the creation of power electronic converters associated with conversion of electrical energy using electronic means. Cumulative electronic means covers the following groups:

- **Power schema made on the basis of power electronic devices (switches)**: Diodes, thyristors (silicon controller rectifier -SCR), insulated gate bipolar transistors (IGBT), metal-oxide-semiconductor field-effect transistors (MOSFET), etc.
- **Control and regulation system made on the basis of analogue and digital electronic elements**: Analogue and digital integral circuits, microprocessors, micro-controllers, digital signal processors, etc. Additionally, software is included here, if a processor is applied in the control system.
- **Sensors used to monitor the basic variables**: Current, voltage, power, temperature, etc.

In this chapter the target of the presented DC/AC conversion system is twofold: the proposed signal requires a switching frequency that is equal to $3f_{res}$ where f_{res} is the desired output frequency leading to much less switching losses and in the meanwhile the generated waveform presents a total harmonic distortion level that is less than 1 unlike the standard results. Switching losses optimization is a sensible task in operation mode where it is required high efficiency at light load. Many devices may show significant degradation in energy capture capability when using PWM converters of low efficiency at light load. In [2], an analytical averaged equivalent circuit model is derived revealing how dominant loss mechanisms vary with power converter operating point in a PWM converter. Higher switching frequency reduces the volume of passive elements, but in the same time increases losses dropping the efficiency. If losses vary linearly with output power, then the converter efficiency is independent of load. Conduction losses of typical PWM inverters vary linearly with or as the square of output power, and hence cannot explain the observed efficiency degradation at light load. Unlike conduction ones, switching losses typically exhibit a less-than-linear dependence on output power. Hence, reducing the output power does not proportionately reduce the switching loss. The second property of the proposed design is the possible total harmonic distortion values associated with the pre-filtered generated waveform. It has been remarked how total harmonic distortion index leads to power losses: high values for the THD mean high power losses as, for example, dissipated heat. The proposed approach permits to obtain pre-filtered THD values that are less than the unity. This means a more convenient filtering action and in the meanwhile less filtering power losses with respect to standard technique,like sinusoidal PWM systems, that provide sinusoidal waveform with a THD at least equal to 1.

3.2 Switching loss mechanisms

Switching loss can be resolved into components induced by the diode reverse-recovery mechanism, the switch (in the following IGBT switches are considered due their practical relevance), current-tailing phenomena, the switch turn-on time, and the output capacitances of the switches and diodes [2]. Each source causes a energy loss that is a function of the semiconductor on-state current and off-state voltage. By defining W_D as the energy loss inducted in IGBT by diode reverse-recovery, W_{tail} the energy loss during IGBT turn-off transistion, owing to current tail, W_r the energy loss during IGBT turn-on transition, in the rise of collector current, and W_C the energy loss induced in IGBT by semiconductor output capacitances, then an estimate of the average energy loss is given by the product between the switching frequency and the sum of these loss sources. Therefore, it is reasonable to assume that the total switching loss is directly proportional to switching frequency: the more switching frequency, the more energy losses.

3.2.1 Diode reverse-recovery

The turn-off transitions of a diode are illustrated in Fig. 3.1

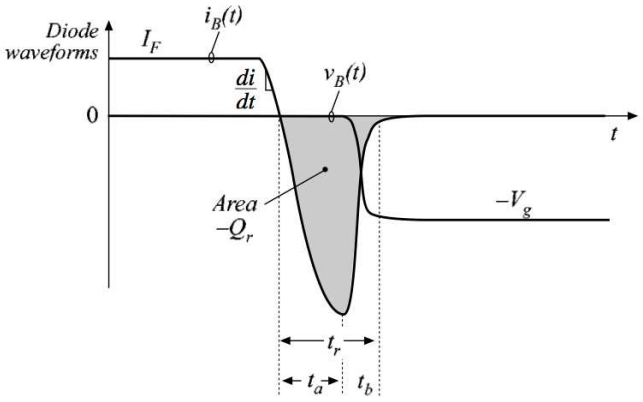

Fig. 3.1. Reverse-recovery occurring during diode turn-off.

When the diode is in its conduction state, stored minority charge of magnitude Q dependent on the forward current I_F can be observed. This minority charge must be removed before the diode can become reverse-biased. There are two mechanisms for removal of this charge: passive removal through recombination inside the diode, and active removal through negative diode current. The amount of charge that recombines is dependent on the rate di/dt at which the diode current changes during the turn-off transition, which in turn depends

on the IGBT turn-on switching speed and stray inductances. The remaining stored charge is actively removed. The actively removed charge is called the *recovered charge* Q_r. During the reverse-recovery time, with duration t_r, it occurs that negative current flows through the diode and the diode remains forward - biased while the instantaneous power loss in the transistor is very high. The voltage V_g in Fig. 3.1 is the dc link voltage (i.e. $V_g = v_1$). The functional dependence of Q_r and t_r on the diode forward current i_L is determined by the physical mechanisms within the diode. At very low current, Shockley-Read-Hall recombination [79, 76], dominates the diode behaviour, and the dependence of the stored charge Q on the forward current can be approximated as linear. For intermediate currents (i.e., the usual operating range of the diode), injection efficiency typically dominates the device behaviour, and Q varies as the square root of forward current. For very large currents, Auger recombination may become dominant, leading to a cube root dependence of Q on forward current. The recovered charge Q_r and reverse-recovery time t_r will be proportional to Q. It means that the forward current can be approximated as a third-order polynomial function of Q. Since injection efficiency usually dominates over the normal operating range of the power diode, a simpler approximation is to express the term Q to be proportional to the square root of the forward current:

$$Q = k_{Q_r}\sqrt{I_F}. \tag{3.1}$$

Hence, the switching loss arising from the diode reverse-recovery mechanism will have a greater impact on efficiency as the load power is reduced. The coefficient k_{Q_r} is also a function of the junction temperature and the turn-off di/dt. The relationship between the on-state stored charge Q and the recovered charge Q_r depends on rate of charge di/dt of the diode current during the IGBT turn-on transition. If di/dt is very high (tending towards a step change of diode current), then $Q_r \approx Q$. It may be supposed that the recovered charge Q_r depends on I_F in the same form as Q. Lower rates of di/dt cause a significant amount of the stored charge to recombine during the diode turn-off process, so that $Q_r < Q$. The quantities Q_r and t_r then additionally depend on di/dt. For very slow di/dt, Q_r and t_r become independent of I_F and are functions of the only term di/dt. The reverse-recovery time t_r is related to the recovered charge Q_r according to

$$t_r = \sqrt{\frac{2Q_r(1+S)}{di/dt}}, \tag{3.2}$$

where S is the *snappiness factor* of the diode and it is determined by the physical diode construction. Moreover, Eqs. (3.1)-(3.2), for fixed di/dt, permit to determine that the diode reverse-recovery time t_r, varies with on-state current I_F according to

$$t_r = k_{tr}\,(I_F)^{\frac{1}{4}}, \tag{3.3}$$

where k_{tr} is a proportionality coefficient that is a function of di/dt.

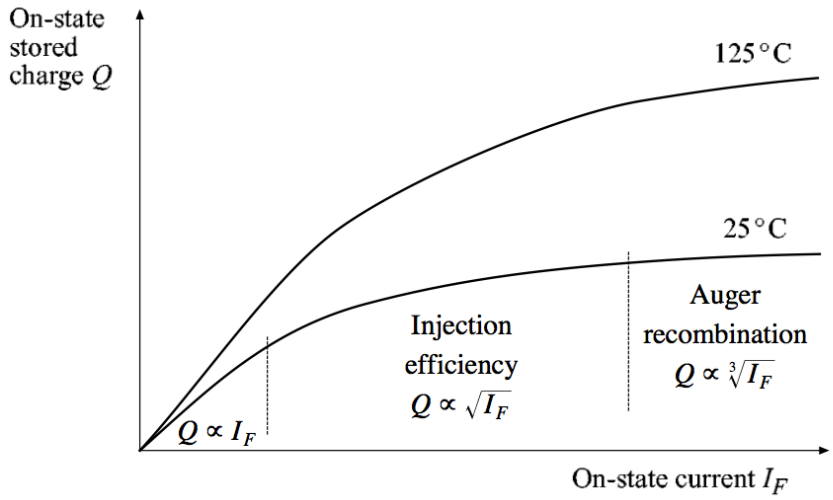

Fig. 3.2. Theoretical variation of diode charge with on-state current, and the dominant physical mechanisms

3.2.2 IGBT current tailing

The IGBT can be viewed as a MOSFET cascaded by a PNP bipolar junction transistor. If the IGBT is in its condition state, part of its current flows through the effective MOSFET, while the remainder flows through the PNP section; the ratio of these two currents is determined by the device construction. During the turn-off transition, the MOSFET turns off very quickly, and its share of the on-state current is therefore interrupted quickly. However, the current of the PNP continues to flow until the stored minority charge within the n region has recombined. The IR data sheets for recent devices illustrate that such energy, Q_{tail}, is a linear function of the on-state current I_F. Current tailing can be the largest single loss mechanism of an IGBT inverter and any dependence of Q_{tail} is critical. It is assumed here that simple recombination leads to a linear dependence:

$$Q_{tail} = k_{Q_t} I_F. \tag{3.4}$$

This linear dependence implies that the effect of current tailing on inverter percent efficiency is independent of load power.

3.2.3 IGBT turn-on loss

Significant losses can also be observed during the rise time of the collector current during the IGBT turn-on transition. During this interval, the gate driver charges the gate capacitance of the IGBT. At high currents, it could

occurs to supply minority charge to the effective PNP transistor within the IGBT, further slowing the turn-on transition. Time t_{on} is required for the IGBT collector current to rise from zero to the inductor current I_F; during this time, the diode remains in its on state and the IGBT collector-to-emitter voltage remains fixed at the dc link voltage V_g. Assuming a constant slope rise, di/dt, of the collector current, then it is possible to derive the equations:

$$\frac{I_F}{t_{on}} = \frac{di}{dt},$$
$$W_r = \frac{1}{2} V_g I_F t_{on} = \frac{V_g I_F^2}{2(di/dt)}.$$

It has already observed that di/dt decreases at large load currents and low dc link voltage. This causes the energy loss induced by this mechanism to increase significantly at high current. The loss during the turn-on transition is not significant at light load current and high voltage, because of the strong dependence on I_F and because di/dt is dominated by the fast switching of the effective IGBT MOSFET at low current.

3.2.4 Device output capacitances

The output capacitances of the IGBT and diode are non-linear elements, whose incremental values vary approximately as the inverse square root of applied voltage. The energy stored in these capacitances is lost in the IGBT during its turn-on transition. Each inverter phase contains two IGBTs and two diodes, each of which exhibits output capacitance. During the turn-on transition of the upper IGBT, the lower diode turns off and undergoes the reverse-recovery process. The switching loss caused by the output capacitance of the lower diode is included in the reverse-recovery computations. However, it remains to include the energy stored in the capacitances of the upper diode and both IGBTs. The incremental output capacitance of an IGBT of diode can be modelled by a function of the form

$$C = \frac{dq}{dv} \approx \frac{C_0}{\sqrt{v}}. \tag{3.5}$$

This model is sufficiently accurate for computation of the switching losses induced by output capacitance. The constant C_0 is extracted from the incremental capacitance specified on the manufacturer's data sheet and the term v represents the applied collector-to-emitter or cathode-to-anode voltage. The energy stored in the output capacitance is found by integration of the above equation, as follows:

$$W_c = 2C_0 V_{max}^{\frac{3}{2}}, \tag{3.6}$$

where V_{max} is the off-state voltage of the device. In a dc-link inverter, this loss is a function of th dc link voltage but is independent of current. Hence this loss

is independent of power throughput. MOSFETs tend to exhibit higher output capacitances than IGBTs or diodes, because of the relatively large chip area of similarly rated MOSFETs. In consequence, this source of switching loss is more significant in MOSFET inverters than in systems containing IGBTs. Nonetheless, it can be a significant loss at light load operating conditions.

3.3 Proposed conversion scheme

3.3.1 The conversion stage

In this section an overview of the proposed scheme is presented with a detailed description of the signal generator and filter characteristics.

The overall scheme

The considered conversion scheme [20] is depicted in Figure 3.3

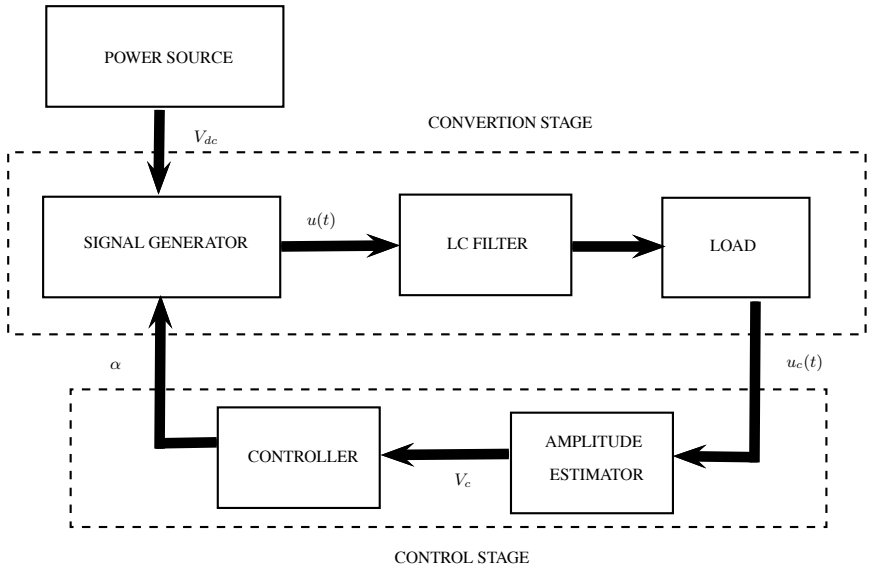

Fig. 3.3. Considered power conversion scheme

A power source, characterized by a constant voltage level equal to $2V_{dc}$, is used to generate a piecewise constant signal, namely $u(t)$, with a period equal to the desired one, via a signal generator block reported in Figure 3.3. An $LC-$type filter is also considered that presents an explicit parameter tuning equations and that is able to generate the desired sinusoidal signal by taking into account the specified load typology. The amplitude estimator and the

controller, that form the control stage of the proposed scheme, are able to adjust the central zero-level of the $u(t)$ signal in a period according to the informations on the estimated amplitude. The developed technique provides a piecewise constant signal symmetric with respect to the half of the period and characterized by an unique adjustable central zero-level governed by a single parameter that is governed by the control algorithm. The signal generator, that is the first block of the entire conversion stage, is able, by an opportune choice of parameter tuning, to provide a $T-$periodic three-level signal where the levels are equal to $\{+V_{dc}, 0, -V_{dc}\}$ and $2V_{dc}$ is the constant input voltage. Therefore, the signal $u(t)$ can be described as follows

$$u(t) = \begin{cases} +V_{dc} & KT \leq t \leq KT + \tau_1 \leq KT + \frac{T}{2}, \\ 0 & KT + \tau_1 \leq t < KT + \tau_2, \\ -V_{dc} & KT + \frac{T}{2} \leq KT + \tau_2 \leq t < (K+1)T, \end{cases} \tag{3.7}$$

where $\tau_2 - \tau_1$ represents the time duration of the central zero-level (as indicated in Figure 3.4)

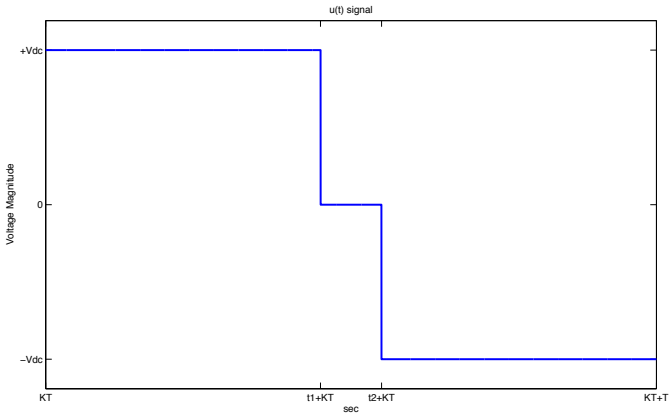

Fig. 3.4. Proposed $u(t)$ signal

In order to guarantee a zero mean value for the generate $u(t)$ signal, it is necessary to consider the following constraint on the commutation instants:

$$\tau_1 + \tau_2 = T. \tag{3.8}$$

By defining the α parameter as the ratio between τ_1 and the period T,

$$\alpha = \frac{\tau_1}{T}, \quad \alpha \in \left(0, \frac{1}{2}\right) \tag{3.9}$$

the signal can be described as

$$u(t) = \begin{cases} +V_{dc} & KT \leq t < (K+\alpha)T \\ 0 & (K+\alpha)T \leq t < (K+1-\alpha)T, \\ -V_{dc} & (K+1-\alpha)T \leq t < (K+1)T. \end{cases} \tag{3.10}$$

Let us define D as the duration of the centered zero-level. It is possible to verify that

$$\alpha = \frac{T-D}{2T}. \tag{3.11}$$

By taking into account the Fourier expansion of the input signal

$$u(t) = a_0 + \sum_{n=1}^{\infty} \left[a_n \cos\left(2\pi n \frac{t}{T}\right) + b_n \sin\left(2\pi n \frac{t}{T}\right) \right], \tag{3.12}$$

it is straightforward to obtain

$$b_n = \frac{4}{n\pi} V_{dc} \sin^2(n\alpha\pi) \qquad n = 1, 2, ... \tag{3.13}$$

while the a_n coefficients are zero because of the symmetry of the signal.

Simple algebraic manipulations lead to a reformulation of the THD index for the proposed waveform $u(t)$ in terms of the aforementioned α parameter as

$$THD = \sqrt{\frac{\pi^2}{4} \alpha csc^4(\alpha\pi) - 1}. \tag{3.14}$$

In Figure 3.5 the THD function with respect to α variations is depicted.

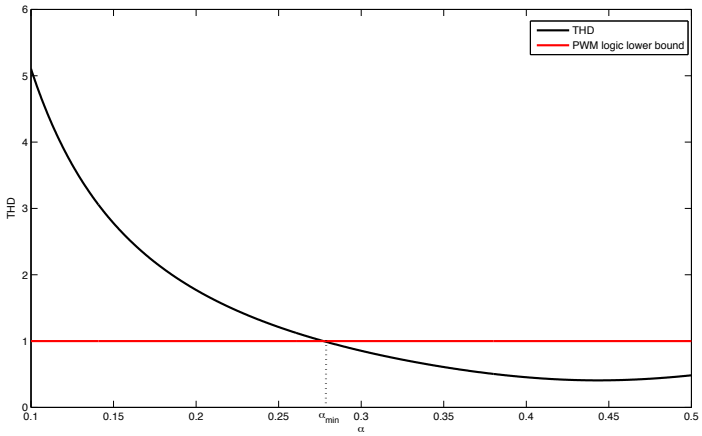

Fig. 3.5. THD function vs α parameter

In order to highlight the results of the proposed method with respect to the ones of standard approaches, a comparison with sinusoidal PWM is provided.

It has been shown that such a technique is based on a comparison between two signals: a carrier signal with amplitude E_c and a modulating one with amplitude E_m. In the case of SPWM, Eq. (2.2) can be rewritten as

$$THD_{SPWM} = \sqrt{\frac{2V_{dc}^2 - (a_1^2 + b_1^2)}{a_1^2 + b_1^2}}. \tag{3.15}$$

It is known that the fundamental amplitude of a SPWM signal is well approximated as

$$\sqrt{a_1^2 + b_1^2} \approx V_{dc}\frac{E_m}{E_c} \tag{3.16}$$

and so Eq. (3.15) can be simplified in

$$THD_{SPWM} \approx \sqrt{\frac{2E_c^2 - E_m^2}{E_m^2}}. \tag{3.17}$$

Since $E_m \leq E_c$, it is evident that, in the best case, the minimum value for the THD_{SPWM} is 1. Moreover, there is an isomorphism between the switching instants computation and Kepler's problem [20]. Therefore, it is interesting to note that by considering the solution of Kepler's problem in terms of Kapteyn series and by taking advantages from the results in [24] where an integral representation of a class of Kapteyn series is proposed, the generated signal spectrum can be analysed by considering simple integral expressions. Figure 3.5 shows that the proposed approach permits to obtain pre-filtered signals with lower THD levels for a determinate values range of the parameter α. Therefore, to obtain pre-filtered THD values less than 1, the inverter must be tuned with α parameter values such that:

$$\alpha \geq \alpha_{min}, \tag{3.18}$$

with $\alpha_{min} = 0.2770805243$. Moreover, it is also evident, by a simple analysis of Eq. 3.14, that a minimum can be obtained in

$$\alpha = \alpha^* = 0.4434849545. \tag{3.19}$$

The inverter switches are stressed only with a working frequency equal to $3f_{ref}$ where f_{ref} is the desired output frequency. Only three commutations are needed unlike standard approaches where the inverter is subject to very higher working frequencies and the switching stress is so drastically reduced.

LC filter tuning

An opportune LC-filter is considered in the conversion scheme in Figure (3.3); such a filter is able to reduce the harmonic content of the input signal providing an output sinusoidal signal with desired amplitude and frequency. It

is worth noting that a very different filtering action is required in this scenario. The discussed signal $u(t)$, in fact, is characterized by a spectrum that is completely different with respect to the ones provided by any PWM signal. In standard approaches, the spectrum is not zero only for particular orders of the harmonics. Unlike the standard one, in the proposed approach the considered signal does not have such a property (see Figs. (3.6) and (3.7)); a more sensitive filtering action of the input signal must be performed and, in order to accomplish this task, the load typology has been taken into account.

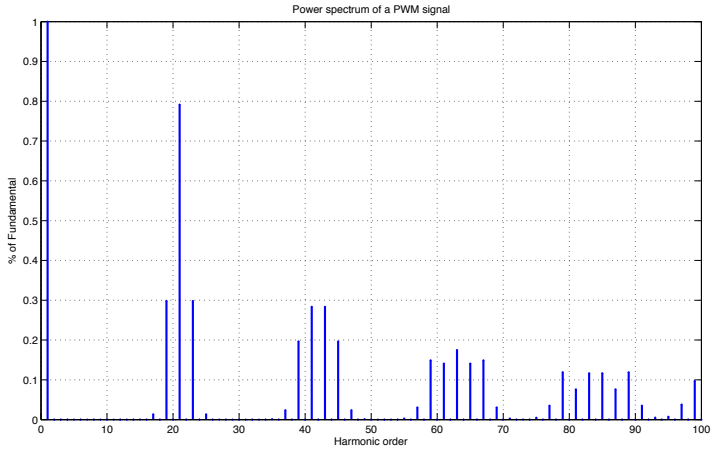

Fig. 3.6. Standard PWM signal frequency spectrum

The implemented tuning algorithm permits to neglect any variations effect of the filter components on the amplitude of the output signal. To better understand the filter action, let us consider the series filter-load that is reported in Figure 3.8 and let us define $F_L(s)$ as the transfer function between the input voltage $u(t)$ and the load voltage $v_L(t)$.

The expressions of the $j-$th harmonic of signal $v_L(t)$ can be derived from Eqs. (3.13) as

$$\begin{cases} \hat{a}_n = 0, \\ \hat{b}_n = \frac{4}{n\pi} V_{dc} \sin^2(n\alpha\pi) \left| F_L(jn\omega_u) \right|, \end{cases} \tag{3.20}$$

where $\omega_u = \frac{2\pi}{T}$ is the desired frequency. The filter tuning must accomplish two targets: it must maintain the amplitude of the output sinusoidal waveform to a desired value and, in the meanwhile, the output amplitude must be insensitive with respect to filter parameters variations. In order to have the fundamental amplitude equal to a desired value, namely V_p, the following equation must be verified.

$$\frac{4}{\pi} V_{dc} sin^2(\alpha\pi) \left| F_L(j\omega_u) \right| = V_p. \tag{3.21}$$

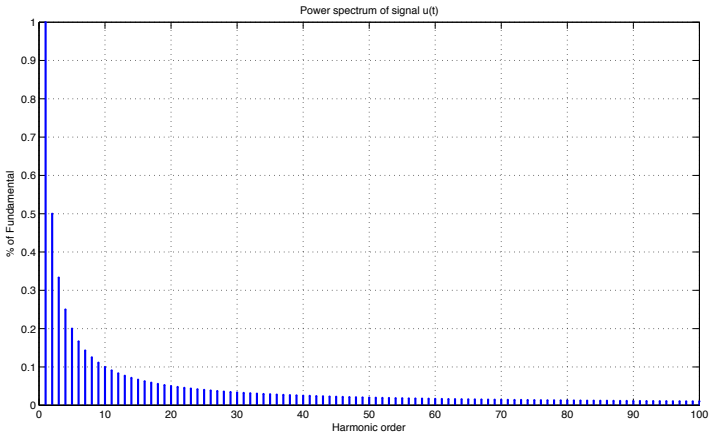

Fig. 3.7. Proposed signal frequency spectrum

Clearly the fundamental amplitude depends on the $LC-$filter parameters: any variation on the filter parameters results in variations on the output amplitude. It is easy to derive that the relation between components and amplitude variations is the following

$$\frac{\Delta\hat{b}_1}{\hat{b}_1} \approx \gamma_L \frac{\Delta L}{L} + \gamma_C \frac{\Delta C}{C}, \tag{3.22}$$

where

$$\gamma_L = \frac{\partial\hat{b}_1}{\partial L}\frac{L}{\hat{b}_1}, \tag{3.23}$$

$$\gamma_C = \frac{\partial\hat{b}_1}{\partial C}\frac{C}{\hat{b}_1} \tag{3.24}$$

are the sensitivity coefficients of the output amplitude with respect to inductance and capacitance variations. By choosing to make insensitive the amplitude to any possible capacitor variation, the following constraint is derived

$$\gamma_C = 0. \tag{3.25}$$

Eqs. (3.21) and (3.25) permit to obtain analytically an opportune tuning of $LC-$filter that guarantees the imposed constraints. In the case of resistive/inductive load (R_L, L_L) (see Figure 3.9), the transfer function $F_L(s)$ can be expressed as

$$F_L(s) = \frac{R_L + sL_L}{R_L + s(L + L_L) + s^2CLR_L + s^3CLL_L} \tag{3.26}$$

and it is straightforward to obtain the filter components by solving Eqs. (3.21) and (3.25) as

$$L = \frac{4}{\pi} V_{dc} \frac{(R_L^2 + L_L^2 \omega_u^2) sin(\alpha\pi)^2}{R_L V_p \omega_u}, \tag{3.27}$$

$$C = \frac{4 L_L V_{dc} \omega_u + \pi R_L V_p csc(\alpha\pi)^2}{4 R_L^2 V_{dc} \omega_u + 4 L_L^2 V_{dc} \omega_u^3}. \tag{3.28}$$

Note that the solutions are still valid in the case of pure resistive load ($L_L \equiv 0$).

Example. A resistive-inductive load is characterized by $R_L = 0.0279\Omega$ and $L_L = 0.18462mH$. The input voltage source is equal to $V_{dc} = 420V$. The load requires a sinusoidal voltage amplitude $V_d = 220\sqrt{2}$ and a desired period $T = 0.02$ seconds. The optimal value for $\alpha = \alpha^*$ is chosen obtaining a pre-filtered THD equal to 0.4073. The results in Eqs (3.27) provides the following tuning

$$L = 0.78697mH,$$
$$C = 57.443mF.$$

In Figs. (3.10)-(3.11) the output voltage and its spectrum are depicted. The THD of the output voltage is 0.00109 with a voltage peak equal to $309.27V$.

3.3.2 The control stage

The control stage consists in an amplitude estimator and a controller that must maintain the output amplitude to a desired value. The overall algorithm takes advantages on the dependence between the output amplitude and the α parameter. Note that variations of the α parameter in an opportune range results in variations on the output fundamental harmonic. Therefore, it has been possible to develop a discrete-time updating law where the update occurs every T seconds and that controls the α parameter in order to obtain a constant output level. The algorithm starts with an initialization phase: the value $\alpha_0 = (T - D_0)/(2T)$ is chosen with D_0 the nominal duration of the centered zero-level, and, according to this value, the filter is tuned with Eqs. (3.27). Considering the $k-$th period of the output voltage, the control algorithm is composed by three steps:

- Step 1. The output voltage amplitude is estimated. Define this estimate as V_c.
- Step 2. The parameter α at the $(k+1)$-th period is updated depending on its value in the k-th period according to

$$\alpha_{k+1} = \frac{1}{\pi} \arcsin \left[\sqrt{\frac{V_p}{V_c}} \sin(\alpha_k \pi) \right]; \tag{3.29}$$

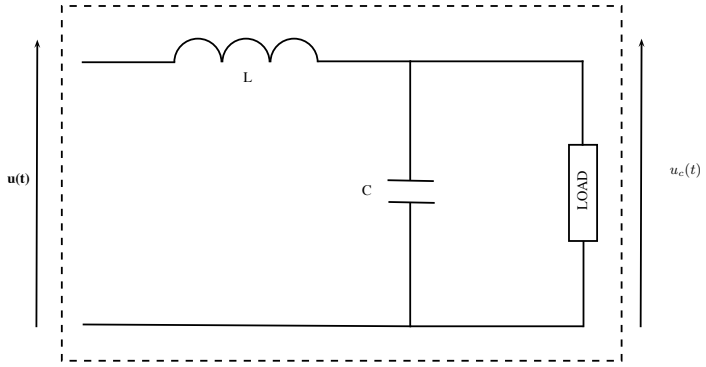

Fig. 3.8. Series filter-load circuit

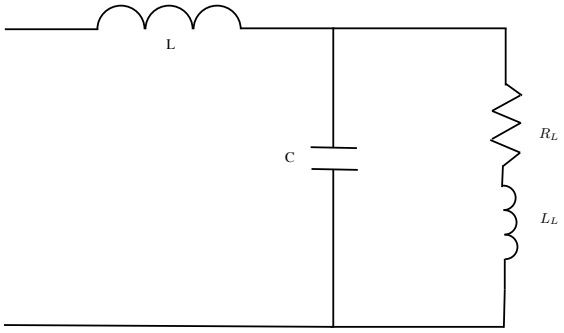

Fig. 3.9. Resistive/Inductive load case.

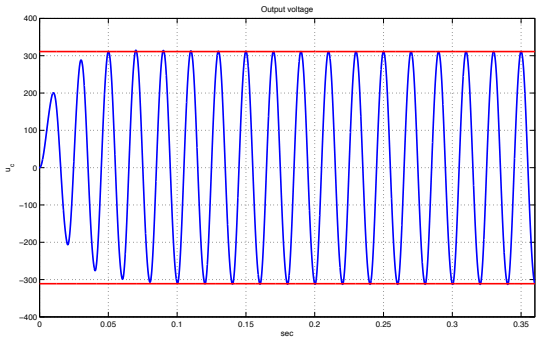

Fig. 3.10. Generated output voltage

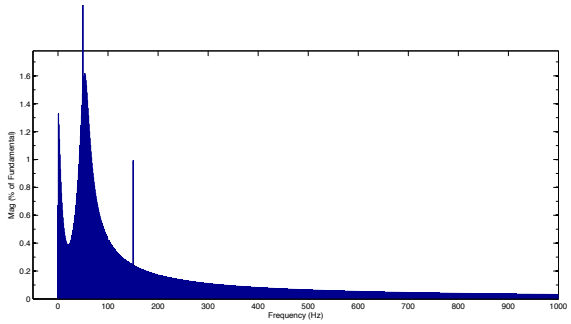

Fig. 3.11. Output frequency spectrum

- Step 3. go to Step 1.

Example. By taking into account the Example in Sec. 3.3.1 a variation of $+10\%$ on the filter inductance and of about -10% on the filter capacitor is assumed to occur. A variation of about -20% of the load resistor is considered too. In Figure 3.12 the output voltage is shown without the action of the proposed controller. Note that the amplitude constraint is valid no more with a voltage peak equal to $335V$. In Figure 3.13 the voltage signal is depicted when the controller action is considered and in Figure 3.14 the adaptation of the parameter α is reported in order to adjust the output amplitude. Figure 3.15 shows how the variations on the parameter α affect the THD values of the output signal that becomes equal to 2.26% with a voltage peak equal to $305.4V$ as reported.

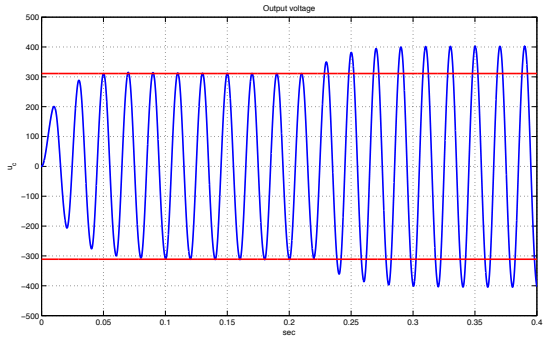

Fig. 3.12. Generated output signal without controller action

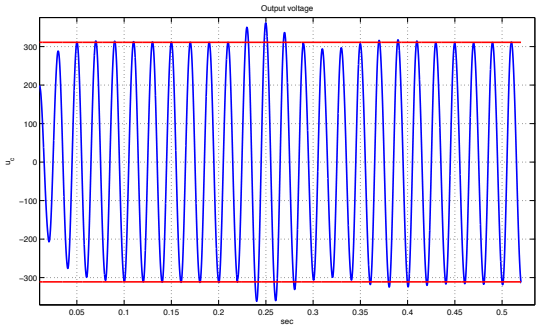

Fig. 3.13. Controller action on the output voltage

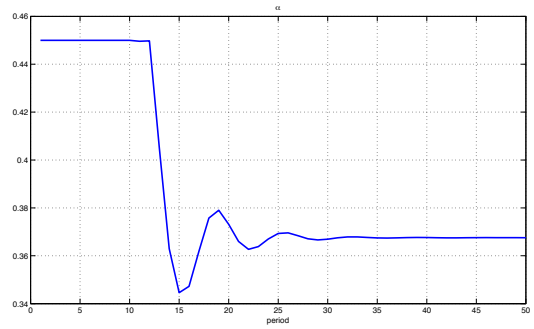

Fig. 3.14. Adaptation of the controller parameter α

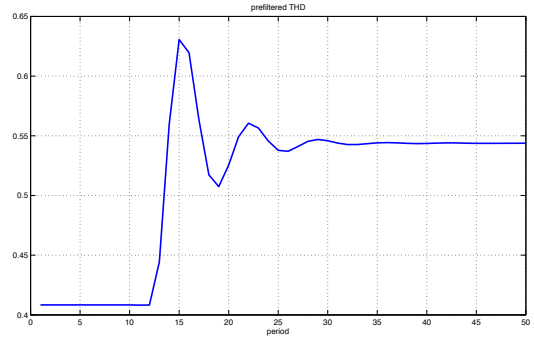

Fig. 3.15. THD changes due to the modifications of parameter α

4

Synchronization techniques

4.1 Introduction

Modern studies about power converters deal largely with the problems arising from the connection between the converter system and the utility power grid. In such cases, the synchronization between the grid voltage and the voltage or current synthesized by the converter is a central task. Therefore, the whole parameters set, i.e. phase, amplitude and frequency of the utility voltage, represents a critical information for the operation of the grid-connected inverter systems. Examples can be pointed out as:

- converters that inject energy coming from alternative supplies into the grid;
- active power line conditioners, FACTS and custom power devices (eg. DVR, STATCOM, active filters).

In such applications, an accurate and fast detection of the phase angle and the amplitude of the utility voltage is essential to assure the correct generation of the reference signals and to cope with the new upcoming standards. The grid voltage monitoring is used to ensure that the performances of a grid-connected system comply the standard requirements for operation under common utility distortions as line harmonics/notches, voltage sags/swells/loss, frequency variations and phase jumps. Moreover, in many cases, the reference signal obtained from the grid voltage is contaminated by harmonics, which may have been produced by the power converter itself or generated elsewhere. Such harmonics degrade the performances of the standard synchronizer systems. These aspects lead to the fact that grid-connected converters have to support the grid services (voltage and/or frequency) and keep generation up event in the case when the voltage are distorted and unbalanced. Basically two families of synchronization systems can be distinguished that are the phase - locked loops (see, among others, [8, 19, 38, 45]) and, on the other hand, the resonant adaptive notch filter (**ANF**, see [17, 39, 43, 44, 69]). A PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference

or input signal in frequency as well as in phase. In the synchronized-, that is often defined as locked-, state the phase error between the oscillator's output signal and the reference signal is zero, or it remains ϵ-constant. If a phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum. In such a control system the phase of the output signal is actually locked to the phase of the reference signal. Eventually present noise, distortions, and frequency variations affect the complexity of such systems. PLL schemes are becoming a standard *de-facto* in the conversion systems. In three-phase systems, the PLL based on a synchronous reference frame (SRF-PLL, in [47]) has become a conventional grid synchronization technique. However, the response of the SRF-PLL is unacceptably deficient when the utility voltage is unbalanced. The decoupled double synchronous reference frame PLL (DDSRF-PLL, see [74]) overcomes this drawback by using two synchronous reference frames and a decoupling network. The second synchronizator family, represented by the ANF filters, are conceptually very similar with PLLs.

ANFs are obtaining a growing interest nowadays and most of the ANF literature involves discrete-time algorithms, motivated by the natural digital implementation route of a digital signal processing. The basic idea is that the measured data is used to excite a resonator, whose output and its time-derivative enter the adaptation law to update the frequency estimate. It is common, in the tuning of a ANF filter, to first use continuous-time theory, given the expected range of frequencies, in order to guarantee the system stability. In a second step, discretisation should take place to build a practical instrument. Modern ANF schemes have their roots in the discrete time method of [69], placed into a continuous-time framework by [12], and analysed by Hsu [46]. In particular, [46] proposes a globally convergent adaptive notch filter in order to estimate on-line the parameters of the input sinusoid. The work of [46] has introduced a continuous-time adaptive notch filter with a time scaling and equipped with a normalized adaptation mechanism. However, the proposed stability analysis is guaranteed only when the input signal is a purely sinusoid while a detection technique based on using adaptive notch filters for estimating multiple frequencies in a single-phase system is presented in [64]. In the following the two families will be discussed in details remarking the differences between the approaches. PLLs systems are different from the ANFs in the sense that they actively generate its output signal while the ANFs passively extract it from the input signal. Most PLLs involve relatively narrow frequency bands but it is possible by careful control analysis to design a PLL for wider ranges. The main design parameters in a PLL is its natural frequency. This loop-bandwidth parameter is analogous to the bandwidth of an ANF and it influences the dynamics for small- perturbation behaviour (on-lock) and the time required to regain lock. It has been demonstrated that large frequencies give fast lock and high variance and *vice versa*.

4.2 Phase-Locked Loop

4.2.1 Basic Concepts

Roughly speaking, a PLL is a device designed in order to that one signal can track another one. It keeps an output signal synchronizing with a reference input signal in frequency as well as in phase. More precisely, the PLL is a servo-system which controls the phase of its output signal guaranteeing that the phase error between output phase and reference phase reduces to a minimum [8, 48, 45]. The functional block diagram of a PLL is shown in Figure 4.1 which consists of a phase detector (**PD**), a loop filter (**LF**), and a voltage-controlled oscillator (**VCO**). Let x_i and x_o be, respectively, the input and the output signals, which can be expressed as

$$x_i(t) = A\cos(\omega_i t + \theta_i) \tag{4.1}$$

and

$$x_o(t) = A\cos(\omega_o t + \phi_o). \tag{4.2}$$

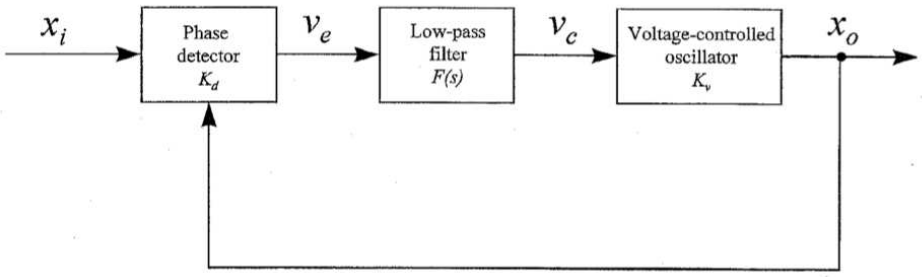

Fig. 4.1. Logic PLL scheme

In the most of the case, the PD is a signal multiplier. If the loop is initially unlocked and the phase detector has a sinusoidal characteristic, the significant output signal $v_e(t)$ at the PD is given by

$$\begin{aligned} v_e(t) = K_d \{ &\cos[(\omega_i - \omega_o)\, t + \theta_i - \phi_o] \\ &+ \cos[(\omega_i + \omega_o)\, t + \theta_i + \phi_o] \}, \end{aligned} \tag{4.3}$$

where K_s is the gain of the PD. The low-pass filter annihilates the component with the higher frequency equals to $\omega_i + \omega_o$. Therefore the output of the LF is

$$v_c(t) = K_d \cos[(\omega_i - \omega_o)\, t + \theta_i - \phi_o]. \tag{4.4}$$

In steady-state conditions,the VCO output signal x_o becomes synchronous with the input signal x_i. The signal x_o can then be expressed as

$$x_o(t) = B\sin(\omega_i t + \phi_o). \tag{4.5}$$

Comparing Eqs. (4.2) and (4.5) shows that the phase ϕ_o in Eq. (4.2) is a linear function of time given by

$$\phi_o = (\omega_i - \omega_o)\, t + \phi_o \tag{4.6}$$

and the LF output signal $v_c(t)$ in Eq. (4.2) is

$$v_c(t) = K_d \cos\left(\theta_i - \phi_o\right). \tag{4.7}$$

The VCO is a frequency-modulated oscillator, whose instantaneous angular frequency ω_{inst} is a linear function of the controlled signal $v_c(t)$, that is

$$\omega_{inst} = \frac{d}{dt}\left(\omega_o t + \phi_o\right) = \omega_o + K_v v_c(t) \tag{4.8}$$

and

$$\frac{d}{dt}\phi_o = K_v v_c(t) \tag{4.9}$$

where K_v is the VCO sensitivity. From Eqs (4.6),(4.7) and (4.9)

$$\omega_i - \omega_o = K_d K_v \cos(\theta_i - \phi_i) \tag{4.10}$$

giving

$$\phi_o = \theta_i - \cos^{-1}\frac{\omega_i - \omega_o}{K_d K_v}. \tag{4.11}$$

Substituting Eq. (4.11) in (4.7) yields

$$v_c = \frac{1}{K_v}\left(\omega_i - \omega_o\right). \tag{4.12}$$

The VCO frequency is dependent on the signal v_c by changing it from its central value ω_o to the input signal angular frequency. If the following relationship

$$\omega_i - \omega_o \ll K_d K_v \tag{4.13}$$

holds, then Eq. (4.11) provides $\theta_i - \phi_o \approx \pi/2$, indicating that the VCO signal is in phase quadrature with the input signal when the loop is in lock. Therefore, the relationship $\theta_o = \phi_o + \pi/2$ can be easily derived. Then Eq. (4.7) becomes

$$v_c = K_d \sin(\theta_i - \theta_o). \tag{4.14}$$

In the case that the phase error $\theta_i - \theta - o$ is sufficiently small, the following approximation can be considered:

$$v_c \approx K_d(\theta_i - \theta_o). \tag{4.15}$$

Due to the fact that θ_o has been expressed in terms of ϕ_o, Eq. (4.11) becomes

$$\phi_o = \theta_i - \cos^{-1} \frac{\omega_i - \omega_o}{K_d K_v}. \tag{4.16}$$

The product $K = K_d K_v$ is referred to as the loop gain. If the frequency difference $|\omega_i - \omega_o|$ is greater than the loop gain, a proper θ_o for lock can no longer exit as evidenced by Eq. (4.16) and, therefore, synchronization can no longer maintain and the loop falls out of lock.

Voltage-Controlled Oscillator

The voltage-controlled oscillators (VCO's) used in the PLL are characterized by the following requirements: 1) phase stability, 2) large frequency deviation, 3) high modulation sensitivity K_v, 4) linearity of frequency versus control voltage and 5) capability for accepting wide-band modulation. The phase stability requirement is in direct opposition to all other four requirements. Four types of VCO commonly used are given in the order of decreasing stability, namely, voltage-controlled crystal oscillators (VCXO's), resonant oscillators, RC multi-vibrators, and $YIG-$tuned oscillators. The phase stability can be enhanced by a number of ways: 1) using high Q crystal and circuit, 2) maintaining low noise in the amplifier portion, 3) stabilizing temperature, and 4) keeping mechanical stability. It worth noting that most of the phase jitter of an oscillator arises from noise in the associated amplifier.

4.2.2 Standard PLL schemes

Ghartemani PLL

The most interesting PLL schemes proposed in literature can be found in [35] (namely **QPLL**). The work in [35] is based on estimating in-phase and quadrature-phase amplitudes of the fundamental component of the input signal and thus is called quadrature PLL (QPLL). An estimation of the input frequency is provided while other informations, i.e. amplitude and phase angle, are not directly estimated but can be obtained through calculation procedures. Further investigations have shown that the QPLL has a highly robust structure. The system permits in fact to filter noise and distortions in a satisfactory manner and it is capable of following large and abrupt variations of the frequency with an adjustable speed. In [36] an enhanced version (namely **EPLL**) has been proposed. The operation scheme of the EPLL system is based on estimating amplitude and phase angle of the fundamental component. The major improvement introduced by the EPLL is in the PD mechanism. The conventional PD mechanism is replaced by a new strategy which allows more flexibility and provides more information such as amplitude and phase angle. Upgrading the proportional controller to a proportional-integrating controller enables the EPLL to estimate the frequency as well. The idea of using in-phase

and quadrature-phase signals in carrier recovery systems is a well- known concept as developed in Costas loop. As the authors have remarked, the QPLL is an improved version of the Costas loop. However, some differences have to be noted: 1) the QPLL multiplies a well-defined error signal with the outputs of the VCO while the Costas loop directly uses the input signal and multiplies it with the outputs of the VCO; 2) the QPLL incorporates two integrating operations after the detectors which can be accompanied by low-pass filters for better performance while the Costas loop only employs low-pass filters; and 3) the QPLL has an external loop to improve its performance. Basically, the QPLL generates the fundamental component of the input signal based on estimations for the in-phase and quadrature amplitudes as well as frequency/phase variations of the input signal. The structure of the QPLL is derived based on applying the gradient-descent method and it considers a sum of two in-phase and quadrature-phase components for its output as

$$y(t) = k_s \sin\phi(t) + k_c \cos\phi(t) \tag{4.17}$$

where the phase can be expressed in terms of the frequency as $\phi(t) = \int_0^t (\omega_0 + \Delta\omega(\zeta))\, d\zeta$. Therefore, the parameters vector is defined as $[k_s, k_c, \Delta\omega]$ and this signal is to estimate the input fundamental component. The QPLL system can be tuned by an opportune choice of three parameters (μ_s,μ_c and μ_f) that control its behaviour. They correspond to the in-phase and quadrature-phase amplitudes k_s and k_c and frequency ω, respectively. The error between the input and the output signal,

$$e(t) = u(t) - y(t), \tag{4.18}$$

is used to adaptively estimate the quadrature amplitudes (k_s, k_c) and phase $\phi(t)$.

The scheme is composed by the following equations

$$\dot{k}_s(t) = 2\mu_s e(t) \sin\phi(t), \tag{4.19}$$

$$\dot{k}_c(t) = 2\mu_c e(t) \cos\phi(t), \tag{4.20}$$

$$\dot{\Delta}\omega(t) = 2\mu_f e(t) \left[k_s \cos\phi(t) - k_c \sin\phi(t)\right], \tag{4.21}$$

$$\dot{\phi}(t) = \omega_0 + \Delta\omega(t), \tag{4.22}$$

$$y(t) = k_s \sin\phi(t) + k_c \cos\phi(t) \tag{4.23}$$

This scheme computes directly the estimates of the parameters vector. It is important to note that the frequency of the input signal is also estimated by the QPLL and it is equal to the derivative of the phase angle. The process of phase detection in the QPLL is fundamentally different from that of the conventional PLL because the structure of the QLL-PD, consisting in six multipliers, two integrators, four different gains and three adders, that enables it to directly estimate the *time derivative* of the phase angle of the desired

component of the input signal. The main structural drawback of the conventional PLL, i.e. presence of non-linear dependency of the error signal to the phase difference, is prevented in the QPLL and the VCO is provided with a driving signal which is equal to the phase variations. As reported in [35], the QPLL presents superior performance over the conventional PLL, particularly wider lock-in and pull-in ranges and faster convergence rate. Mathematical stability analysis to ensure desirable performance of the QPLL is carried out based on the theory of dynamical systems. Specifically, presence and stability of a locally unique periodic orbit are proved in the case of bounded almost periodic signal and in presence of small positive parameters μ_s, μ_c and μ_f

4.2.3 SOGI-PLL

PLL systems make use of functional schemes that must provide signals in quadrature each other. The common methods for the orthogonal signals generator are based on the transport delay block, Hilbert transformation, inverse Park transformation. However these methods have one or more of the following shortcomings: frequency dependency, high complexity, non-linearity, poor or no filtering. In [71] the case of distributed power generation system (**DPGS**) based on a PLL technique is covered that uses a second order generalized integrator (SOGI) as orthogonal generator system. Consequentially, the proposed system has been named as the **MSOGI-FLL** since it is based on multiple SOGIs working together inside of a decoupling detection network which is frequency-adaptive.

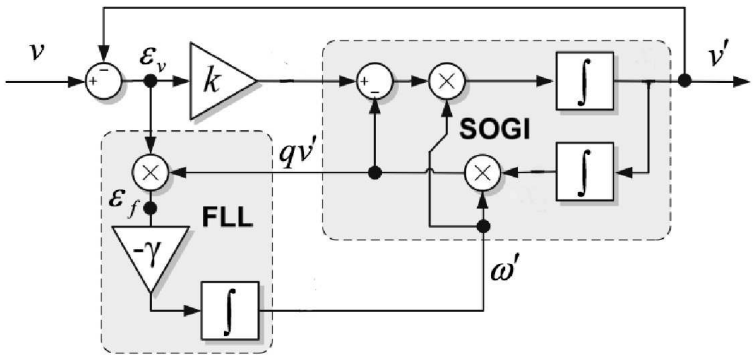

Fig. 4.2. Single-phase grid synchronization system

The block **FLL** in Figure 4.2 stands for *Frequency-Locked Loop* and it permits to adjust the frequency of the generalized integrator in order to track the unknown input frequency. In [71] a local stability analysis for the SOGI system has been presented. Moreover, the general structure of the single-phase

DPGCS including the power circuit and the control diagram is presented in Figure 4.3. As far as FLL system in [71] is concerned, the authors remark the fact that the two SOGI output signals have the same amplitude only when the frequency of the input signal is equal to the SOGI resonant one. Therefore the center frequency of the SOGI block should be adapted until it converges on the unknown input frequency in order to achieve a balanced set of in-quadrature signals with equal amplitudes at its output. The transfer function form the input signal $v(t)$, centered at the unknown frequency ω_c, to the error signal ϵ_v is given by

$$E(s) = \frac{\epsilon_v}{v}(s) = \frac{s^2 + \omega'^2}{s^2 + k\omega' s + \omega'^2}. \tag{4.24}$$

The signals $v_2(t)$ and $\epsilon_v(t)$ are in phase when input frequency is lower than the SOGI resonance one and in counter-phase otherwise. By taking into account such a property, the frequency error variable ϵ_f can be defined as the product of the output signal qv' and ϵ_v. Hence, an integral controller with a negative gain $-\gamma$ can be used to make zero the dc component of the frequency error variable by shifting the SOGI resonant frequency on the unknown one. In [71], an analysis about local stability is conducted under the assumption $\omega' \approx \omega_c$. In such a case, the local dynamics of the FLL can be described as

$$\dot{\omega}_s \approx -2\frac{\gamma}{K_s} x_{1\infty}^2 (\omega' - \omega_c)\omega'. \tag{4.25}$$

where $x_{1\infty}$ takes into account output SOGI signals informations.

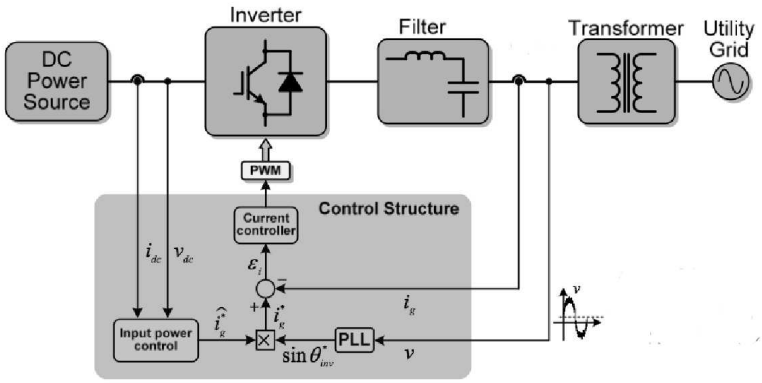

Fig. 4.3. Single-phase DPGS based on PLL technique

An alternative of creating an orthogonal voltage system for a single-phase PLL is presented in [15]. The proposed Orthogonal Signal Generator (**OSG**) method relies on the SOGI concept. The advantages of the proposed approach

include simple implementation independent of the grid frequency and avoidance of filtering delays due to its resonance at the fundamental frequency as it has been shown in the next section. The single-phase PLL based on the SOGI combines all the advantages of other known methods such as Transport-Delay, Hilbert Transformation, and Inverse Park Transformation. In particular it has been shown that the system is characterized by the following properties: 1) filtering of the orthogonal voltage system without delay and 2) making the OSG structure frequency adaptive. However, such a method, as it has been presented, suffers for a common drawback specific to all methods presented. Namely, all OSG methods are sensible at voltage offset. Therefore, an improved OSG-SOGI structure has been proposed in [16] and it is shown in Figure 4.4 that is able to neglect any introduced offset effects.

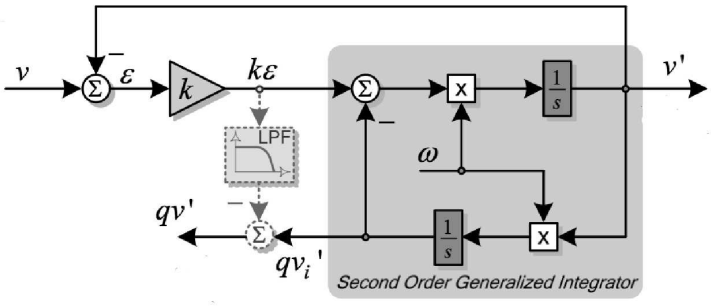

Fig. 4.4. Improved OSG-SOGI structure

In the next Chapter, the most recent proposed SOGI-based schemes will be presented that are able to completely track any unknown biased sinusoid input signal.

Second-Order Generalized Integrator

By considering the SOGI scheme depicted in Figure 4.2, let us assume $v_1(t)$ and $v_2(t)$ the output signals of the SOGI block. In order to generate two orthogonal signals, the filter gain, namely K_S and a frequency values $\omega_s \equiv \omega'$ are needed in input. In the operating mode, if the input frequency is equal to the reference signal frequency, SOGI generates two sine waves ($v_1(t)$ and $v_2(t)$) that have the same magnitude of $v(t)$ and with a phase shift of $\pi/2$ each other. Moreover, v' is in phase with the fundamental of the input signal. Then, intuitively, the presented scheme can be used to track the input signal $v(t)$. The characteristic closed-loop transfer functions of the structure are given by:

$$F_1(s) = \frac{V_1(s)}{V(s)} = \frac{K_s \omega_s s}{s^2 + K_s \omega_s s + \omega_s^2}, \tag{4.26}$$

$$F_2(s) = \frac{V_2(s)}{V(s)} = \frac{K_s \omega_s^2}{s^2 + K_s \omega_s s + \omega_s^2}, \tag{4.27}$$

where $V_1(s), V_2(s)$ stands for the Laplace transforms of $v_1(t)$ and $v_2(t)$ respectively. It is easy to observe that these functions represent two second-order filters with a bandwidth affected by the gain K_s and a resonance angular frequency equal to ω_s. At the resonant frequency there is no attenuation and the phase is equal to zero; instead, there is a quite large attenuation outside the resonance and moreover, if K_s decreases, the bandwidth of the filter becomes narrower resulting a heavy filtering, nevertheless this entails a slowdown on the dynamic response of the system increasing oscillations and the stabilization time. As a consequence, if the input frequency ω_c is equal to the resonance one, the input signal $v(t)$ is filtered and then the signal $v_1(t)$ has the same phase and magnitude as the fundamental of the input signal. The second function represents a second order low-pass filter, with static gain K_s and damping coefficient $K_s/2$; so it has no attenuation and phase equal to $-\pi/2$ at the resonant frequency ω_s. Thus, if the input frequency is at the resonance frequency of the SOGI, the signal $v_2(t)$ is a clean signal orthogonal to $v_1(t)$. Consequently, a trade-off between frequency selectivity and response speed should be adopted. The use of the SOGI as sinusoid signal tracking strongly depends on the frequency input ω_s, thus problems can occur when signal frequency has fluctuations. Then, in order to adjust the SOGI resonance frequency, in many cases its structure is coupled with an adaptive tuning algorithm, as follows. For the orthogonal signals generator, based on SOGI scheme, with the controller gains $K_s, \omega_s > 0$ if $v(t) = A_c \sin(\omega_c t + \phi_c)$, $A_c > 0$, it is effortless to show that $v_1(t)$ and $v_2(t)$ converge exponentially fast to the following quantities

$$v_1(t) = m_1 A_c \sin(\omega_c t + \phi_c + \phi) \tag{4.28}$$

$$v_2(t) = -m_2 A_c \cos(\omega_c t + \phi_c + \phi) \tag{4.29}$$

where

$$m_1 = \frac{K_s \omega_s \omega_c}{\sqrt{(\omega_s^2 - \omega_c^2)^2 + K_s^2 \omega_s^2 \omega_c^2}}, \tag{4.30}$$

$$m_2 = m_1 \frac{\omega_c}{\omega_s} \tag{4.31}$$

and

$$\phi = sign[\omega_s - \omega_c]\frac{\pi}{2} - atan\frac{K_s \omega_c \omega_s}{\omega_s^2 - \omega_c^2}, \tag{4.32}$$

with

$$sign(x) = \begin{cases} +1, x \geq 0, \\ -1, x < 0. \end{cases} \tag{4.33}$$

In [27] a simple relationship between the SOGI signals has been proved via the following result. It has been shown, in fact, that

$$\cos(\phi) = m_1. \tag{4.34}$$

The proof follows by considering the quantity γ as

$$\gamma = \cos\left(sign[\omega_s - \omega_c] - atan\frac{K_s\omega_s\omega_c}{\omega_s^2 - \omega_c^2}\right). \tag{4.35}$$

By using simple trigonometric identities and the equality $\sin(atan(x)) = x/\sqrt{1+x^2}$, the proof follows. Note now that the difference between $v(t)$ and $v_1(t)$ can be expressed as

$$v(t) - v_1(t) = A\sin(\omega_c t + \phi_c + \overline{\phi}) \tag{4.36}$$

where $A = A_c\sqrt{1-m_1^2}$ and

$$\overline{\phi} = -m_1\frac{\sin\phi}{1 - m_1\cos(\phi)}. \tag{4.37}$$

Eq. (4.34) can be used to prove another interesting property involving signals $v(t), v_1(t)$ and $v_2(t)$ that can be rewritten as

$$v_2(t) = m_2 A_c \sin\left(\omega_c t + \phi_c + \phi + \frac{3}{2}\pi\right). \tag{4.38}$$

Taking into account the following equality:

$$\tan\left(x + \frac{3}{2}\pi\right) = -\frac{\cos(x)}{\sin(x)}, \tag{4.39}$$

and the results above, it follows that

$$\frac{v(t) - v_1(t)}{v_2(t)} = sign[\omega_s - \omega_c]\frac{\sqrt{1-m_1^2}}{m_2}. \tag{4.40}$$

Eq. (4.40) represents the central relationship carrying out all the information set needed to track the input sinusoidal signal. Such an expression puts in evidence that the convergence value of the cited sinusoidal signals converges to a constant value affected by all the parameters of the input sinusoid. As a consequence, thanks to these results, the estimation of ω_c, namely $\hat{\omega}_c$, can be obtained as

$$\hat{\omega}_c = \omega_s\sqrt{1 - K_s\frac{v(t) - v_1(t)}{v_2(t)}}. \tag{4.41}$$

It is worth to observe that, from a theoretical point of view, Eq. (4.41) allows to estimate the unknown frequency ω_c, independently from the choice

of K_s and ω_s. To estimate amplitude and phase of the signal $v(t)$, the following signal can be considered

$$\alpha(t) = -v_2(t) + \jmath v_1(t)\frac{\omega_s}{\omega_c}, \tag{4.42}$$

then

$$|\alpha(t)| = m_2 A_c$$
$$arg(\alpha(t)) = \omega_c t + \phi_c + \phi$$

for which, once an estimation of ω_c is obtained, it is straightforward to explicit the estimation of A_c and ϕ_c. By considering the related literature, this method turns out to be one of the first order globally stable non-linear system whose stationary point is the unknown parameter and, as a result, it always converges to the true parameter. The above analysis is based on the assumption of steady-state. In practice, if SOGI is not in its steady state, then the estimator for ω_c is not valid and there is an error between the estimate value $\hat{\omega}_c$ and the true one. This error will be a function of initial conditions and will decay exponentially fast to zero since $K_s, \omega_s > 0$. If the measurements of $v(t)$ are noise free, an estimation $\hat{\omega}_c$ of ω_c can be obtained by Eq. (4.41). Nevertheless, the division in such an equation is not desirable since $v_2(t)$ could assume values nearly close to zero and, in practice, the noise affecting the measurements may lead to an erroneous estimate of ω_c. Therefore, even if the aforementioned non-linear system is theoretically sufficient to estimate all the unknown parameters, it is necessary to overcome these drawbacks, as it has reported in the next Chapter.

4.3 Adaptive notch filters

The concept of frequency-locked loop is extremely related to *adaptive notch filters* ideas. Such filters are particular system characterized by a damping factor ζ and an adaptive gain γ and they are proposed with the prospect of greater scope in design, as there are only two key parameters to be tuned. The problem they cope with it to estimate the frequency ω_c of a sinusoid:

$$y(t) = A_c \sin(\omega_c t + \phi_c). \tag{4.43}$$

The basic structure of a general ANF filter is reported in Figure 4.5,

The estimate of the unknown frequency, namely θ, returns to the resonator, so that it is turned (locked on) to the incoming sinewave when $\theta = \omega_c$. In the original method presented in [69] there are two design parameters: the damping factor ζ, which determines the bandwidth of the resonator, and the adaptive gain γ, which affects the convergence properties of the algorithm. By considering the algorithm in [69], the resonator is given by

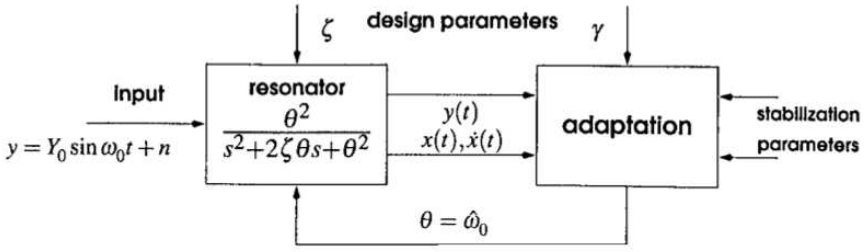

Fig. 4.5. Structure of an adaptive notch filter

$$\ddot{x}(t) + 2\zeta\theta\dot{x}(t) + \theta^2 x(t) = y, \tag{4.44}$$

and the adaptation law is

$$\dot{\theta} = -\gamma_R \left(y - 2\zeta\theta\dot{x}(t)\right) x(t). \tag{4.45}$$

Is is important to remark that these differential equations are highly coupled and non-linear, so that the majority of the approaches to the analysis for the solutions of such equations is based only on averaging (*frozen parameter*) methods where the adaptive gain γ_R is small and θ is varying slowly enough so that transient effects in the resonator can be ignored. Substituting Eq. (4.44) into Eq. (4.46) one can obtain the *frozen* θ:

$$\dot{\theta} = -\gamma_R \left(\theta^2 - \omega_0^2\right) x(t)^2, \tag{4.46}$$

using the fact that the resonator output, in the steady-state with θ constant and when $n = 0$, is just a sine wave at the incoming frequency ω_0. In [46] a *scaling* is introduced into resonator providing the following equations

$$\ddot{x}(t) + 2\zeta\theta\dot{x}(t) + \theta^2 x(t) = \theta^2 y, \tag{4.47}$$

and with the parameter-update equation

$$\dot{\theta} = -\gamma_H \left(\theta^2 y - 2\zeta\theta\dot{x}(t)\right) x(t). \tag{4.48}$$

The adaptive gain is no longer constant but includes normalization terms essential for the proof of global convergence:

$$\gamma_H = \frac{\epsilon}{\left(1 + NX^2\right)\left(1 + \mu\theta^\alpha\right)}, \tag{4.49}$$

where X^2 is the internally computed amplitude variable:

$$X^2(t) = x^2(t) + \left(\frac{\dot{x}(t)}{\theta}\right)^2. \tag{4.50}$$

The extra parameters N, μ and α are required for stabilisation of the algorithm; their choice if relatively straightforward from knowledge of the bounds on the data characteristics. As already reported, frozen-parameter analysis [51] has be used to deduce the behaviour of algorithm in [46]. It has be essentially assumed that the parameter γ in the update

$$\dot{\theta} = -\gamma x(t) x_N(t) \tag{4.51}$$

is small enough and that the signals $x(t), x_N(t)$ are the outputs of constant-coefficient transfer functions $G_R(s)$ (the resonator) and $G_N(s)$ (the notch filter). By following this approach, the equations for $x(s)$ and $x_N(s)$ can be derived as

$$\begin{aligned} x(s) &= \frac{\theta^2}{s^2 + 2\zeta\theta s + \theta^2} y(s) = G_R(s) y(s) \\ x_N(s) &= \frac{\left(s^2 + \theta^2\right)\theta^2}{s^2 + 2\zeta\theta s + \theta^2} y(s) = G_N(s) y(s). \end{aligned} \tag{4.52}$$

Once the input data $y(t)$ is a purely sinusoid at frequency ω_c, both x, x_N are also sinusoidal at the same frequency. If the ANF scheme is locked, i.e. $\theta = \omega_c$, it has been shown that $x_N = 0$. Moreover, the phase lags of x, x_N are equal for all θ, except that there is a phase change of π when θ becomes greater than ω_c.

The resonator equation for a given fixed $\theta = \theta_o$ is

$$\ddot{x} + 2\zeta\theta_o \dot{x} + \theta_o^2 x = \theta_o^2 Y_o \sin(\omega_0 t). \tag{4.53}$$

If the ANF filter is initially locked, then it must be verified that $\ddot{x} + \theta_o^2 x = 0$ and so, clearly,

$$\dot{x}(t) = \frac{1}{2\zeta} A_c \theta_0 \sin(\theta_0 t) \tag{4.54}$$

From the relationship above, the following can be easily obtained

$$x(t) = -\frac{1}{2\zeta} A_c \cos(\theta_0 t). \tag{4.55}$$

From Eqs. (4.54)-(4.55), the amplitude variable used for normalization is

$$X^2 = x^2 + \left(\frac{\dot{x}}{\theta_0}\right)^2 = \frac{A_c^2}{4\zeta^2}. \tag{4.56}$$

Note that the effect of small ζ is to provide a much magnified amplitude: this improves the noise rejection of the ANFs, as discussed below. As ζ is known, X^2 represents a measurement of the unknown amplitude A_c without any harmonics, unlike simple phase-locked loops which produce second harmonics, even when in lock. If the input frequency suddenly changes to $\omega_c \neq \theta_0$, then the response of the resonator has two components: the transient due to

the original locked oscillations at θ_0, and the steady-state response caused by the sinusoidal forcing function at ω_c. Clearly, the update $\dot{\theta} = -\gamma x x_N$ involves signals which are non-linear functions of θ via the resonator equations and therefore full analysis of transient behaviour is impossible, but considerable insight is obtained by assuming γ to be so small that the resonator output is always *steady state* ('frozen parameter' analysis). Therefore, the signals x, x_N can be deduced as

$$x(t) = \frac{\theta^2}{\sqrt{\left(\theta^2 - \omega_c^2\right)^2 + 4\zeta^2\theta^2\omega_c^2}} A_c \sin(\omega_c t - \phi). \tag{4.57}$$

Even this function is non-linear in θ. Therefore, it is convenient to write $\omega_c = \lambda\theta$ such that $\lambda = 1$ when the estimate θ equals the input frequency ω_c. The time-scale is also changed to give $t^* = \theta t$, so that the input signal $y(t)$ becomes

$$y(t) = A_c \sin(\omega_c t) \rightarrow y(t^*) = A_c \sin(\lambda t^*). \tag{4.58}$$

By considering $s \sim d/dt$ and defining $p \sim d/dt^*$, the time-scaling gives $s = \theta p$. If ω_c is constant, it is easy, from $\omega_c = \lambda\theta$, to obtain

$$\dot{\theta} = -\frac{\omega_c}{\lambda^2}\dot{\lambda}. \tag{4.59}$$

Hence, the frozen-parameter update equations become

$$\frac{d}{dt}\lambda = \gamma\frac{\lambda^2}{\omega_c} x(t^*) x_N(t^*) \tag{4.60}$$

where

$$x = \frac{1}{p^2 + 2\zeta p + 1} y, \quad x_N = \frac{p^2 + 1}{p^2 + 2\zeta p + 1}\theta^2 y \tag{4.61}$$

and it is noted that the transfer functions are now *independent* of θ. The steady-state solution for the signals $x(t^*)$, $x_N(t^*)$ are

$$x(t^*) = \frac{1}{\sqrt{(1-\lambda^2)^2 + 4\zeta^2\lambda^2}} Y_0 \sin(\lambda t^* - \phi), \tag{4.62}$$

where

$$\phi = atan\frac{2\zeta\lambda}{1-\lambda^2} \tag{4.63}$$

and

$$x_N(t^*) = \frac{1}{\lambda^2}\omega_c^2(1-\lambda^2)\sin(\lambda t^* - \phi). \tag{4.64}$$

By taking into account such expressions, the update equation for λ can be derived as

$$\frac{d}{dt}\lambda = \gamma\omega_c(1-\lambda^2)X_*^2 \sin^2(\lambda t^* - \phi). \tag{4.65}$$

By averging Eq. (4.65), the update equation in the time-scale t is

$$\frac{d}{dt}\lambda = \frac{1}{2}\gamma\omega_c \frac{1-\lambda^2}{(1-\lambda^2)^2 + 4\zeta^2\lambda^2} A_c^2 \tag{4.66}$$

and, in order to reduce the equivalent equation for Regalia's method in [69], note that x and x_N leading to Eq. (4.67) are both scaled by a factor $\theta^2 = (\omega_c/\lambda)^2$. Hence, the transients for Regalia's ANF are described by

$$\frac{d}{dt}\lambda = \frac{1}{2}\frac{\gamma\lambda^4}{\omega_0^3} \frac{1-\lambda^2}{(1-\lambda^2)^2 + 4\zeta^2\lambda^2} Y_0^2. \tag{4.67}$$

The system response clearly suffers from two major scaling defects. In terms of frequency, the term ω_c^3 indicates that the transient response is strongly affected by the input frequency. Moreover, the factor A_c^2 shows that the adaptive response depends on the input amplitude. There is a further consideration represented by the numerical solution involving very stiff differential equations. In comparison, the methods of Hsu modifies the adaptive gain γ_H to become of the form $\epsilon/((1+NX^2)(1+\mu\theta^\alpha))$. The term $\mu\theta^\alpha$ is required in the convergence proof but the author observers that μ may be taken arbitrarily small and therefore such method can be approximated by setting $\mu = 0$. During the transient period, the normalising variable X^2 is dominated by the decaying exponential term (far from lock) and equals the true squared-magnitude of $x(t)$ when in lock. For frozen-parameter analysis, however, steady-state conditions are valid and $\theta \neq \omega_c$. Hence, X^2 then contains sinusoidal components at ω_c, and the update term has a factor $\sin^2/(1+a\sin^2)$. The average of this term is indeed obtainable by integration, but the result is algebraically complex.

Again, by simple algebraic manipulation, the updating law for λ can be simplified in

$$\frac{d}{dt}\lambda = \gamma\omega_0 \frac{1-\lambda^2}{1+\lambda^2}. \tag{4.68}$$

By considering the obtained relationships, it can be concluded that the approach in [46] should provide, for small γ, a response to changes in the input frequency which is independent of the amplitude A_c. Moreover the design produces transients which vary according to the frequency ω_c, i.e. faster as ω_c increases. In [17] a modification is proposed to set up α parameter to be 1 and μ to be chosen large enough so that $(1+\mu\theta)/\mu \approx \theta$). In this case

$$\frac{d}{dt}\lambda = \gamma \frac{\lambda(1-\lambda^2)}{1+\lambda^2}. \tag{4.69}$$

and now all the influencing parameters ω_c, A_c, ζ have been removed from the transient response.

4.3.1 ANFs for biased sinusoid input signal

A central task into the grid voltage monitoring problem is to limit the effects of the presence on an offset in the measured grid voltage. This offset is

typically introduced by the measurements and data conversion processes and causes errors for the estimated parameters of the grid voltage. As reported in [16], the error caused by the voltage offset has the same frequency as the utility voltage and low pass filtering effects are difficult to obtain due to the low error frequency. Therefore a trade-off between the time response performances and the filtering action must be taken into account. In [16] a structural modification of the SOGI system in presented in order to remove the offset term from the input data. A more interesting ANF scheme has been developed in [4] to estimate amplitude, frequency and bias of an input signal of the form

$$y(t) = A_0 + A_c \sin(\omega_c t + \phi_c). \tag{4.70}$$

The authors consider an auxiliary second-order filter to generate such a signal

$$\begin{cases} \dot{\varsigma}_1(t) = \varsigma_2(t), \\ \dot{\varsigma}_2(t) = -2\alpha\varsigma_2(t) - \alpha^2\varsigma_1(t) + y(t), \\ \varsigma(t) \ = \varsigma_1(t) \end{cases} \tag{4.71}$$

or

$$\varsigma(t) = \frac{1}{(p+\alpha)^2} y(t), \tag{4.72}$$

where p is differentiation operator and number $\alpha > 0$. It is easy to prove that the considered input signal can be obtained by

$$\dot{y}(t) = 2\alpha\ddot{\zeta}(t) + \alpha^2\dot{\zeta}(t) + \theta\dot{\zeta}(t) + \epsilon_y(t), \tag{4.73}$$

where $\epsilon_y(t)$ is exponentially decaying function of time caused by nonzero initial conditions.

Since the term $\epsilon_y(t)$ depends on parameter α, it is possible to accelerate convergence of $\epsilon_y(t)$ to zero by increasing α. By considering the above formulation, an adaptive identification of the unknown parameter θ identification can be easily obtained. The first step consists in assuming the function $\dot{y}(t)$ is measured. There, neglecting exponentially decaying item $\epsilon_y(t)$, ideal identification algorithm can be written in the following way

$$\dot{\hat{\theta}}(t) = k\dot{\zeta}(t)z(t) - k\dot{\zeta}^2(t)\hat{\theta}(t)) \tag{4.74}$$

and

$$\hat{\omega_c}(t) = \sqrt{\left|\hat{\theta}(t)\right|}, \tag{4.75}$$

where $z(t) = \dot{y}(t) - 2\alpha\ddot{\zeta}(t) - \alpha^2\dot{\zeta}(t)$ and $k > 0$. Consider estimation error of parameter θ as $\tilde{\theta}(t) \triangleq \theta - \hat{\theta}(t)$. By a computation of the time-derivative of this term, the following holds

$$\dot{\tilde{\theta}}(t) = -k\dot{\zeta}^2(t)\tilde{\theta}(t). \tag{4.76}$$

Solving such an equation, an expression of the estimation error with respect to time t can be derived as

$$\tilde{\theta}(t) = \tilde{\theta}(t_0)e^{-k\gamma(t,t_0)}, \tag{4.77}$$

where

$$\gamma(t,t_0) = \int_{t_0}^{t} \dot{\varsigma}^2(\tau)d\tau. \tag{4.78}$$

It is obvious that, as polynomial $(p+\alpha)^2$ is Hurwitz, function $\varsigma(t)$ takes the form

$$\varsigma(t) = \overline{A}_0 + \overline{A}_c \sin(\omega_c t + \overline{\phi}_c) + \Delta \tag{4.79}$$

where $\overline{A}_0, \overline{A}_c$ and $\overline{\phi}_c$ are constant coefficients depending on parameters of signal $y(t)$ and number α, and Δ is an exponentially decaying item, caused by transient. Neglecting such a term, it can be considered that $\dot{\varsigma}(t) = \overline{A}_c\omega_c \sin(\omega_c t + \overline{\phi}_c)$. Such formulation leads to

$$\gamma(t,t_0) = \gamma_0 t + \gamma_1(t,t_0) \tag{4.80}$$

where $\gamma_1(t,t_0)$ is a bounded function. Therefore

$$\tilde{\theta}(t) = \tilde{\theta}(t_0)e^{-k\gamma_0 t}e^{-k\gamma_1(t,t_0)}. \tag{4.81}$$

It is an immediate result to note that the convergence time is a function of the gain coefficient k that dictates the speed of the algorithm. A strong assumption has been made: the signal, and in particular its time-derivatives, must be measurable signals. If it not true, in [4] a more practical identification algorithm has been also proposed as

$$\begin{aligned}\dot{\chi}(t) = k\dot{\varsigma}(t)\left(-2\alpha\ddot{\varsigma}(t) - \alpha^2\dot{\varsigma}(t)\right) - k\dot{\varsigma}^2\hat{\theta}(t) \\ -k\ddot{\sigma}(t)y(t) - \overline{k}_a\hat{\theta}(t),\end{aligned} \tag{4.82}$$

and

$$\hat{\theta}(t) = \chi(t) + k\dot{\varsigma}(t) + k\dot{\varsigma}(t)y(t) \tag{4.83}$$

where ς is solution of system in Eq. (4.71) and $\overline{k}_a \geq 0$ is considered in order to prevent parameter estimated drift. Amplitude and offset estimator are also presented but it has been noticed [22] that the identification scheme behaviour is better if there is a roughly initial estimation of the unknown frequency. In the same way, $\overline{k}_a$ must be carefully tuned in order to not filter too much the signal similarly to α. All these considerations may be addressed in the case the magnitude of the unknown frequency is roughly known, what is common in practical applications. Moreover, amplitude and offset estimator should not be taken into account while not close to steady state.

5

SOGI methods for signal synchronization

5.1 Introduction

In this chapter SOGI systems are investigated to cope with the biased sinusoid signals case. The concept of the generalized integrator, namely **GI**, for sinusoidal signal was formally introduced in [93], where a simplified block with transfer function $2s/(s^2+\omega^2)$ was presented as a GI for single sinusoidal signals and it is the core unit of proportional-resonant (**PR**) controllers [87]. In the last decades, SOGI schemes have been largely studied in an very impressive application scenarios for power converters. Some applications have been proposed to obtain zero steady-state error using stationary frames in grid-converters applied to active rectifiers, active filters, uninterruptible power supplies and distributed generation. These integrators have been also included in algorithms of grid synchronization, detection of sequences, harmonic compensation, etc [75]. A system-on-chip harmonic detector, based on FPGA technology, has been proposed in [23] by using SOGI extensions, namely **DSOGI-QSG** (dual SOGI-quadrature signal generation) that permit to detect positive and negative sequences of a specified harmonic. Further modified GI structure can be found in [9]. By considering the amount of devoded literature, it is straightforward to understand that SOGI provides a powerful tools to completely analyse the waveforms of interest in more than one scenario and an important role is assumed by the adaptive SOGI scheme that are very useful to completely track an input sinusoid. In particular, the synthesis of an accurate method for the on line estimation of the entire parameters set for a biased sinusoidal signal represents a very attractive challenge. An impressive amount of works have been proposed to cope with this task until now. The majority of the recently published papers treat the most general case of multi-sinusoidal estimation problem [96, 44, 62, 66, 78, 14] but it is worth noting that several proposed techniques not cope with biased sinusoid. Such methods can not be adapted to deal with the problem discussed here and so the cases of singular sinusoid and singular biased sinusoid are widely investigated nowadays [15, 43, 11, 4]. In [43] a seventh-order global estimator for recov-

ering the frequency, amplitude and offset of a sinusoidal signal is presented. The estimator has global convergence property but it is not able to track the input signal since it does not estimate the initial phase angle. Moreover the presence of the quadratic term of the input signal may heavily affect the estimation in the case of noisy data. For the merely frequency estimation, a global adaptive estimator of order 2, 3, 4 and 5 is proposed in [43, 96, 66] and [62] respectively. In [11] a new approach to the problem of globally convergent frequency estimator is proposed where the estimator is represented by a fourth-order system for the case of biased sinusoidal signals. Based on previous results in [28], an estimation scheme, relying on OSG-SOGI, is presented in [29]. A continuous-time least-square algorithm is used for the estimation of both bias and frequency. The remaining parameters are obtained via simple relationships between the OSG-SOGI output signals. The exponential convergence of such an estimator is proved and the resulting estimator permits to track the unknown input signal with satisfactory accuracy. In [30], an adaptive method, that presents only a dynamic order equal to 4 is able to estimate the overall parameters set of a biased sinusoidal signal. Unlike method in [4], the approach presented in [30] permits to track the input signal as the one presented in [15]. As it is shown in the following sections, unlike method in [15], that requires an initial condition very close to the unknown frequency to be estimated, the OSG-SOGI method is more insensitive to initial conditions choice.

5.2 Adaptive-SOGI scheme

In [28] an averaging analysis for the adaptive law of the SOGI resonant frequency has been presented. To verify the stability property for the SOGI system, including the adaptive law and the offset-free property for the frequency estimation, the singular perturbation theory [51] has been used. The averaging method applies to a system of the form

$$\dot{x} = \gamma f(t, x, \gamma) \tag{5.1}$$

where γ is a small positive parameter and $f(t, x, \gamma)$ is a T-periodic function. The evolution of such a system is supposed to be determinate by two time-scaled dynamics: a fast oscillatory dynamic and a slow one due to the presence of parameter γ. The averaging method associates at the original system in Eq. (5.1) an autonomous average system

$$\dot{x} = \gamma f_{av}(x) \tag{5.2}$$

where

$$f_{av}(x) = \frac{1}{T} \int_0^T f(\tau, x, 0) d\tau. \tag{5.3}$$

Standard method may be employed to analyse the equilibrium points and their stability of such a system. Stability of the averaged and the original systems are related by the following theorem (see [51]).

Theorem 1. *Let $f(t, x, \gamma)$ and its partial derivatives with respect to (x, γ) up to the second order be continuous and bounded for $(t, x, \gamma) \in [0, \infty) \times D_0 \times [0, \gamma_0]$, for every compact set $D_0 \in D$, where $D \in \mathcal{R}^n$ is a domain. Suppose f is T-periodic in t for some $T > 0$ and γ is a positive parameter. Let $x(t, \gamma)$ and $x_{av}(\gamma t)$ denote the solutions for the original and averaged systems, respectively. Then*

- *If $x_{av}(\gamma t) \in D \ \forall t \in [0, b/\gamma]$ with finite $b > 0$ and $x(0, \gamma) - x_{av}(0) = \mathcal{O}(\gamma)$, then there exists $\gamma^* > 0$ such that for all $0 < \gamma < \gamma^*$, $x(t, \gamma)$ is defined and*

$$x(t, \gamma) - x_{av}(t, \gamma) = \mathcal{O}(\gamma) \quad \text{on } [0, b/\gamma]. \tag{5.4}$$

- *If the origin $x = 0 \in D$ is an exponentially stable equilibrium point of the average system in Eq. (5.2), $\Omega \in D$ is a compact subset of its region of attraction, $x_{av}(0) \in \Omega$, and $x(0, \gamma) - x_{av}(0) = \mathcal{O}(\gamma)$, then there exists $\gamma^* > 0$ such that for all $0 < \gamma < \gamma^*$, $x(t, \gamma)$ is defined and*

$$x(t, \gamma) - x_{av}(t, \gamma) = \mathcal{O}(\gamma) \quad \text{for all } t \in [0, \infty). \tag{5.5}$$

- *If the origin $x = 0 \in D$ is an exponentially stable equilibrium point of the average system in Eq. (5.2), then there exist positive constants γ^* and k such that, for all $0 < \gamma < \gamma^*$, the original system in Eq. (5.1) has a unique, exponentially stable, T-periodic solution $\overline{x}(t, \gamma)$ with the property $\|\overline{x}(t, \gamma)\| \leq k\gamma$.*

In [28] the resonant frequency is updated by the following

$$\dot{\omega}_s = -\gamma K_s \omega_s (v(t) - v_1(t)) v_2(t). \tag{5.6}$$

where γ is a positive constant. The adaptive system can be rewritten in state space as

$$\dot{\omega}_s = -\gamma K_s^2 \omega_s^3 \left(v(t) - K_s \omega_s x_2(t)\right) x_1(t), \tag{5.7}$$

$$\dot{x}_1(t) = x_2(t), \tag{5.8}$$

$$\dot{x}_2(t) = -\omega_s^2 x_1(t) - K_s \omega_s x_2(t) + v(t). \tag{5.9}$$

In order to move the equilibrium point to the origin in the state space, let consider the following positions

$$\omega_s = \omega_e + \omega_c, \tag{5.10}$$

$$x_1(t) = x_{1e} - \frac{A_c}{K_s \omega_c^2} \cos(\theta_c), \tag{5.11}$$

$$x_2(t) = x_{2e} + \frac{A_c}{K_s \omega_c} \sin(\theta_c), \tag{5.12}$$

where $\theta_c = \omega_c t + \phi_c$ and the second terms on the right-hand sides are the equilibrium solutions for the system in Eqs. (5.7)-(5.9).

By considering the error in frequency estimation $\sigma = \omega_s - \omega_c$, the relative Lyapunov function σ^2 is always positive and its derivative negative for positive values in the detected frequency ω_s. Eqs. (5.7)-(5.9) can be separated into two parts, a slow and a fast system:

$$\dot{\omega}_e = -\gamma f(t, \omega_e, x_e), \tag{5.13}$$

$$\dot{x}_e = g(t, \omega_e, x_e) \tag{5.14}$$

where

$$f(t, \omega_e, x_e) = -K_s \frac{(\omega_e + \omega_c)^3}{\omega_c^3} \left(K_s \omega_c^2 x_{1e} - A_c \cos(\theta_c)\right) \times \\ \times \left(K_s \omega_c \left(\omega_e + \omega_c\right) x_{2c} + A_c \omega_e \sin(\theta_c)\right) \tag{5.15}$$

and

$$g(t, \omega_e, x_e) = A_g x_e + \begin{bmatrix} 0 \\ \beta \sin\left(u - atan\left(\frac{2\omega_c + \omega_e}{K_s \omega_c}\right)\right) \end{bmatrix} \tag{5.16}$$

with

$$A_g = \begin{bmatrix} 0 & 1 \\ -(\omega_e + \omega_c)^2 & -K_s(\omega_e + \omega_c) \end{bmatrix}, \tag{5.17}$$

$$\beta = \frac{A_c \omega_e}{K_s \omega_c^2} \sqrt{K_s^2 \omega_c^2 + (2\omega_c + \omega_e)^2}. \tag{5.18}$$

The system in Eqs. (5.13)-(5.14) is a classical standard singular perturbation model of a finite-dimensional dynamical system. In the proposed adaptive control system, the term ω_e is the slow state variable, and x_e contains the fast state variables. The singular perturbation theory gives that under certain technical conditions, if the slow system (5.13) is stable and the fast system (5.14) is stable around the manifold $\overline{x}_e = \hat{g}(t, \omega_e)$ where $\overline{x}_e$ is the solution of $g(t, \omega_e, x_e) = 0$, then the overall system is stale for γ sufficiently small. Certainly there exists a neighbourhood B_{r1} of ω_c in which the matrix A_g is non-singular and it has its eigenvalues in the left half $s-$plane. Moreover $f(t, 0, 0) = 0$ and $g(t, 0, 0) = 0$ and the equation $g(t, \omega_e, x_e) = 0$ has an isolated root $\overline{x}_e = \hat{g}(t, \omega_e)$ such that $\hat{g}(t, 0) = 0$ where

$$\hat{g}(t, \omega_e) = -A_g^{-1} \begin{bmatrix} 0 \\ \beta \sin\left(u - atan\left(\frac{2\omega_c + \omega_e}{K_s \omega_c}\right)\right) \end{bmatrix}. \tag{5.19}$$

Thus, if $\dot{\omega}_e = f(t, \omega_e, \hat{g}(t, \omega_e))$ is also exponentially stable, that is, if the adaptation in Eq. (5.6) is exponentially stable, the origin of system (5.13)-(5.14) is exponentially stable for all $0 < \gamma < \gamma^*$. An alternative solution to (5.19) can be computed by using the steady-state SOGI output expression in

Eqs. (4.28)-(4.29), by assuming $\omega_e = \omega_s - \omega_c$. From Eq. (4.40), with $\omega_e = \omega_s - \omega_c$, the following equation holds:

$$\dot{\omega}_e = -\gamma f(t, \omega_e, \hat{g}(t, \omega_e)) \tag{5.20}$$

$$= -\gamma \hat{f}(t, \omega_e, x_e)\omega_e, \tag{5.21}$$

where

$$\hat{f}(t, \omega_e, x_e) = \frac{A_c^2 K_s^2 (\omega_e + \omega_c)^3 |2\omega_c + \omega_e| \sin(\theta_c + \overline{\phi})^2}{K_s^2 \omega_c^2 (\omega_e + \omega_c)^2 + \omega_e^2 (2\omega_c + \omega_e)^2}. \tag{5.22}$$

Note that the functions f, g and $\hat{g}$ and their partial derivatives are bounded for $|x_e - \hat{g}(t, \omega_e)| \in B_{r2}$, where B_{r2} is a neighbourhood of $\hat{g}(t, \omega_e)$. By considering the Lyapunov function $V(\omega_e) = \omega_e^2$, it follows that

$$\dot{V}(\omega_e) = -2\gamma \hat{f}(t, \omega_e, x_e)\omega_e^2 < 0, \omega_e > -\omega_c. \tag{5.23}$$

Let $\omega_s = \rho\omega_c$ then from Eq. (5.23) it follows that the system $\dot{\omega}_e = f(t, \omega_e, \hat{g}(t, \omega_e)$ is exponentially stable for $\rho > 0$ and the equilibrium point $(\omega_e = 0)$ is exponentially stable for γ sufficiently small. An analysis for the case of multi-sinusoidal signals has been conducted too, i.e. the input of the SOGI system has been considered to be equal to

$$v(t) = \sum_{i=1}^{m} A_{c_i} \sin(\theta_i), \qquad \text{with } \theta_i = \omega_{c_i} t + \phi_{c_i}. \tag{5.24}$$

A cascade of m-SOGI blocks has been considered and, with the assumption that the $i-$th SOGI system is tuned on the resonance frequency ω_{c_i}, with $i = 1, 2, \ldots$, then, in steady-state condition, its output is equal to $v_i(t) = A_{c_i} \sin(\omega c_i t + \phi_i)$. By taking advantages to the particular considered SOGIs-scheme, the following matrix equation is proved to hold:

$$A\overline{U} = \overline{Y}, \tag{5.25}$$

where

$$A(i, j) = \begin{cases} F_1^{(j)}(s), & i \neq j \\ 1, & i = j \end{cases} \tag{5.26}$$

$$\overline{U}(s) = \left[U_1(s), U_2(s), \ldots, U_m(s) \right]^T, \tag{5.27}$$

and

$$\overline{Y}(s) = \left[V_(s), V_(s), \ldots, V(s) \right]^T, \tag{5.28}$$

where the upper case $s-$notation stands for the Laplace transform of the related time-dependent signals. The matrix A can be factorized as

$$A = (M + uv^T), \tag{5.29}$$

where

$$M = diag\left\{1 - F_1^{(i)}(s)\right\}_{i=1,2,\ldots,m}, \tag{5.30}$$

$$u = [1, 1, \ldots, 1]^T \tag{5.31}$$

and

$$v = \left[F_1(s)^{(1)}, F_1(s)^{(2)}, \ldots, F_1(s)^{(m)}\right]^T. \tag{5.32}$$

By using the Sherman-Morrison's formula [37], one can obtain:

$$A^{-1} = M^{-1} - \frac{M^{-1}uv^TM^{-1}}{1 + v^TM^{-1}u} = Q_1 - \frac{1}{\lambda}Q_2, \tag{5.33}$$

where

$$Q_1 = diag\left\{\frac{1}{1 - F_1^{(i)}(s)}\right\}_{i=1,2,\ldots,m}, \tag{5.34}$$

$$Q_2(i,j) = \frac{F_1^{(j)}(s)}{(F_1^{(i)}(s) - 1)(F_1^{(j)}(s) - 1)}, \tag{5.35}$$

and

$$\lambda = 1 + \sum_{j=1}^{m} \frac{F_1^{(j)}(s)}{1 - F_1^{(j)}(s)}. \tag{5.36}$$

Therefore

$$U_i(s) = H(s)\frac{1}{1 - F_1^{(i)}(s)}Y(s), \quad i = 1, 2, \ldots, m, \tag{5.37}$$

with

$$H(s) = \frac{1}{1 + \sum_{j=1}^{m} \frac{F_1^{(j)}(s)}{1 - F_1^{(j)}(s)}}. \tag{5.38}$$

Since

$$\lim_{s \to \jmath\omega_k} F_1^{(i)}(s) = \begin{cases} 1, & i = k, \\ \jmath\frac{K_s\omega_i\omega_s}{(\omega_i^2 - \omega_k^2) + \jmath K_s\omega_i\omega_s}, & i \neq k, \end{cases} \tag{5.39}$$

it follows that

$$\lim_{s \to \jmath\omega_k} \frac{H(s)}{1 - F_1^{(i)}(s)} = \begin{cases} 1, & i = k, \\ 0, & i \neq k. \end{cases} \tag{5.40}$$

By the above analysis it follows that in the multi-SOGI system, the output of each SOGI tuned on the frequency of one component of the signal, converges exponentially fast to the corresponding sinusoidal component. The filter-bank possesses the desired quality that the enhanced outputs have the same magnitude and phase as the input spectral components. The SOGI-filter bank can be used to estimate the unknown parameters of a multi-sinusoidal signal. Here a signal composed by a sum of harmonics, i.e. with $v_i(t) = A_i \sin(i\overline{\omega}t + \phi_i)$ is considered. In this case, only the first SOGI is adapted while the others are tuned with multiple frequencies. Taking into account the structure of the

filter bank, the input to the first SOGI, after a transient period, assumes the form

$$u_1(t) = \sum_{k=1}^{m} A_k \, |H_1(\jmath k\overline{\omega})| \sin(k\overline{\omega}t + \phi_k + arg|H_1(\jmath k\overline{\omega}|), \tag{5.41}$$

where

$$H_1(s) = \frac{1}{1 - \sum_{i=1}^{m} \frac{F_1^{(i)}(s)}{1 - F_1^{(i)}(s)}} \frac{1}{1 - F_1^{(1)}(s)} \tag{5.42}$$

Moreover, the outputs of the first SOGI, namely $v_1^{(1)}(t)$ and $v_2^{(1)}(t)$, become

$$\begin{aligned} v_1^{(1)}(t) = \sum_{k=1}^{m} & A_k \, |H_1(\jmath k\overline{\omega})| \, |F_1^{(1)}(\jmath k\overline{\omega}| \times \\ & \times \sin(k\overline{\omega}t + \phi_k + arg[H_1(\jmath k\overline{\omega})] + arg[F_1^{(1)}(\jmath k\overline{\omega})]), \end{aligned} \tag{5.43}$$

and

$$\begin{aligned} v_2^{(1)}(t) = \sum_{k=1}^{m} & A_k \, |H_1(\jmath k\overline{\omega})| \, |F_2^{(1)}(\jmath k\overline{\omega}| \times \\ & \times \sin(k\overline{\omega}t + \phi_k + arg[H_1(\jmath k\overline{\omega})] + arg[F_1^{(1)}(\jmath k\overline{\omega})]), \end{aligned} \tag{5.44}$$

Substituting the expressions above into the updating law,

$$\omega_{s1} = -\gamma K_s \omega_{s1} \left(u_1(t) - v_1^{(1)}(t) \right) v_2^{(1)}(t) \tag{5.45}$$

and using the fact that

$$\begin{aligned} \xi(\omega_{s1}) = \frac{\overline{\omega}}{2\pi} \int_0^{\frac{2\pi}{\overline{\omega}}} \left(u_1(t) - v_1^{(1)}(t) \right) v_2^{(1)}(t) dt = \\ = \sum_{k=1}^{m} \frac{\frac{A_k^2}{2} |H_1(\jmath k\overline{\omega})|^2 |F_2^{(1)}(\jmath k\overline{\omega})|}{\sqrt{1 + \frac{k^2 K_s^2 \omega_{s1}^2 \overline{\omega}^2}{(\omega_{s1}^2 - k^2\overline{\omega}^2)^2}}}, \end{aligned} \tag{5.46}$$

it follows that the averaged system is

$$\dot{\omega}_{e1} = -\gamma K_s \omega_{e1} \xi(\omega_{e1} + \overline{\omega}), \tag{5.47}$$

whose origin $\omega_{e1} = 0$ is exponentially stable. Thus, by applying singular perturbation theory, the SOGI-filter bank including the proposed adaptive law is exponentially stable and ω_{sk} converges to $k\overline{\omega}$ for $k = 1, 2, \ldots, m$ exponentially for γ sufficiently small.

5.3 Biased sinusoid identification

5.3.1 SOGI Structural properties

In [31] a modification of the classical SOGI scheme has been proposed to deal with biased sinusoidal input signal of the form in Eq. (4.70) and the proposed scheme is reported in Figure 5.1.

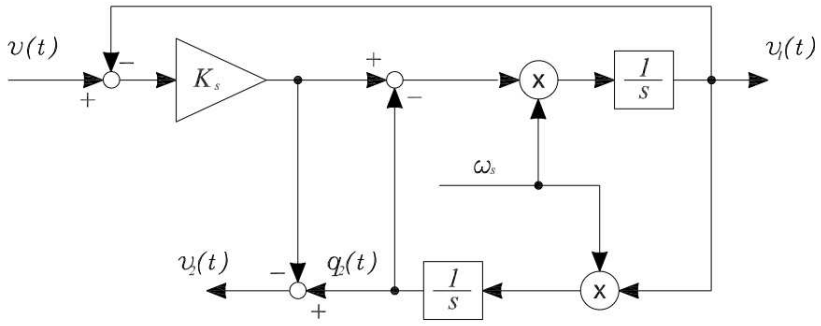

Fig. 5.1. Modified version of the classical SOGI scheme

By considering such a scheme, the transfer functions between the input signal $v(t)$ and the three output signals, $v_1(t)$, $v_2(t)$, and $q_2(t)$ respectively, become

$$F_1(s) = \frac{V_1(s)}{V(s)} = \frac{K_s\omega_s s}{s^2 + K_s\omega_s s + \omega_s^2}, \tag{5.48}$$

$$F_1(s) = \frac{V_2(s)}{V(s)} = -\frac{K_s s^2}{s^2 + K_s\omega_s s + \omega_s^2} \tag{5.49}$$

and

$$Z_2(s) = \frac{Q_2(s)}{V(s)} = \frac{K_s\omega_s^2}{s^2 + K_s\omega_s s + \omega_s^2}. \tag{5.50}$$

As it is evident by the transfer function $Z_2(s)$ the orthogonal component $q_2(t)$ is directly affected by the presence of any input signal offset, unlike $v_2(t)$ due to the presence of a double-derivative block in its transfer function expression. It is effortless to show that the output signals converge exponentially fast to the following steady-state signals:

$$v_{1\infty}(t) = m_1 A_c \sin(\omega_c t + \phi_c + \phi), \tag{5.51}$$

$$v_{2\infty}(t) = -m_3 A_c \cos(\omega_c t + \phi_c + \phi), \tag{5.52}$$

$$q_{2\infty}(t) = A_0 K_s - m_2 A_c \cos(\omega_c t + \phi_c + \phi). \tag{5.53}$$

The parameter m_3 is defined as

$$m_3 = m_1 \frac{\omega_c}{\omega_s}, \tag{5.54}$$

while the other parameters are the same as in Paragraph 4.2.3. An estimator for the input frequency ω_c, namely $\hat{\omega}_c$, can be performed as

$$\hat{\omega}_c = \omega_s \sqrt{\frac{v_{2\infty}(t)}{v_{2\infty}(t) + K_s(v(t) - v_{1\infty}(t) - A_0)}} \tag{5.55}$$

and it is worth to note that Eq. (5.55) needs of an estimate of the parameter A_0.

5.3.2 Non-adaptive SOGI estimation scheme

In [29] a non-adaptive OSG-SOGI system, for the case of biased sinusoid signals in input, has been largely investigated in continuous time mode.

Remark 1. Generally, the OSG-SOGI structure requires an adaptive tuning with respect to its resonance frequency. This can be achieved by adjusting the resonance frequency of the SOGI on-line using, for example, the frequency provided by the feedback control loop of a PLL structure as proposed in [15] or the frequency tracking method based on modulating functions. In [29], it has been shown that the unknown parameters can be estimated through the measurements of the OSG-SOGI output signals without any adaptation of the resonant frequency.

Estimation method

In the nominal case, i.e. when the input signal is not affected by noise, by Eqs. (5.52), (5.53) the following linear relationship can be obtained

$$y(t) = \phi^T(t)\theta^*, \tag{5.56}$$

where $\phi(t)$ is the regressor vector,

$$\phi(t) = \begin{bmatrix} q_{2\infty}(t) \\ -K_s \end{bmatrix}, \tag{5.57}$$

θ^* is the vector of unknown parameters

$$\theta^* = \begin{bmatrix} \omega_c^2 \\ A_0\omega_c^2 \end{bmatrix} \tag{5.58}$$

and

$$y(t) = \omega_s^2 v_{2\infty}(t). \tag{5.59}$$

To obtain the unknown vector θ^*, an estimate $\hat{\theta}(t)$ is computed by minimizing the cost function

$$J(\hat{\theta}) = \int_0^t e^{-\lambda(t-\tau)}\tau \left(\phi(\tau)\hat{\theta} - y(\tau)\right)^2 d\tau + \frac{1}{2}e^{-\lambda(t-\tau)} \left(\hat{\theta} - \theta\right)^T Q_0 \left(\hat{\theta} - \theta\right) \tag{5.60}$$

where $Q_0 = Q_0^T > 0$ and $\lambda \geq 0$ are design constans, $\hat{\theta}_0 = \hat{\theta}(0)$ is the initial parameters estimate and the linear term in the integrand function provides a zero-convergent estimation error in the nominal case, as explained in the following.

Setting $\partial J/\partial\hat{\theta} = 0$, the estimate that minimizes (5.60) is

$$\hat{\theta}(t) = P(t)\left[e^{-\lambda t}Q_0\hat{\theta}_0 + \int_0^t e^{-\lambda(t-\tau)}\tau\phi(\tau)y(\tau)d\tau\right] \tag{5.61}$$

with

$$P(t) = \left(e^{-\lambda t}Q_0\hat{\theta}_0 + \int_0^t e^{-\lambda(t-\tau)}\tau\phi(\tau)\phi^T(\tau)d\tau\right)^{-1}. \tag{5.62}$$

To achieve computational efficiency, it is desirable to compute $P(t)$ recursively. This amounts to replacing the above equation by the differential equation

$$\frac{dP^{-1}(t)}{dt} = -\lambda P^{-1}(t) + t\phi(t)\phi^T(t). \tag{5.63}$$

By using the identity

$$\frac{d}{dt}\left[P(t)P^{-1}(t)\right] = \frac{dP(t)}{dt}P^{-1}(t) + P(t)\frac{dP^{-1}(t)}{dt} = 0 \tag{5.64}$$

we obtain

$$\frac{dP(t)}{dt} = \lambda P(t) - tP(t)\phi(t)\phi^T(t)P(t). \tag{5.65}$$

Differentiating (5.61) and using (5.65), we find that the parameters update satisfies

$$\frac{d\hat{\theta}(t)}{dt} = -tP(t)\phi(t)\left(\phi^T(t)\hat{\theta}(t) - y(t)\right). \tag{5.66}$$

Let $\epsilon(t) = \hat{\theta}(t) - \theta^*$ be the estimation error, then it is straightforward to derive the following expression:

$$\epsilon(t) = -\epsilon P^{-1}(t)\theta^*. \tag{5.67}$$

To investigate the convergence properties of the proposed estimator, an important result has been reported in [29]. It has been demonstrated, in fact, that, as $t \to \infty$, the norm of the matrix $P^{-1}(t)$ is unbounded. The proof is an immediate results of the aforementioned relationship. The inequality

$$P^{-1}(t) \geq e^{-\lambda\delta}\int_{t-\delta}^t \tau\phi(\tau)\phi^T(\tau)d\tau \tag{5.68}$$

holds with $\delta \in (0, t]$ because of the non-negative definition of the integrand function.

Solving the integral in Eq. (5.68) with $\delta = \frac{2\pi}{\omega_c}$, one has

$$P^{-1}(t) \geq e^{-\lambda \frac{2\pi}{\omega_c}} \left(\left(t - \frac{\pi}{\omega_c} \right) M_1 + \frac{A_c m_2 \pi}{\omega_c^2} \sin(\rho(t)) M_2 \right) \tag{5.69}$$

where

$$M_1 = \frac{2\pi}{\omega_c} \begin{bmatrix} A_0^2 K_s^2 + \frac{1}{2} m_2^2 A_c^2 & -A_0 K_s^2 \\ -A_0 K_s^2 & K_s^2 \end{bmatrix}, \tag{5.70}$$

$$M_2 = \begin{bmatrix} -4A_0 K_s + m_2 A_c \cos(\rho(t)) & 2K_s \\ 2K_s & 0 \end{bmatrix} \tag{5.71}$$

and $\rho(t) = \omega_c t + \xi_c + \xi$.

Note that M_1 is a constant symmetric positive definite matrix, moreover each element of M_2 is bounded. Therefore the Frobenius norm of $P_\phi(t)$ tends to infinity as $\mathcal{O}(t)$.

As an immediate consequence of previous results, the norm of the relative error, i.e.

$$||\epsilon(t)|| \leq \frac{e^{-\lambda t}}{||P^{-1}(t)||} ||P^{-1}(0)\epsilon(0)|| \tag{5.72}$$

tends to zero exponentially.

If the signal $v(t)$ is corrupted by additional bounded disturbance, namely $w(t)$, the noise affects both the regressors and the signal $y(t)$. However the noise present in the output signals is bounded due to the filtering characteristics of the OSG-SOGI system. In such a case the error estimation is expressed as

$$\epsilon(t) = \bar{P}(t)\epsilon_n \tag{5.73}$$

where ϵ_n depends on the noise $w(t)$ as

$$\epsilon_n = \int_0^t e^{-\lambda(t-\tau)} \tau \bar{\phi}(\tau) w(\tau) d\tau \tag{5.74}$$

where the bar notation stands for noisy variables.

By similar arguments, the norm of $\bar{P}^{-1}(t)$ tends to infinity as $\mathcal{O}(t)$. Moreover

$$||\epsilon_n|| \leq ||\bar{\phi}|| ||w|| \frac{\lambda t + e^{-\lambda t} - 1}{\lambda^2}. \tag{5.75}$$

Therefore $||\epsilon_n||$ tends to infinity in $\mathcal{O}(t)$ time and, as a consequence, the boundedness of the estimation error norm can be guaranteed. Given the estimate of A_0 and ω_c, the amplitude A_c is estimated as

$$\hat{A}_c(t) = \sqrt{\frac{v_{1_\infty}^2(t) + \frac{\hat{\omega}_c(t)^2}{\omega_s^2} \zeta(t)^2}{m_1^2}}$$

where $\zeta(t) = q_{2_\infty}(t) - K_s \hat{A}_0(t)$. Moreover the phase angle of the sinusoidal signal can be estimated as

$$\hat{\rho}(t) = arg\left(\eta(t)\right) - \xi,$$

with

$$\eta(t) = -\frac{\hat{\omega}_c(t)^2}{\omega_s^2}\zeta(t) + \jmath\frac{\hat{\omega}_c(t)}{\omega_s}v_{1_\infty}(t).$$

5.3.3 Adaptive SOGI estimation scheme

OSG-TOGI properties

An innovative scheme that requires only a 4−th order system to completely track the input sinusoid unlike the 7−th order system presented in [29] has been proposed in [30]. The presented OSG-TOGI structure is depicted in Figure 5.2.

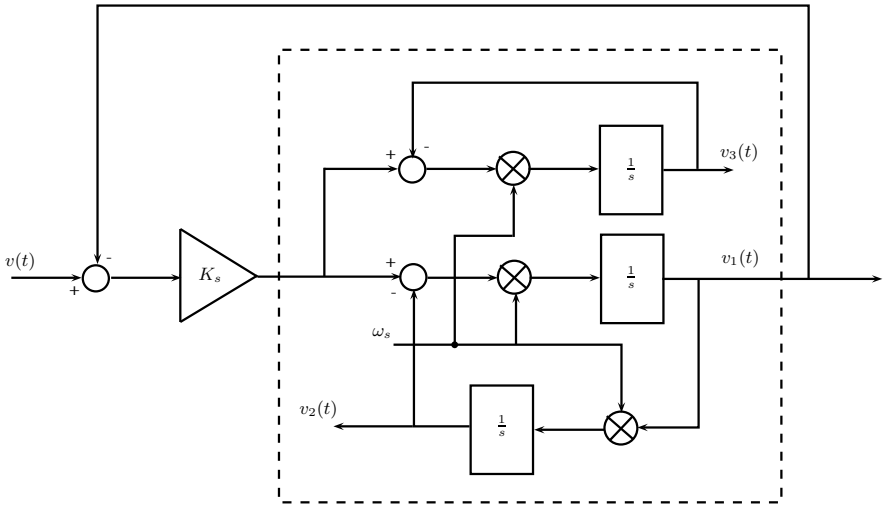

Fig. 5.2. Block diagram of the Orthogonal Signals Generator based on TOGI.

Output signals $v_1(t)$, $v_2(t)$ and $v_3(t)$ are related to the input one $v(t)$ by the following transfer functions

$$F_1(s) = \frac{V_1(s)}{V(s)} = \frac{K_s\omega_s s}{s^2 + K_s\omega_s s + \omega_s^2}, \tag{5.76}$$

$$F_2(s) = \frac{V_2(s)}{V(s)} = \frac{K_s\omega_s^2}{s^2 + K_s\omega_s s + \omega_s^2}, \tag{5.77}$$

and

$$F_3(s) = \frac{V_3(s)}{V(s)} = \frac{K_s\omega_s\left(s^2 + \omega_s^2\right)}{\left(s + \omega_s\right)\left(s^2 + K_s\omega_s s + \omega_s^2\right)}, \tag{5.78}$$

where $V_1(s), V_2(s)$ and $V_3(s)$ represents the Laplace transform of the signals $v_1(t), v_2(t)$ and $v_3(t)$ respectively while $V(s)$ is the Laplace transform of the input signal $v(t)$. An immediate result is that, in steady-state conditions, the signal $v_1(t)$ converges to an unbiased sinusoid, due to the derivative term in $F_1(s)$, unlike signals $v_2(t)$ and $v_3(t)$ that are both affected by a bias term, as it can be proved by an investigation on the transfer functions in Eqs. (5.76)-(5.78). The latter filter, represented by transfer function $F_3(s)$, is a proper notch filter with a band stop centered at w_s. Eq. (5.78) reveals that the filter gain at the frequency ω_s is equal to zero, i.e. $|F_s(j\omega_s)| = 0$. This fact implies that every sinusoidal input term with frequency equal to the resonant one is completely removed. As a consequence, an adaptation of the resonant frequency to the unknown one ω_c means a complete filtering of the signal $v(t)$ that results in a constant $v_3(t)$ signal depending on the bias term. For the proposed OSG-TOGI with the controller parameters $K_s, \omega_s > 0$, the output signals converge exponentially fast to the following quantities

$$v_{1\infty}(t) = m_1 A_c \sin(\omega_c t + \phi_c + \phi), \tag{5.79}$$

$$v_{2\infty}(t) = K_s A_0 - m_1 A_c \frac{\omega_s}{\omega_c} \cos(\omega_c t + \phi_c + \phi) \tag{5.80}$$

and

$$\begin{aligned} v_{3\infty}(t) = K_s A_0 - K_s A_c \omega_s \sqrt{\frac{1-m^2}{\omega_s^2 + \omega_c^2}} sign[\omega_s - \omega_c] \\ \times \cos\left(\omega_c t + \phi_c + \phi - \arctan\left(\frac{\omega_c}{\omega_s}\right)\right) \end{aligned} \tag{5.81}$$

where the parameters have the usual meaning. If the resonant frequency is tuned on the unknown input one, then the signal $v_{1\infty}(t)$ coincides with the unbiased sinusoid in input, $v_{2\infty}(t)$ is a biased sinusoidal signal with a phase shift of $\pi/2$ with respect to $v_{1\infty}(t)$ and finally $v_{3\infty}(t)$ represents the offset term of $v_{2\infty}(t)$. In such a case, OSG-TOGI output signals assume the following form

$$v_{1\infty}(t) = A_c \sin(\omega_c t + \phi_c), \tag{5.82}$$

$$v_{2\infty}(t) = K_s A_0 - A_c \cos(\omega_c t + \phi_c) \tag{5.83}$$

and

$$v_{3\infty}(t) = K_s A_0. \tag{5.84}$$

This idea suggests a simple method for biased sinusoidal signal estimation. An adaptive tuning of the OSG-TOGI resonant frequency, in fact, permits to obtain a set of three signals, as reported in Eqs. (5.82)-(5.84), that provide all the required informations to track the input $v(t)$. Moreover the aforementioned OSG-TOGI filtering properties permit to cope with noises that are eventually present in the input channel.

Adaptive tuning of the TOGI resonant frequency

The adaptive resonant frequency law for the OSG-TOGI system in [30], together with its exponential stability property, is here investigated. In Figure 5.3, the overall scheme based on OSG-TOGI is depicted where, in order to achieve an on-line estimation of all the unknown parameters, the following adaptive tuning law for the resonant frequency of the OSG-TOGI is proposed

$$\dot{\omega}_s = \gamma \left(v(t) - v_1(t) - \frac{v_3(t)}{K_s} \right) (v_3(t) - v_2(t))\, \omega_s. \tag{5.85}$$

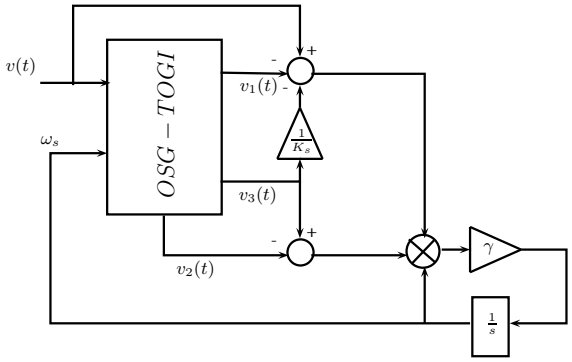

Fig. 5.3. Overall OSG-TOGI scheme.

For small enough values of γ, with $\gamma > 0$, it is possible to proof the exponential convergence property of such a law by using the averaging theory [51]. Once ω_s reaches its equilibrium point, i.e. ω_s is tuned on ω_c, the bias term can be estimated as (see Eq. (5.84))

$$\hat{A}_0 = \frac{v_{3\infty}(t)}{K_s}. \tag{5.86}$$

Moreover, by considering the signal

$$\xi(t) = v_{3\infty}(t) - v_{2\infty}(t) + jv_{1\infty}(t), \tag{5.87}$$

the unknown amplitude A_c and the phase angle $\Theta(t) = \omega_c t + \phi_c$ are estimated respectively as

$$\hat{A}_c = |\xi(t)|\,, \tag{5.88}$$

$$\hat{\Theta}(t) = arg\xi(t). \tag{5.89}$$

Stability analysis

At the limiting case $\gamma \to 0$, the resonant frequency ω_s can be assumed frozen. Therefore it is possible to consider the steady state signals $v_{1\infty}(t)$, $v_{2\infty}(t)$ and $v_{3\infty}(t)$ instead of $v_1(t)$, $v_2(t)$ and $v_3(t)$ respectively in Eq. (5.85). Therefore, the averaging method, applied to the adaptive law (5.85), provides the averaged system

$$\dot{\omega}_{s,av} = -\frac{\gamma}{2} A_c^2 m_{av} \sqrt{1 - m_{av}^2} \text{sign}[\omega_{s,av} - \omega_c] \frac{\omega_c \omega_{s,av}^2}{\omega_c^2 + \omega_{s,av}^2} \tag{5.90}$$

where the notation m_{av} stands for the expression of m when ω_s is replaced by $\omega_{s,av}$. To prove the stability of the averaged system, a candidate quadratic Lyapunov equation is

$$V(\omega_{s,av}) = (\omega_{s,av} - \omega_c)^2 . \tag{5.91}$$

From Eq. (5.91), it follows that

$$\dot{V}(\omega_{s,av}) = -\gamma A_c^2 m_{av} \sqrt{1 - m_{av}^2} |\omega_{s,av} - \omega_c| \frac{\omega_c \omega_{s,av}^2}{\omega_c^2 + \omega_{s,av}^2}. \tag{5.92}$$

$\dot{V}(\omega_{s,av})$ is negative definite for all possible values of $\omega_{s,av}$. Therefore for all initial condition $\omega_{s,av} > 0$ the stability of the averaged system is proved and, by the statement of Theorem 1, the original system has the exponentially stable solution $\{v_{1,\infty}, v_{2,\infty}, v_{3,\infty}, \omega_c\}$.

5.4 Numerical simulation

Some significant simulation are conducted in order to highlight the properties of the discussed SOGI-based methods.

5.4.1 Non-adaptive SOGI estimation scheme

The discussed non-adaptive scheme in [29] is here considered. Input signals, sampled with a period of $T_s = 3 \times 10^{-4} s$, are affected by a zero mean Gaussian noise with a signal-to-noise (SNR) ratio equal to 10. The SNR is measured in decibels as the logarithm of the average power of the reference signal samples, namely $y(t)$, and the noise ones, namely $w(t)$, over the experiment time as

$$SNR \triangleq 10 \log_{10} \frac{\sum_{k=0}^{n-1} y(kT_s)^2}{\sum_{k=0}^{n-1} w(kT_s)^2}, \tag{5.93}$$

where n is the number of samples.

Example 1. The aim of this example is to highlight the capability of the method in [29] to identify all the parameters of a biased sinusoid and then to on-line reconstruct the input signal. The biased sinusoid The input signal is the following

$$y(t) = 1 + 5\sin(3t + \frac{\pi}{4})$$

is considered as OSG-SOGI input signal. The parameters of the method are chosen as $K_s = 1$, $\lambda = 10$, $Q_0 = \frac{1}{\lambda}\mathcal{I}$, $\hat{\theta}_0 = [\omega_s^2, \omega_s^2]^T$ and ω_s is chosen equal to twice the unknown angular frequency initial value. Figure 5.4 depicts the noisy input signal, the nominal and the reconstructed one. As it can be noted the OSG-SOGI method seems to show fast and accurate signal reconstruction capability and a good rejection to noise.

The OSG-SOGI parameters are $K_s = 1$ and ω_s is chosen equal to half of the unknown frequency initial value. The forgetting factor is chosen equal to $\lambda = 100$

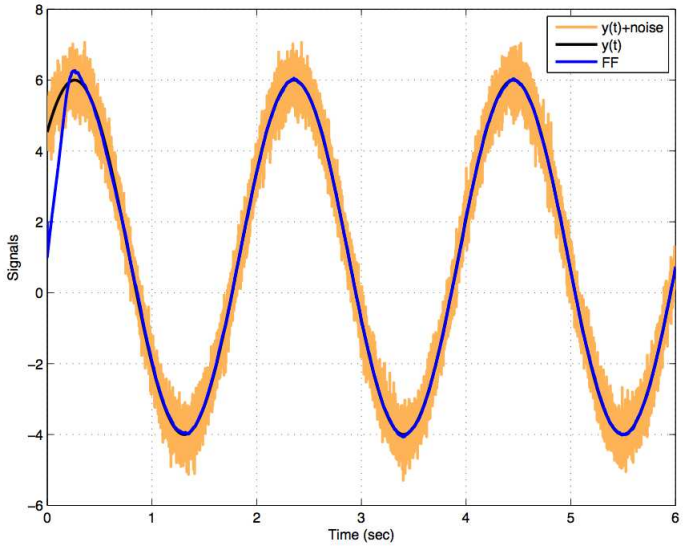

Fig. 5.4. Example. Signal reconstruction

Example 2. In this example, a signal with two frequency steps is used to compare the method in [29] with the CTA and ABKNS methods. Let us assume an input signal $v(t) = 2 + 2\sin(\omega_c t)$ with

$$\omega_c = \omega_c(t) = \begin{cases} 4,\ 0 \leq t < 20, \\ 8,\ 20 \leq t < 40 \\ 2,\ 40 \leq t < 60. \end{cases}$$

All the methods are initialized with the same initial condition $\hat{\omega}_c(0) = 3.2$. The parameters of the Fedele method are chosen as $K_s = 1, \omega_s = \hat{\omega}_c, \lambda = 1, Q_0 = \frac{1}{\lambda}\mathcal{I}$ and $\theta_0 = [\omega_s^2, \omega_s]^T$. CTA method is tuned with $k = 1, \omega = \hat{\omega}_c(0)$ and the PI regular gains $K_p = 1.51$ and $K_I = 0.89$. As far as ABKNS method is concerned, the chosen parameters are $k = 10, \alpha = 1$ and $\theta_0 = 5$. The results are reported in Figure 5.5.

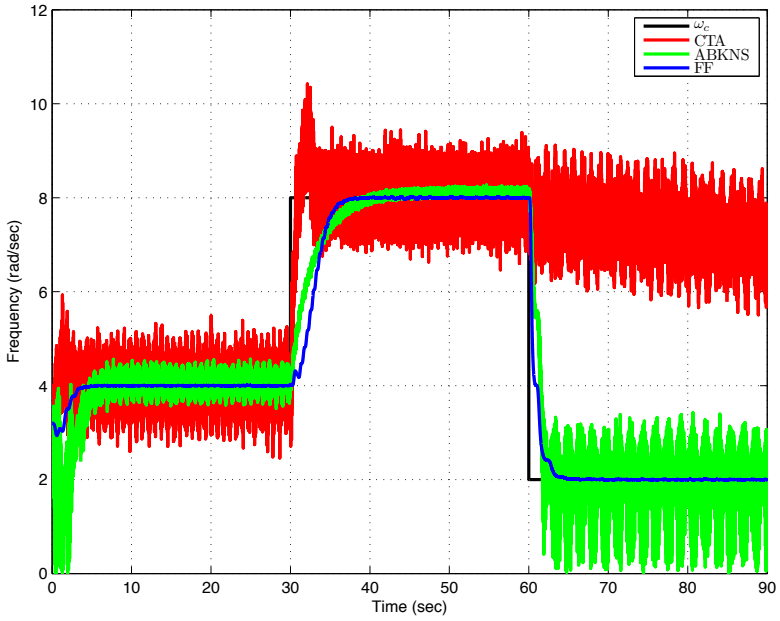

Fig. 5.5. Example 2. Frequency step

As shown in Figure 5.5 the frequency estimation provided by the OSG-SOGI method reaches the reference value with satisfactory precision. The PLL completely tracks the first step but it falls when the new steady state condition is the 25% of the present one. Unlike PLL, SOGI scheme tracks both the steps in a satisfactory manner and, in comparison with the filter in [4] indicated as AKBNS, it seems provide a more robustness property.

5.4.2 Adaptive-SOGI estimation scheme

The cases of frequency step, frequency sweep and voltage sag have been considered. Input signals, sampled with a period of $T_s = 10^{-6}s$, are affected by two sources of noise: the harmonic signal $0.01\sin(2\pi 150t)$ and a Gaussian noise with zero mean and standard deviation equal to 0.01. To put in evidence the performances of the method in [30], a comparison with PLL- based

estimation technique proposed in [16], namely **CTA**, and the linear scheme AKBNS, has been provided. The adaptive SOGI method is indicated as **FF** method. The PI controller depends on the gain parameters K_i and K_p while the orthogonal system generator is based on a modified version of standard SOGI structure that is able to deal with biased sinusoid and characterized by gain K_{PLL} and resonant frequency ω. For all the cases, the OSG-TOGI parameters are $K_s = 1$ and $\gamma = 100$. The PLL-based method is tuned with the following parameters $K_{PLL} = 1, K_i = 986.96$ and $K_p = 62.83$. The parameters $K_b = 10^8, \alpha = 6 \times 10^2$ and $\theta_0 = 10^5$ are chosen for the ABKNS technique.

Frequency step. The first experiment deals with the input signal

$$v(t) = 1 + \sin\left(2\pi f_c(t)t + \frac{\pi}{4}\right),$$

where the frequency $f_c(t)$ is defined as

$$f_c(t) = \begin{cases} 47, 0 \leq t < 0.4, \\ 52, 0.2 \leq t < 0.8. \end{cases}$$

The same initial condition for all the methods is $\omega_s(0) = 266\ rad/s$. As shown in Figure 5.6 the frequency estimation of the OSG-TOGI method reaches the reference value with satisfactory precision. The noise heavily affects the estimates of CTA and ABKNS methods while FF is characterized by a better filtering action on the input signal.

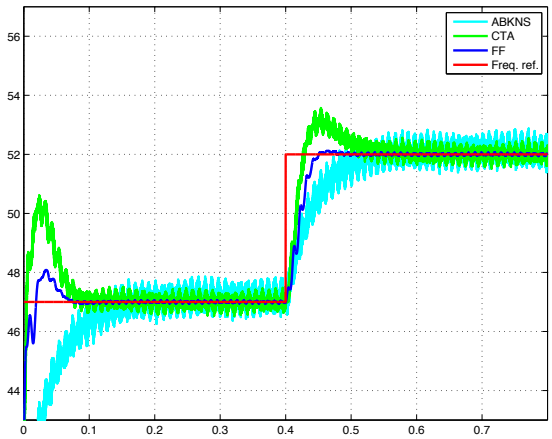

Fig. 5.6. Example 1. Frequency step case.

Frequency sweep. In this simulation the case of frequency sweep has been considered. The input signal is the following

$$v(t) = sin\left(2\pi f_c(t)t + \frac{\pi}{4}\right) \tag{5.94}$$

where the frequency is defined as

$$f_c(t) = \begin{cases} 50, & 0 \leq t < 0.2667, \\ 3.75t + 49, & 0.2667 \leq t < 0.5333, \\ 51, & 0.5333 \leq t < 0.8. \end{cases}$$

The initial choice of $\omega_s(0) = 283\, rad/s$ has been done for all methods. Also in this case, as depicted in Figure 5.7 the proposed method performs a better filtering action on the estimated frequency with respect to other methods. Note however that the filtering characteristics of CTA and AKBNS methods can be improved by increasing the gain parameters at the expense of longer transient periods. The tuning must be carefully done in order to not filter too much the input signal so a trade-off between filtering action and estimation response must be taken into account.

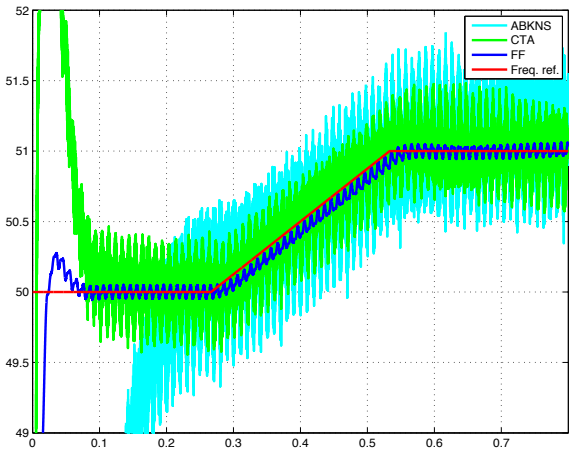

Fig. 5.7. Example 2. Frequency sweep case.

Voltage sag. The last simulation is devoted to the voltage sag case. The methods are initialized by choosing $\omega_s(0) = 565\ rad/s$. The input signal is the following

$$v(t) = 1 + A_c(t) \sin\left(2\pi 100t + \frac{\pi}{4}\right).$$

where

$$A_c(t) = \begin{cases} 1, & 0 \leq t < 0.16, \\ -2.5t + 1.4, & 0.16 \leq t < 0.32, \\ 0.6, & 0.32 \leq t < 0.48, \\ 2.5t - 0.6, & 0.48 \leq t < 0.64, \\ 1, & 0.64 \leq t < 0.8. \end{cases}$$

The results are depicted in Figure 5.8

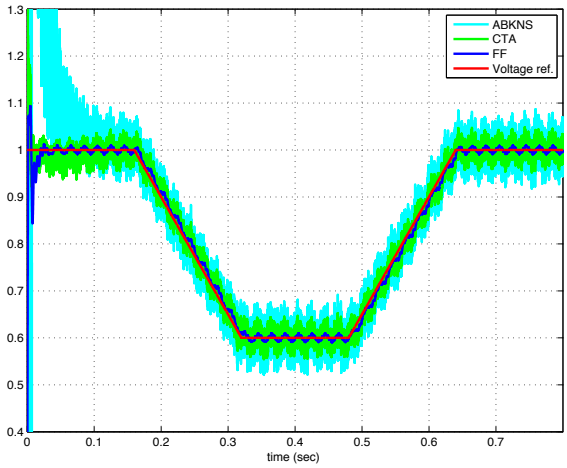

Fig. 5.8. Example 2. Voltage sag case.

6

Conclusions

In this thesis, several problems arising in the power conversion system area have been covered. Power conversion is assuming a central role in the modern research trends due to the growing world energy requests. In particular, this work has treated the efficiency and the synchronization problems that affect the conversion systems. The efficiency problems has been analysed in terms of switching losses reduction and pre-filtered total harmonic distortion optimization. As far as switching losses are considered, it has shown that such losses are linearly dependent with the working switching frequency: the more switching frequency, the more switching losses. An innovative output signal has been presented that is a piece-wise constant signal with an unique centered zero-level. The most interesting property is that such zero-duration is adjustable according to achieve some power quality targets. Such a signal requires only three communications to be generated in a single period unlike the standard PWM techniques that require greater switching frequencies. Another interesting property that has been investigated is related to the range of THD values that the considered signal can assume. It has been proved that an oculate choice of the zero-level duration permits to obtain THD values that are less than the corresponding PWM ones. An LC filter has been also presented to regulate the output amplitude to a desired level and to guarantee that the system is insensitive to any possible filter components variations. Regarding the synchronization problems, new approaches have been proposed that are based on second-, or third-, order generalized integrators. The obtained schemes have been shown to be simpler and more efficient than the standard techniques based on PLL. SOGI synchronizer are more insensitive with respect to the initial conditions than the PLL ones and they can completely track the unknown input signal unlike the approaches based on adaptive notch filters. The case of biased sinusoid signal, often arising in the grid-connected devices, has been also covered. Adaptive or non-adaptive SOGI-schemes have been discussed that permit to reconstruct the input signal even with the presence of bias term. Numerical simulations confirm the very attractive properties of such estimation schemes.

Acknowledgements

There are so many people that I have to thank and that are very important for me but the first I have to thank is my colleague, Edoardo Serra. Thanks to him I remembered to do my final thesis requirements so, without our conversation, this thesis would probably come out next year. Therefore, thank you so much.The second person I want to thank is Giuseppe Fedele. This thesis is the result of my collaboration with him and I must admit that his reprimands have helped me to grow up. Thanks for what you have done for me. Thank to my supervisor, Prof. Alfredo Eisinberg, to have given me the opportunity to attempt a PHD course too and thanks to the DEIS staff for their kindness and their availability. Thanks to my parents: in my life there are three or four constants and you are one of them. In everything I will do in my life, I know that you will be always on my side. Thank you for your love and your patience. One day I hope I will be a parent like you. Thanks to Annalisa. You have probably the worst temper I have ever met. You are moody and patience-consuming. Thank to you I known what hypochondria means. However you have the most lovely smile I have ever seen. I cannot tell you anything bad and simply, thank you for all. Thanks to my friends, Roberto and Stefano Truzzolillo. You are the best friends I could ever deserve. Clever and funny. They have always been with me in the most of my adventures.Thank you! I am very glad that you call me friend. Thanks to Eugenio: I hope this thesis can be as rigorous as Eugenio Pino but I known that it is impossible to beat him. Thanks to Claudio: you are probably the most dangerous and craziest man I ever met in my life. In this thesis there is a little piece of all the people I met. In good and bad times, all of you have influenced me: Pietro, Luca, Andrea, Antonello, Giuseppe, Mario, Serafino, Massimiliano, Maurizio, Francesco, Piero, Enrico, Raffaele, Alessandro, Domenico, Corrado, Nicola, Antonio, Francesca, Claudia, Cristina, Chiara, Dora, Roberta, Franco, Fabrizio, Enrico, Giovanni, Sergio, Alfredo and so on. A special thanks to Filippo Foglia because of his friendship. Lastly, I want to thank you for what you have done in my life. I am what I am because of your friendship. I have always tried to get the best from all you: our conversations, our experiences, even a "good

day". All of you gave me a lot.You are the solely responsible for what I have become. Thank you so much.

References

1. J.P. Agrawal, *Power electronics systems*, Prentice Hall, 2001.
2. O. Al-Naseem, R.W. Erickson, and P. Carlin, "Prediction of switching loss variations by averaged switch modelling", *IEEE App. Power Elect. Conf., APEC*, pp. 242-248, 2000.
3. M.H. Antchev, *Technologies for Electrical Power conversion, Efficiency, and Distribution: Methods and Processes*, Engineering Science Reference, 2009.
4. S. Aranovskiy, A. Bobtsov, A. Kremlev, N. Nikolaev, and O. Slita, *Identification of frequency of biased harmonic signal*, Eur. J. on Control, vol. 2, pp. 129-139, 2010.
5. S.C. Bansal, and U.M. Rao, "Evaluation of PWM inverter schemes", *Proc. on Inst. of Elect. Eng, PIEE.*, pp. 328-334, 1978.
6. G. Bartolini, A. Pisano, and E. Usai, *First and second derivative estimation by sliding mode technique*, J. Sig. Proc., vol. 4, no. 2, pp. 167-176, 2000.
7. S. Bernet, *State of the art and developments of medium voltage converters – An overview*, Elect. Rev., vol. 82, no.5, pp. 1-10, 2006.
8. R.E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, McGraw-Hill, 1999.
9. E. Blanco, E. Bueno, F. Espinosa, S. Cobreces, F.J. Rodriguez, and M.A. Ruiz, "Fast harmonics compensation in VCSs connected to the grid by synchronous-frame generalized integrators", *IEEE Proc. on Ind. Elec., ISIE*, pp. 751-755, 2005.
10. V. Blasko, "A hybrid PWM strategy combining modified space vector and triangle comparison methods", *Power Elect. Spec. Conf., PESC*, pp. 1872-1878,1996.
11. A.A. Bobtsov, *New approach to the problem of globally convergent frequency estimator*, Int. J. of Adapt. Contr. and Sig. Proc., vol. 22, no. 3, pp.306-317, 2008.
12. M. Bodson, and S.C. Douglas, *Adaptive algorithms for the rejection of sinusoidal disturbances with unknwon frequency*, Automatica, vol. 33, no. 12, pp. 2213-2221, 1997.
13. H.W. van der Broek, H.C. Skudelny, and G.V. Stanke, *Analysis and realization of PWM based on voltage space vectors*, IEEE Trans. on Ind. App., vol. 24, no.1, pp. 142-150, 1988.
14. X. Chen, *Identification for a signal composed of multiple sinusoids*, IET Contr. Th.&App., vol. 2, no. 10, pp. 875-883, 2008.

15. M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator", *Power Elect. Spec. Conf., PESC*, pp.1-6,2006.
16. M. Ciobotaru, R. Teodorescu, and V. Agelidis, "Offset rejection for PLL based synchronization in grid-connected converters", *IEEE App. Power Elect. Conf., APEC*, pp.1611-1617, 2008.
17. D.W.Clarke, *On the design of adaptive notch filters*, Int. J. of Adapt. Contr. and Sig. Proc., vol. 15, no. 7, pp. 715-744, 2001.
18. V.D. Colli, P. Cancellieri, F. Marignetti, and R. Di Stefano, *Voltage control of current source inverters*, IEEE Trans on E. Conv. , vol. 21, no. 2, pp. 451-458, 2006.
19. J.A. Crawford, *Advanced phase-lock techniques*, Artech House, 2008.
20. M. Crea, A. Eisinberg, G. Fedele, A. Ferrise, D. Frascino, *Automatic zero interval regulation for DC/AC conversion*, Patent request No. CZ2009A00007, 2009.
21. P.A. Dahono, T. Kataoka, and T. Sato, "Dual relationships between voltage-source and current-source three-phase inverters and its applications", *Proc. on Pow. Ele. and Drive Sys.*, pp. 559-565, 1997.
22. G. Damm, S. Aranovskiy, A. Bobtsov, A. Kremlev, N. Nikolaev, and O. Slita, *Discussion on Identification of frequency of biased harmonic signal*, Eur. J. on Control, vol. 2, pp. 140-143, 2010.
23. M.J. Diaz, E. Bueno, R. Mateos, F.J. Rodriguez, and E. Monmasson, "FPGA implementation of harmonic detector based on Second Order Generalized Integrators", *IEEE Conf. on Ind. Elec.*, pp.2453-2458, 2008.
24. A. Eisinberg, G, Fedele, A. Ferrise, and D. Frascino, *On an integral representation of a class of Kapteyn (Fourier-Bessel) series: Kepler's equation, radiation problems and Meissel's expansion*, App. Math. Letters, vol. 23, no. 11, pp. 1331-1335, 2010.
25. EN50160, *Voltage Characteristics of Electricity Supplied by Public Distribution Systems*, European Standard EN50160, CENELEC, 1994.
26. R. W. Erickson, and D. Maksimovic, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2004.
27. G. Fedele, *Amplitude, frequency and phase observer of a sinusoid using a second-order generalized integrator*, submitted.
28. G. Fedele, A. Ferrise, and D. Frascino, "Multi-sinusoidal signal estimation by an adaptive SOGI-filters bank", *15th Symposium on Sys. Iden, IFAC.*
29. G. Fedele, and A. Ferrise, *Non adaptive second order generalized integrator for PLL systems*, submitted.
30. G. Fedele, and A. Ferrise, "An adaptive quasi-notch filter for a biased sinusoidal signal estimation", *9th IEEE Int. Conf. on Cont. Aut., ICCA*, 2011.
31. G. Fedele, A. Ferrise, and D. Frascino, "Structural properties of the SOGI system for parameters estimation of a biased sinusoid", *9th Int. Conf. on Env. and Elec. Eng.*, 2010.
32. F.D.F. Fernandez1, *Contributions to Grid-Synchronization Techniques for Power Electronic Converters*, PhD thesis, Electronic Technology Department, Vigo University,2009.
33. S. D. Freeland, *A unified analysis of converters with resonant switches*, PhD Thesis, California Institute of Technology, 1988.
34. E. F. Fuchs, and M. A. M. Masoum, *Power Quality in Power Systems and Electrical Machines*, Elsevier Inc., 2008.

35. M. Karimi-Ghartemini, H. Karimi, and R. Iravani, *A Magnitude/Phase-Locked Loop System Based on Estimation of Frequency and In-Phase/Quadrature-Phase Amplitudes*, IEEE Trans. on Ind. Electr., vol. 51, no. 2, pp. 511-517, 2004.
36. M. Karimi-Ghartemini, and A.K. Ziarani, *Periodic orbit analysis of two dynamical systems for electrical engineering applications*, J. Eng. Math., vol. 45, no. 2,pp. 135-154, 2003.
37. G.H. Golub, and A. van Loan, *Matrix Computations*, John Hopkins U. Press, 1996.
38. S.C. Gupta, Phase-locked loops, *Proc. IEEE*, pp. 291-306, 1975.
39. S. Haykin, *Adaptive Filter Theory*, Prentice Hall, 2003.
40. W.A. Hill, and C.D. Harbourt, "Performance of medium voltage multilevel inverters", *Conf. Rec. IEEE-IAS Ann. Meeting*, pp. 1186-1192, 1999.
41. D. Holmes, and T. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, Wiley-IEEE Press, 2003.
42. J. Holtz, *Pulse width Modulation – A Survey*, IEEE Trans on Ind. Elec., vol. 39, no. 5, pp. 410-420, 1992.
43. M. Hou, *Amplitude and frequency estimator of a sinusoid*, IEEE Trans. on Aut. Contr., vol. 50, no. 5, pp. 855-858, 2005.
44. M. Hou, *Estimation of sinusoidal frequencies and amplitudes using adaptive identifier and observer*, IEEE Trans. on Aut. Contr., vol. 52, no. 3, pp. 493-498, 2007.
45. G.-C. Hsieh, and J.C. Hung, *Phase-Locked Loop Techniques – A Survey*, IEEE Trans. on Ind. Elec., vol. 43, no. 6, pp. 609-615, 1996.
46. L. Hsu, R. Ortega, and G. Damm, *A globally convergent frequency estimator*, IEEE Trans. on Aut. Contr., vol. 44, no. 4, pp. 698-713, 1999.
47. V. Kaura, and V. Blasko, *Operation of a phase locked loop system under distorted utility conditions*, IEEE Trans. on Ind. App., vol. 33, no. 1, pp. 58-63, 1997.
48. P. Karuppanan, and K.K. Mahapatra, *PLL synchronization with PID controller based shunt active power line conditioners*, Int. J. of Comp. and Elec. Eng., vol. 3, no. 1, pp. 42-47, 2011.
49. M. P. Kazmierkowski, and R. Krishnan, *Control in power electronics*, Academic Press, 2002.
50. M. P. Kazmierkowski, and L. Malesani, *Current control techniques for three-phase voltage-source PWM converters: a survey*, IEEE Trans. on Ind. App., vol. 45, no. 5, pp. 691-703.
51. H. K. Khalil, *Nonlinear Systems*, Prentice Hall Inc., 2000.
52. J. W. Kolar, H. Ertl, and F.C. Zach, *Influence of the modulation method on the conduction and switching losses of a PWM converter system*, IEEE Trans. on Ind. App., vol. 27, no. 6, pp. 1064-1075, 1991.
53. J.-S. Lai, C.-M. Li, and C.-H. Liu, "Harmonic elimination pulse-width modulation techniques of real time inverter control for induction motor drives", *Proc. on Ind. Ele. Soc., IECON*, pp. 1391-1396, 1999.
54. J.-S. Lai, F.Z. Peng, *Multilevel converters-a new breed of power converters*, IEEE Trans. on Ind. App., vol. 32, no. 3, pp. 509-517, 1996.
55. M. Liserre, R. Teodorescu, and F. Blaabjerg, *Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values*, IEEE Trans. on Power. Elec., vol. 21, no. 1, pp. 263-272, 2006.
56. M. Liserre, F. Blaabjerg, and S. Hansen, *Design and Control of an LCL-Filter-Based three-phase Active Rectifier*, IEEE Trans. on Ind. App., vol. 41, no. 5, pp. 1281-1291, 2005.

57. M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of grid-connected PV inverters with large grid impedance variation", *Conf. Power. Elec. Spec., PESC*, pp. 4773-4779, 2004.
58. P.C. Loh, P.C. Tan, F. Blaabjerg, and T.K. Lee, "Topological Development and Operational Analysis of Buck-Boost Current Source Inverters for Energy Conversion Applications", *Proc. on Ele. Spec. Conf., PESC*, pp. 1-6, 2006.
59. R. Lund, M. Manjerkar, P. Steimer, and T. Lipo, "Control strategy for a hybrid seven-level inverter", *Proc. Eur. Pow. Elec. Conf., EPE*, 1999.
60. L. Malesani, and P. Tomasin, "PWM current control techniques of voltage source converters - a survey", *Proc. on Ind. Ele., Contr., and Inst., IECON*, pp. 670-675, 1993.
61. M.D. Manjrekar, P.K. Steimer, and T. A. Lipo, *Hybrid multilevel power conversion system: a competitive solution for high-power applications*, IEEE Trans. on Ind. App., vol. 36, no. 3, pp. 834-841, 2000.
62. R. Marino, and P. Tomei, *Global estimation of n unknown frequencies*, IEEE Trans. on Aut. Contr., vol. 47, no. 8, pp. 1324-1328, 2002.
63. N. Mohan, T. M. Underland, and W. P. Robbins, *Power Electronics: converters, applications, and design*, John Wiley & Sons, Inc., 2003.
64. M. Mojiri, M. Karimi-Ghartemani, and A. Bakhshai, *Time-Domain Signal Analysis Using Adaptive Notch Filter*, IEEE Trans. on Sig. Proc., vol. 55, no. 1 , pp. 85-93, 2007.
65. D. O. Neacsu, *Power-switching converters*, CRC Press, 2006.
66. G. Obregon-Pulido, B. Castillo-Toledo, A.A. Loukianov, *Global convergent estimator for n−frequencies*, IEEE Trans. on Aut. Contr., vol. 47, no. 5, pp. 857-863, 2002.
67. B. Panda, D.P. Bagarty, S. Behera, *Soft-switching DC-AC converters: a brief literature review*, Int. J. on Eng. Sc. and Tech., vol. 2, no. 12, pp. 7004-7020, 2010.
68. C. Ramos, A. Martins, and A. da Silva Carvalho, "Synchronizing renewable energy sources in distributed generation systems", *Conf. on Renew. Ener. and Power Quality, ICREPQ*, pp. 1-5, 2005.
69. P.A. Regalia, *An improved lattice-based IIR notch filter*, IEEE Trans. on Sig. Proc., vol. 39, no. 9, pp. 2124-2128, 1991.
70. Technology Roadmaps, *Solar photovoltaic energy*, International Energy Agency, 2010.
71. P. Rodriguez, A. Luna, I. Candela, R. Teodorescu, and F. Blaabjerg, "Grid synchronization of power converters using multiple second order generalized integrators", *Industrial Electronics, IECON*, pp. 755-760, 2003.
72. J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, *Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives*, IEEE Trans on Ind. Elec., vol. 54, no. 6, pp. 2930-2945, 2007.
73. J. Rodriguez, J.S. Lai, and F.Z. Peng, *Multilevel inverters: A survey of topologies, controls and applications*, IEEE Trans on Ind. Elec., vol. 49, no. 4, pp. 742-738, 2002.
74. P. Rodriguez, J. Pou, J. Bergas, J.I. Candela, R.P. Burgos, and D. Boroyevich, *Decoupled Double Synchronous Reference Frame PLL for Power Converters Control*, IEEE Trans. on Power. Elec., vol. 22, no. 2, pp. 584-592, 2007.
75. F.J. Rodriguez, E. Bueno, M. Aredes, L.G.B. Rolim, F.A.S. Neves, and M.C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters", *IEEE Conf. on Ind. Elec., IECON*, pp. 176-181, 2008.

76. M. Ruff, H. Mitlehner, and R. Helbig, *SiC Devices: Physics and Numerical Simulation*, IEEE Trans. Elec. Devices, vol. 41, no. 6, pp. 1040-1054, 1994.
77. S. Santoso, H. W. Beaty, R. C. Dugan, and M. F. McGranaghan, *Electrical Power Systems Quality*, McGraw-Hill, 2003.
78. B.B. Sharma, and I.N. Kar, *Design of asymptotically convergent frequency estimator using contraction theory*, IEEE Trans. on Aut. Contr., vol. 53, no. 8, pp. 1932-1937, 2008.
79. W. Shockley, and W. T. Read, *Statistics of the Recombinations of Holes and Electrons*, Phys. Rev., vol. 87, no. 5, pp. 835-842, 1952.
80. J.A. Short, D.G. Infield, and L.L. Freris, *Stabilization of Grid Frequency Through Dynamic Demand Control*, IEEE Trans. on Power. Sys., vol. 22, no. 3, pp. 1284-1293, 2007.
81. G. Sinha, and T.A. Lipo, "A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters", *Conf. on Ind. Elec., Contr. and Instr., IECON*, pp. 670-675, 1997.
82. T. L. Skvarenina, *The power electronics handbook*, CRC Press, 2002.
83. H.S. Song, and K. Nam, *Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions*, IET Proc. on Gen. Trans. and Dist., vol. 147, no. 6, pp. 409-415, 2000.
84. B.M. Song, S. Gurol, C.Y. Jeong, D. W. Yoo, and J.S. Lai, "A soft-switching high-voltage active power filter with flying capacitors for urban maglev system applications", *Conf. Rec. IEEE-IAS Ann. Meeting*, pp. 1461-1469, 2001.
85. B.M. Song, and J.S. Lai, *A multilevel soft-switching inverter with inductor coupling*, IEEE Trans. on Ind. App., vol. 37, no. 2, pp. 628-636, 2001.
86. J. Svensson, *Synchronization methods for grid-connected voltage source converters*, IEE Proc. on Gen. Trans. and Dist.,vol. 148, no. 3, pp. 229-235, 2001.
87. R. Teodorescu, F. Blaabjerg, M. Liserre, and P.C. Loh, *Proportional-resonant controllers and filters for grid-connected voltage-source converters*, IEE Proc. Electr. Power App., vol 153, no. 5, pp. 750-762, 2006.
88. R. Teodorescu, F. Blaabjerg, M. Liserre, and P.C. Loh, *Proportional-resonant controllers and filters for grid-connected voltage-source converters*, IEE Proc. on Elec. Power Appl., vol. 153, no. 5, pp. 750-762, 2006.
89. A.V. Timbus, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Adaptive resonant controller for grid-connected converters in distributed power generation systems", *Conf. on App. Power Elec.,APEC*, pp.6-13, 2006.
90. S. Valiviita, *Zero-crossing detection of distorted line voltages using* $1-b$ *measurements*, IEEE Trans. on Ind. Elec., vol. 46, no. 5, pp. 917-922, 1999.
91. G. J. Wakileh, *Power Systems Harmonics: Fundamentals, Analysis and Filter Design*, Springer Berlin Heidelberg, 2001.
92. B. Wu, *High-Power Converters and AC Drives*, Wiley-IEEE Press, 2006.
93. X. Yuan, W. Merk, H. Stemmler, and J. Allmeling, *Stationary frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions*, IEEE Trans. on Ind. App.,vol. 38, no. 2, pp. 523-532, 2002.
94. X.Yuan, and G. Orgimeister, *ARCPI resonant snubber for the neutral-point-clamped (NPC) inverter*, IEEE Trans. on Ind. App., vol. 36, no. 2, pp. 585-595, 2000.
95. X.Yuan, and I. Barbi, *Zero voltage switching for three level capacitor clamping inverter*, IEEE Trans. on Power. Elec., vol. 14, no.4, pp. 771-781, 1999.

96. X. Xia, *Global frequency estimation using adaptive identifiers*, IEEE Trans. on Aut. Contr., vol. 47, no. 7, pp. 1188-1193, 2002.