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TITOLO TESI

Reliability of GaN-based devices for Energy Efficient Power Applications

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"A dream you dream alone is only a DREAM. A dream you dream TOGETHER is reality."

Yoko Ono

Abstract

The wide spectrum of power electronics applications, including their role in renewable energy conversion and energy saving, require the innovation from conventional Silicon (Si) technology into new materials and architectures that allow the fabrication of increasingly lightweight, compact, efficient and reliable devices. However, the trade-off between long lifetime, high performance and low cost in the emerging technologies represents a huge limitation that has gained the attention of different research groups in the last years.

Gallium Nitride (GaN) is a wide-bandgap semiconductor (WBGS) that constitutes an excellent candidate for high-power and high-frequency applications due to its remarkable features such as high operating temperature, high dielectric strength, high current density, high switching speed, and low on-resistance. Compared with its Silicon counterpart, GaN is superior in terms of high breakdown field (3 MV/cm), exceptional carrier mobility, and power dissipation. By taking into account other WBG materials such as SiC, GaN grown on Si substrates promises similar performance but at a much lower cost in the low to mid power and high-frequency range.

Since GaN allows size and weight device reduction due to a better relationship between on-resistance and breakdown voltage, it is suitable for a variety of applications such as RF power amplifiers, power switching systems, sensors, detectors, etc. Especially, in the field of energy efficiency, GaN technology appears as a future successor of Si in power conversion circuits. However, some drawbacks related to technology cost, integration, and long-term reliability have to be overcome for its wide adoption in the power applications market.

One of the worst inconveniences of AlGaN/GaN High Electron Mobility Transistors (HEMTs) is the normally-ON operation. Since a two-dimensional electron gas (2DEG) channel is formed at the AlGaN/GaN interface due to inherent material properties, a negative bias has to be applied at the gate to switch the device off. Among the proposed solutions to fabricate normally-OFF devices, the metal-oxide/insulator-semiconductor (MOS/MIS) structure with different insulators has shown remarkable improvements in gate leakage reduction and drain current increase. Also in AlGaN/GaN Schottky Barrier Diodes (SBDs), the introduction of a MOS structure to create a gated edge termination (GET) at the anode area has resulted in significant improvements in reverse diode leakage and forward diode voltage. Nevertheless, the improvement in the device performance by the introduction of a dielectric could seriously affect the device long-term reliability since additional degradation in this layer and at its interfaces with AlGaN or GaN occurs.

In the case of conversion systems, power devices are continuously switched from an OFF-state condition at high drain bias to an ON-state condition at large drain current. Therefore, the reliability of GaN-based devices has to be proven for the complete ON/OFF operation. This dissertation focuses on providing a more comprehensive analysis of two main reliability issues related to the dielectric insertion under the gate/anode stacks by analyzing the use of different dielectric materials and device architectures.

The first issue is the positive bias temperature instability (PBTI), which is related to the degradation of electrical parameters when high gate voltages and temperatures are applied and is especially observed during the ON-state operation of the transistor. By using MOS-HEMT structures with different gate dielectrics (SiO_2, Al_2O_3, and AlN/Al_2O_3), the impact of the stress voltage, recovery voltage and temperature on the device reliability is analyzed including the role of oxide traps and the interface states to provide physical insights into this mechanism.

The second phenomenon discussed in this thesis is the time-dependent dielectric breakdown (TDDB) observed on GET-SBDs during its OFF-operation. The percolation model and Weibull distribution are used to understand this degradation mechanism. As a result, it has been demonstrated that the time to breakdown t_{BD} is influenced by the GET structure (single vs. double), the passivation thickness, the preclean process at the anode region before the GET dielectric deposition and the capping layer. Finally, by using 2D TCAD simulations, the long-term reliability improvement has been related to the reduction of the electric field peaks at critical areas such as the GET corner and beneath the anode field plate.

Sommario

Il nitruro di gallio (GaN) è un semiconduttore ad ampia banda proibita (WBGS) che costituisce un candidato eccellente per applicazioni ad alta potenza e ad alta frequenza grazie alle sue notevoli caratteristiche come alta temperatura operativa, elevata rigidità dielettrica, alta densità di corrente, elevata velocità di commutazione e bassa resistenza.

Poiché GaN consente riduzioni di dimensioni e peso del dispositivo grazie a una migliore relazione tra tensione on e resistenza, è adatto per una varietà di applicazioni come amplificatori di potenza RF, sistemi di commutazione dell'alimentazione, sensori, rivelatori, ecc. Soprattutto nel campo di efficienza energetica, la tecnologia GaN appare come un futuro successore di Si nei circuiti di conversione di potenza. Tuttavia, alcuni inconvenienti legati al costo, all'integrazione e all'affidabilità a lungo termine della tecnologia devono essere superati per la sua ampia adozione nel mercato delle applicazioni di potenza.

Uno dei peggiori inconvenienti dei transistor ad alta mobilità di elettroni AlGaN/GaN (HEMT) è l'operazione normalmente attivata. Poiché un canale bidimensionale a gas di elettroni (2DEG) è formato all'interfaccia AlGaN/GaN a causa delle proprietà intrinseche del materiale, è necessario applicare una polarizzazione negativa al gate per spegnere il dispositivo. Tra le soluzioni proposte per fabbricare dispositivi normalmente OFF, la struttura di ossido di metallo/isolante-semiconduttore (MOS/MIS) con diversi isolanti ha mostrato notevoli miglioramenti nella riduzione della perdita di gate e nell'aumento della corrente di drain. Anche nei diodi a barriera Schottky (SBD) AlGaN/GaN, l'introduzione di una struttura MOS per creare una terminazione del bordo gated (GET) nell'area dell'anodo ha portato a miglioramenti significativi nella perdita di diodo inversa e nella tensione di diodo diretta. Tuttavia, il miglioramento delle prestazioni del dispositivo mediante l'introduzione di un dielettrico potrebbe seriamente compromettere l'affidabilità a lungo termine del dispositivo poiché si verifica un ulteriore degrado in questo strato e nelle sue interfacce con AlGaN o GaN.

Questa dissertazione si concentra sulla fornitura di un'analisi più completa di due principali problemi di affidabilità relativi all'inserzione dielettrica sotto le pile di gate/anodi analizzando l'uso di diversi materiali dielettrici e architetture di dispositivi. Il primo problema è l'instabilità positiva della temperatura di polarizzazione (PBTI), che è correlata alla degradazione dei parametri elettrici quando vengono applicate alte tensioni di gate e temperature e viene particolarmente osservato durante il funzionamento a stato ON del transistor. Utilizzando strutture MOS-HEMT con diversi dielettrici di gate (SiO_2, Al_2O_3, e AlN/Al_2O_3), l'impatto della tensione di tensione, della tensione di recupero e della temperatura sull'affidabilità del dispositivo viene analizzato includendo il ruolo delle trappole di ossido e gli stati dell'interfaccia per fornire intuizioni fisiche in questo meccanismo.

Il secondo fenomeno discusso in questa tesi è la ripartizione dielettrica dipendente dal tempo (TDDB) osservata su GET-SBD durante la sua operazione OFF. Il modello di percolazione e la distribuzione di Weibull sono utilizzati per comprendere questo meccanismo di degrado. Di conseguenza, è stato dimostrato che il tempo di rottura del t_{BD} è influenzato dalla struttura GET (singola contro doppia), dallo spessore di passivazione, dal processo precluso nella regione dell'anodo prima

della deposizione dielettrica GET e dallo strato di capping. Infine, utilizzando simulazioni 2D TCAD, il miglioramento dell'affidabilità a lungo termine è stato correlato alla riduzione dei picchi del campo elettrico in aree critiche come l'angolo GET e sotto la piastra del campo anodico.

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Finally, these words are for you my dear Cristian: Thank you so much for your deepest love, for your support through the distance, for encouraging me to pursue my dreams and for holding my hands in my ups and downs. I still cannot believe how lucky I am to be your wife. I am eternally in debt to God for having you in my life. Your love was and is my greatest inspiration every day and makes me a better version of myself. I love you.

Thank you all,
Eliana

Contents

List of Figures

List of Tables

List of Abbreviations

2D	Two-**D**imensional
2DEG	Two-**D**imensional **E**lectron **G**as
AER	**A**ctive **E**nergy **R**egion
AlGaN	**A**luminium **G**allium **N**itride
ALD	**A**tomic **L**ayer **D**eposition
ALE	**A**tomic **L**ayer **E**tching
AlN	**A**luminium **N**itride
Al_2O_3	**A**luminium **O**xide
APM	**A**mmonia and hydrogen **P**eroxide **M**ixture
BTI	**B**ias **T**emperature **I**nstability
CAD	**C**omputer **A**ided **D**esign
CCM	**C**ontinuous **C**onduction **M**ode
CCS	**C**onstant **C**urrent **S**tress
CDF	**C**umulative **D**istribution **F**unction
CISM	**C**omplete **I**nductor **S**upplying **M**ode
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CVS	**C**onstant **V**oltage **S**tress
DC	**D**irect **C**urrent
DUT	**D**evice **U**nder **T**est
EPC	**E**fficient **P**ower **C**onversion
FN	**F**owler-**N**ordheim
FOM	**F**igure **O**f **M**erit
FP	**F**ield **P**late
GaAs	**G**allium **A**rsenide
GaN	**G**allium **N**itride
GET	**G**ated **E**dge **T**ermination
HEMT	**H**igh **E**lectron **M**obility **T**ransistor
HCI	**H**ot **C**arrier **I**njection
HCl	**H**ydrogen **C**hloride
HfO_2	**H**afnium **O**xide
HfSiON	**H**afnium **S**ilicon **O**xynitride
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
InGaAs	**I**ndium **G**allium **A**rsenide
InGaN	**I**ndium **G**allium **N**itride
IPL	**I**nterfacial **P**assivation **L**ayer
IPM	**I**ntelligent **P**ower **M**odule
JEDEC	**J**oint **E**lectron **D**evice **E**ngineering **C**ouncil
MIS	**M**etal **I**nsulator **S**emiconductor
MOCVD	**M**etal **O**rganic **C**hemical **V**apour **D**eposition
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransitor
NBTI	**N**egative **B**ias **T**emperature **I**nstability
PAE	**P**ower **A**dded **E**fficiency

PBTI	**P**ositive **B**ias **T**emperature **I**nstability
PDF	**P**robability **D**istribution **F**unction
PEALD	**P**lasma **E**nhanced **A**tomic **L**ayer **D**eposition
PECVD	**P**lasma **E**nhanced **C**hemical **V**apour **D**eposition
RF	**R**adio **F**requency
SBD	**S**chottky **B**arrier **D**iode
Sc_2O_3	**S**candium **O**xide
SCLC	**S**pace **C**harge **L**imited **C**urrent
SCR	**S**ilicon **C**ontrolled **R**ectifier
SEM	**S**canning **E**lectron **M**icroscope
SiC	**S**ilicon **C**arbide
SiGe	**S**ilicon **G**ermanium
SiN_x	**S**ilicon **N**itride
SiO_2	**S**ilicon **O**xide
SiON	**S**ilicon **O**xynitride
SOI	**S**ilicon **O**n **I**nsulator
SPM	**S**ulfuric acid and hydrogen **P**eroxide **M**ixture
TCAD	**T**echnology **C**omputer **A**ided **D**esign
TDDB	**T**ime **D**ependent **D**ielectric **B**reakdown
TiN	**T**itanium **N**itride
TLM	**T**ransfer **L**ength **M**easurement
VDP	**V**an **D**er **P**auw
WBG	**W**ide **B**and **G**ap
WBGS	**W**ide **B**and **G**ap **S**emiconductor
ZrO_2	**Z**irconium **O**xide

Physical Constants

c	speed of light in vacuum =	$(2.997\,924\,58 \times 10^{8}\,\mathrm{m\,s^{-1}}$ (exact))
ϵ_0	vacuum permittivity =	$(8.854\,187 \times 10^{-12}\,\mathrm{A\,s\,V^{-1}\,m^{-1}})$
h	Planck constant =	$(6.626\,069 \times 10^{-34}\,\mathrm{J\,s})$
q	elementary charge =	$(1.602 \times 10^{-19}\,\mathrm{C})$
k	Boltzmann constant =	$(1.380\,649 \times 10^{-23}\,\mathrm{J\,K^{-1}})$

List of Symbols

a	Strained lattice constant	Å
a_0	Unstrained lattice constant	Å
b	Trapping rate parameter	*numerical value*
C	Capacitance	F
C_{13}	Elastic deformation constant	GPa
C_{33}	Elastic deformation constant	GPa
C_{OX}	Oxide capacitance	F
D	Duty cycle	%
D_{ot}	Oxide defect density	cm^{-2}
e_{31}	Piezoelectric coefficient	$\mathrm{C\,m}^{-2}$
e_{33}	Piezoelectric coefficient	$\mathrm{C\,m}^{-2}$
E_a	Activation energy	eV
E_c	Conduction band edge energy	eV
$E_{critical}$	Critical electric field	$\mathrm{MV\,cm}^{-1}$
E_D	Surface-state energy	eV
$E_{F,C}$	Channel Fermi Level	eV
E_g	Energy bandgap	eV
E_{ox}	Electric field within the oxide	$\mathrm{MV\,cm}^{-1}$
E_p	Vertical polarization field	$\mathrm{MV\,cm}^{-1}$
E_v	Valence band edge energy	eV
E_x	Lateral polarization field	$\mathrm{MV\,cm}^{-1}$
f or (f_s)	Switching frequency	Hz
i	Current	A
I_{ac}	Anode-cathode current	A
I_D	Drain current	A
I_{DSS}	Saturation current	A
I_G	Gate current	A
$I_{leakage}$	Leakage current	$\mathrm{A\,mm}^{-1}$
I_{OFF}	OFF-state current	A
I_{ON}	ON-state current	A
$I_{threshold}$	Threshold current	A
L	Inductance	H
L_{ac}	Anode=cathode length	µm
L_g	Gate length	µm
L_{g1}	First edge termination length	µm
L_{g2}	Second edge termination length	µm
L_{gd}	Gate-drain length	µm
L_{gs}	Gate-source length	µm
L_{sc}	Schottky contact length	µm
m	Trap generation rate	*numerical value*
n_i	Carrier concentration density	cm^{-3}
n_s or (N_s)	2DEG carrier density	cm^{-2}

N_D	Doping density	cm^{-3}
N_{min}	Oxide-trap density needed to cause the breakdown	cm^{-2}
$N_{threshold}$	Threshold noise amplitude	dB
P_{OFF}	OFF-state dissipation	W
P_{ON}	ON-state dissipation	W
P_{out}	Output power	W
P_{pz}	Piezoelectric polarization	$\mathrm{C\,m}^{-2}$
P_{sp}	Spontaneous polarization	$\mathrm{C\,m}^{-2}$
P_{static}	Static power loss	W
q	Elementary charge	C
r	Radius of the sphere around generated traps	Å
R_C	Contact resistance	$\Omega\,\mathrm{mm}$
R_{load}	Load resistance	Ω
R_{ON}	ON-resistance	$\Omega\,\mathrm{mm}$
$R_{ON,sp}$	Specific ON-resistance	$\Omega\,\mathrm{cm}^2$
R_{sheet}	2DEG sheet resistance	Ω/sq
R_{th-jc}	Junction-to-case thermal resistance	$\mathrm{K\,W}^{-1}$
t	Time	s
t_{AlGaN}	AlGaN barrier thickness	Å
t_{BD}	Time to breakdown	s
t_{CR}	critical AlGaN barrier thickness	Å
t_M	Measurement delay	s
t_{ox}	Oxide thickness	µm
t_{relax}	Relaxation time	s
t_{stress}	Stress time	s
v	Voltage	V
V_{ac}	Anode-cathode voltage	V
V_B	Barrier voltage drop	V
V_{BD}	Breakdown voltage	V
$V_{CRITICAL}$	Critical voltage	V
V_D	Drain voltage	V
V_{DS}	Drain-source voltage	V
V_{DS_kink}	Drain-source voltage to trigger the kink effect	V
V_F	Forward voltage	V
V_G	Gate voltage	V
V_{GS}	Gate-source voltage	V
V_{IN}	Input voltage	V
V_{OFF}	OFF-state voltage	V
V_{ON}	ON-state voltage	V
V_{OUT}	Output voltage	V
$V_{recovery}$	Recovery voltage	V
V_{sense}	Sensing voltage	V
V_{stress}	Stress voltage	V
V_{sat}	Saturated electron drift velocity	$\mathrm{cm\,s}^{-1}$
V_{th}	Threshold voltage	V
$V_{th,after}$	Threshold voltage after a stress pulse	V
V_{TON}	Turn-on voltage	V
W	Gate width	µm
W_D	Drift region width	µm
ΔE_c	Conduction band offset	eV

ΔI	Current step	A
ΔN_{OT}	Density of trapped charges	cm^{-2}
ΔV_{OUT}	Output voltage ripple	V
ΔV_{max}	Maximum threshold voltage shift	V
ΔV_{th}	Threshold voltage shift	V
ϵ (or ϵ_r)	Dielectric constant or relative permittivity	$F\,m^{-1}$
ϵ_0	Vacuum permittivity	$F\,m^{-1}$
ε_1	Strain in the basal plane	*numerical value*
ε_3	Strain along the growth directione	*numerical value*
ξ	Relaxation time divided by stress time	*numerical value*
ξ_M	Measurement delay divided by stress time	*numerical value*
η	Scale factor or 63.2% value	s
λ	Thermal Conductivity	$W\,cm^{-1}\,K^{-1}$
λ	Wavelength	nm
μ_n	Electron mobility	$cm^2\,V^{-1}\,s^{-1}$
σ_{POL}	Positive bound charge density	$C\,m^{-2}$
ϕ_B	Barrier height	eV
τ	Time constant	s

To love in all its manifestations in my life, through my merciful God, my unconditional family, my beloved husband and my supportive friends. This strong and wonderful force has allowed me to create dreams, has motivated me to pursue them and has given me the perseverance to finally reach them. In special, this work is dedicated to self-love that is so meaningful in a person's life and which I have rediscovered through this Ph.D. journey…

Chapter 1

Introduction

1.1 Modern Power Electronics

Power electronics is the branch of electrical engineering related to the efficient conversion, control and conditioning of electric power in the wide range of milliwatts to gigawatts by means of switching power semiconductor devices. Although the term "Power Electronics" was introduced systematically from the early of the 1970s, officially it was born in 1901 by the invention of glass-bulb mercury-arc rectifier [1]. Subsequently, the eras of gas tube electronics and saturable core magnetic amplifiers appeared in the 1930s and 1940s, respectively. In 1958, this field went through the modern era of solid-state power electronics with the introduction of the thyristor or silicon controlled rectifier (SCR) in 1958. Since then, the development of this branch of electronics has taken different directions as depicted in Figure 1.1. Regarding the power semiconductor devices technology, the research has been focused on different semiconductor materials, processing, fabrication, and packaging techniques. Moreover, computer-aided-design (CAD) techniques and new simulation software helped in device modeling, characterization, and development of modern intelligent power modules (IPMs) [2]. As a result, improved new devices with high power capabilities emerged allowing a spread field of applications.

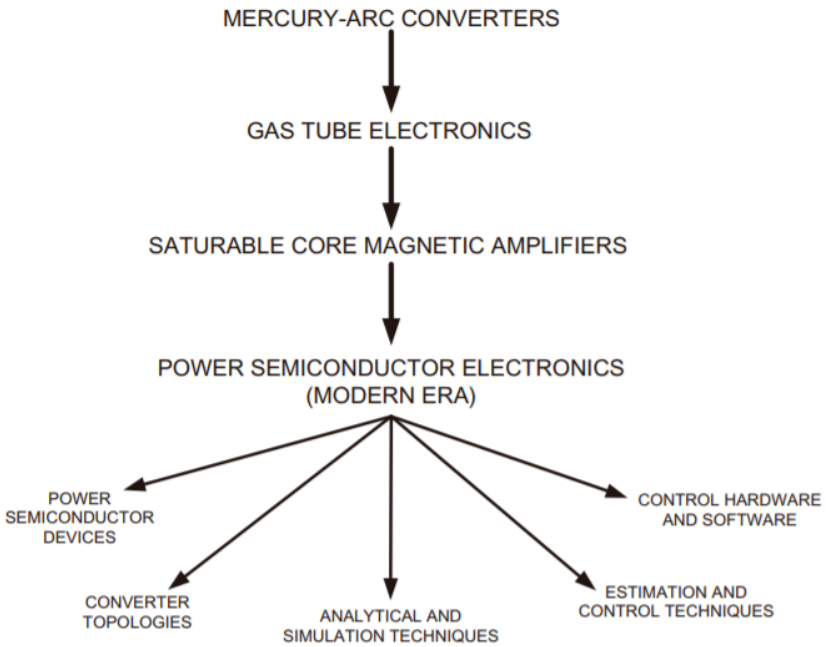

FIGURE 1.1: Historical evolution of power electronics [3].

Modern power electronics has also demonstrated higher efficiency and longer life reliability at a lower cost and smaller size compared with its predecessor technologies which make it an essential element in different industrial processes nowadays. As it can be seen from Figure 1.2, the power electronics applications have a very wide spectrum that covers from the low to the ultra-high-power range and a variety of frequencies by using different devices and materials.

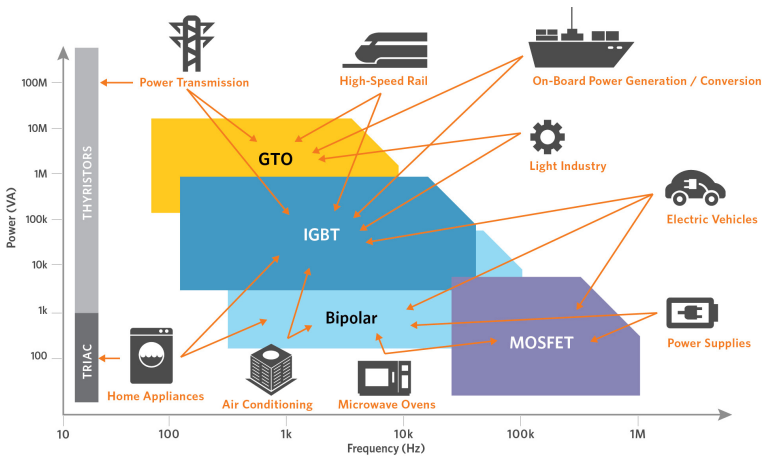

FIGURE 1.2: Application fields of power electronics [4].

Another important aspect of power electronics is related to its role in energy saving and renewable energy conversion to contribute to the environmental pollution control trends of the last decades (Figure 1.3). At least 50% of the electricity used in the world is controlled by power devices [5], of which almost 10% is lost due to the inefficiency of the conversion systems (EIA U.S. Electric Power Generation). Therefore, the research in the field of the power semiconductors is highly relevant to more fruitful efforts focused on minimizing losses and saving energy in these systems.

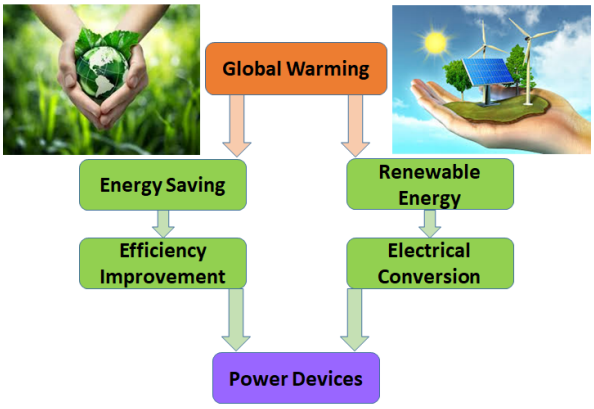

FIGURE 1.3: Importance of the research and development of power devices for more efficient and eco-friendly power systems.

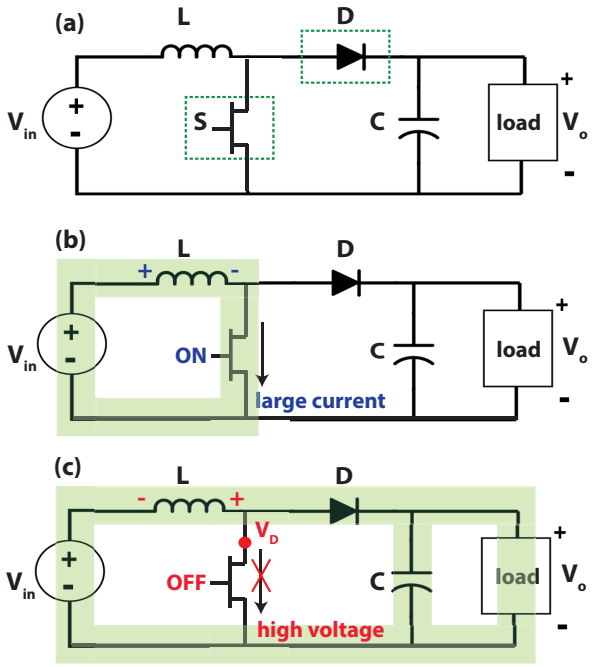

FIGURE 1.4: (a) Simplified schematic of a boost converter, which steps the DC voltage up. (b) ON-state transistor operation (large drain current). (c) OFF-state transistor operation (high drain voltage).

1.2 Switching devices in power conversion systems

Figure 1.4 (a) illustrates the schematic circuit of a boost converter that is a DC-to-DC power converter normally used to step DC voltages up (while stepping down current). It is important to mention that this converter aims to exemplify the role of switching semiconductor devices and their requirements for more efficient power systems and not to deeply describe the theory of DC-DC converters. In its more simplified form, it contains at least two semiconductor devices (a diode and a transistor), and one passive element to store energy (a capacitor, an inductor, or both). A normally-OFF transistor is always preferred in case of a gate driver failure from the safety point of view, and a Schottky diode instead of other types due to its lower forward voltage and reverse recovery current.

When the transistor is switched on, the current flows from the positive to the negative supply terminal through the inductor, which stores energy by generating a magnetic field. During this phase, the transistor is submitted to a high drain current and the diode is negatively biased (Figure 1.4 (b)). Once the power transistor is switched off, the inductor produces a back electromotive force (e.m.f.) and inverters its polarity to allows the current flow since an inductor is opposed to a sudden change in the current because of its voltage-current relationship given by:

$$v(t) = L\,\frac{\delta i(t)}{\delta t}. \tag{1.1}$$

As a result, the supply voltage appears in series with the back e.m.f in the inductor which generates a higher voltage to charge the capacitor through the diode. Under the OFF-state condition of the transistor, it tolerates a high drain voltage, while the diode is forward biased (Figure 1.4 (c)).

By considering a continuous conduction mode operation, i.e. the current through the inductor never falls to zero, the equation that describes the output voltage as a function of the input voltage is:

$$V_{OUT} = \frac{V_{IN}}{1 - D} \tag{1.2}$$

where D is the duty cycle (transistor ON-time divided by the switching period). Since D is a number between 0 and 1, it is clear that V_{OUT} is always greater than V_{IN}.

A high efficient power conversion system is always desired from the input to the output. Hence, the electronic components should warranty a minimal energy dissipation. The power loss of a switching circuit is basically classified into two components: static and dynamic power loss. The static power loss is described by:

$$P_{static} = P_{ON} + P_{OFF} = V_{ON} \times I_{ON} + V_{OFF} \times I_{OFF} \tag{1.3}$$

where there is a contribution of the ON- and OFF-state dissipation. In the ideal case, the switching devices provide infinite current with no voltage drop during the ON-state, while completely block the current when a reversed bias is applied. However, typical power devices require a voltage to keep the current flowing during the ON-state, and the leakage currents are not negligible at high reverse bias as illustrated in Figure 1.5.

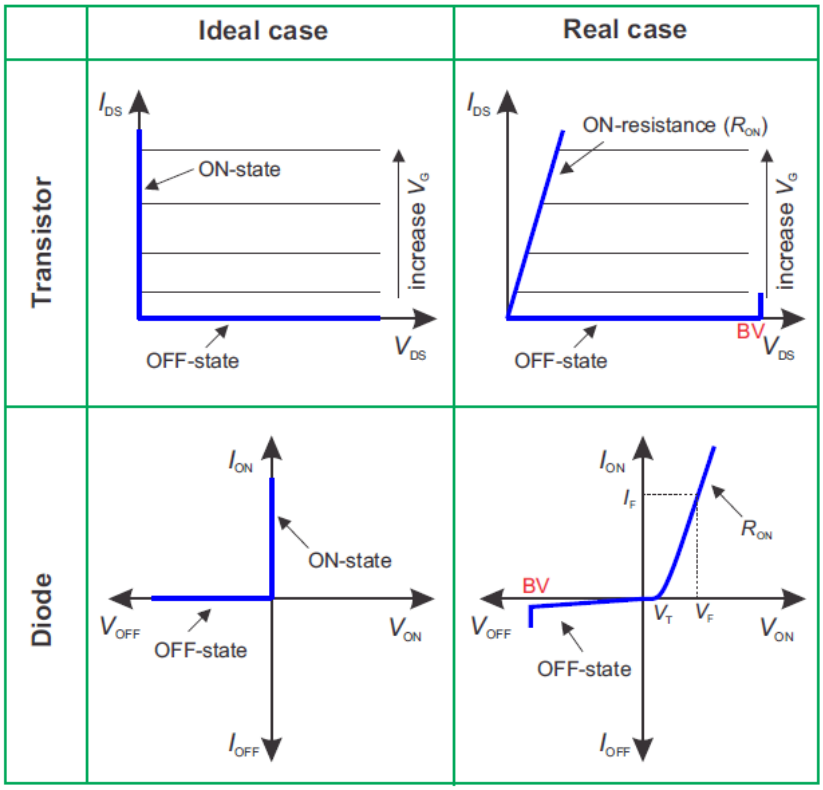

FIGURE 1.5: Ideal and real *I-V* curves of a diode and a transistor during ON- and OFF-state operation [5], [6].

Moreover, devices can fail at determined reverse bias known as breakdown voltage (V_{BD}) and lose their functionality and blocking capability in the circuit. Consequently, switching devices with low ON-state voltages (low ON-resistance R_{ON}) and low leakage currents are the challenge in the device engineering field.

On the other hand, the dynamic power loss occurs in the switching operation of the devices from ON- to OFF-state and vice versa. Therefore, low dynamic dissipation could be obtained by using devices with fast switching capability and low recovery current which are some of the advantageous characteristics of unipolar devices. Additionally, a faster switching frequency also helps to minimize the inductor and capacitor size, which consequently improves the transient performance, the circuit power density, and control bandwidth [7]. This latter relationship can be clarified if the output voltage ripple (ΔV_{OUT}) of the boost converter is analyzed. By considering that the converter is in a continuous conduction mode (CCM) and only the inductor supplies the energy for the load after the switch is turned off, i.e. complete inductor supplying mode (CISM) [8], the output voltage ripple can be calculated as:

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{D}{R_{load}\, C\, f_s} \tag{1.4}$$

where R_{load}, C, and f_s are the load resistance, the capacitance of the capacitor and the switching frequency, respectively.

As observed in Eq. 1.4, the adoption of faster-switching devices allow the use of smaller passive components for a given output voltage ripple, which is a key parameter in the DC-DC converter design.

1.3 Comparison of semiconductor materials for power applications

In the past decades (since the late 1950s), Silicon has been a more dominant semiconductor material in power electronics compared to earlier materials such as germanium or selenium. Its popularity is based on the new applications that it enabled, its high reliability, the easy way to use it and its low cost [9]. Additionally, the basic physical properties of this material in conjunction with the enormous investment in research and manufacturing infrastructure allowed its wide adoption. The first power metal oxide silicon field effect transistor (MOSFET) appeared in 1976 as a more robust alternative to bipolar transistors. Since then, the power handling efficiency and cost have improved continuously with the innovations of this structure.

However, a slow rate of improvement has been observed recently because Si-based power MOSFETs asymptotically approaches their theoretical limits. Although some studies have reported breaking the Si limits [10], [11] and there is still work to do in superjunction structures and Insulated Gate Bipolar Transistors (IGBTs), the newer power systems require to move towards other semiconductor materials with better performance to enhance the efficiency during power conversion. In this approach, wide bandgap semiconductors (WBGS) emerged as a possible Si successor in the medium- to high-power ratings (Figure 1.6) because their characteristics promise relevant performance improvements over their silicon-based counterparts.

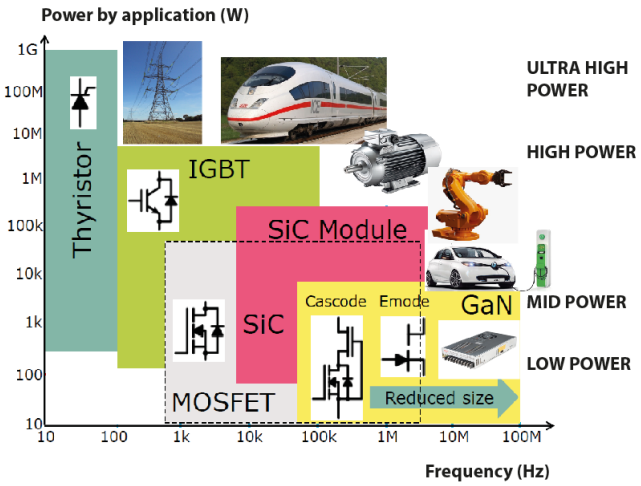

FIGURE 1.6: Emerging WBDS (Silicon Carbide and Gallium Nitride) in power applications.

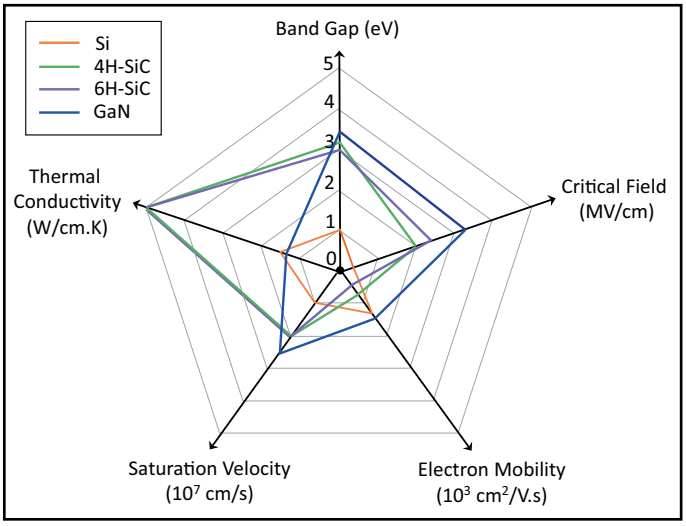

FIGURE 1.7: Physical properties comparison between WBGS and Si.

Figure 1.7 shows the comparison of five key physical properties that are indispensable for power applications, and a complete superiority of two specific wide bandgap materials contending for the power market, Silicon Carbide (SiC) and Gallium Nitride (GaN), is observed over the well know Silicon. The description of these properties is summarized below.

1.3.1 Bandgap (E_g)

This property is associated with the strength of the chemical bonds between atoms [9]. Therefore, the stronger the bonds, the harder is a jump of an electron from the top of the valence band to the bottom of the conduction band. The energy required to cause this electron movement is $E_g = E_c - E_v$, where E_g, E_c and E_v are the bandgap, the lowest energy of the conduction band and the upper energy level of the valence band, respectively (Figure 1.8). WBGS normally have bandgaps about three times or more that of Si. A high bandgap implies lower carrier concentration (n_i) and consequently lower leakage current due to its proportional dependence on n_i or n_i^2

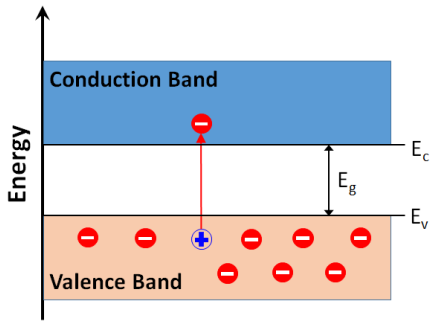

FIGURE 1.8: Simplified energy band diagram of a semiconductor [12].

[13]. Among WBGS, diamond has the widest bandgap (5.45 eV) and consequently, the highest critical electric field. It is followed by GaN (3.45 eV) and SiC (3.26 eV and 3.03 eV for 4H-SiC and 6H-SiC, respectively) with similar bandgaps, but remarkably higher than those of Si (1.12 eV) and GaAs (1.43 eV) [12].

1.3.2 Critical Electric Field ($E_{critical}$)

This characteristic is also related to the chemical bond strength that causes the wider band gap. Hence, WBGS need higher critical electric fields to initiate impact ionization, which finally results in an avalanche breakdown. According to Poisson's equation, the critical electric field and the breakdown voltage can be obtained with the formulas:

$$E_{critical} = \frac{q\, N_D\, W_D}{\epsilon_o\, \epsilon_r} \tag{1.5}$$

$$V_{BD} = \frac{1}{2}\, E_{critical}\, W_D = \frac{1}{2}\, \frac{q\, N_D\, W_D^2}{\epsilon_o\, \epsilon_r} \tag{1.6}$$

where $E_{critical}$, q, N_D, W_D, ϵ_o, and ϵ_r are the critical electric field, the charge of an electron, the doping density, the width of the drift region, the vacuum permittivity, and the semiconductor relative permittivity, respectively. From the Eq. 1.5 and 1.6, it can be seen that a 10 times increase in the electric field in conjunction with a 10 times reduction in the depletion width results in a 100 times greater number of electrons, N_D, in the drift region. This is the basis that allows the WBGS to outperform Si in power conversion [9]. Moreover, WBGS can reduce their physical size because it is possible to thin the drift region width while obtaining the same breakdown voltage as depicted in Figure 1.9.

1.3.3 Electron Mobility (μ_n)

A higher electron mobility allows lower resistivity since it is inversely proportional to the specific R_{ON} (resistance times unit area) due to the drift region through the equation:

$$R_{ON,sp} = \frac{W_D}{q\, \mu_n\, N_D}. \tag{1.7}$$

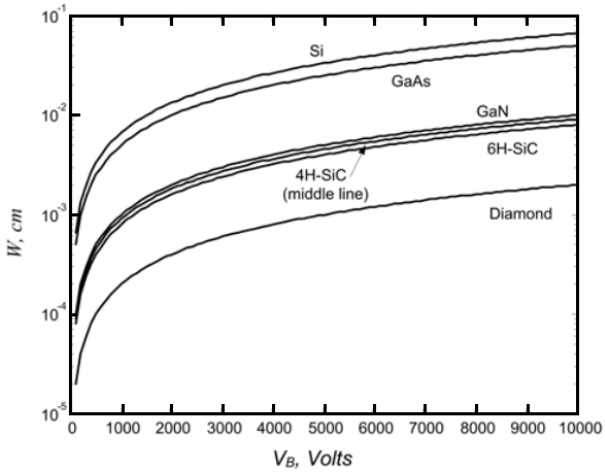

FIGURE 1.9: Drift region width for each material at different breakdown voltages [12].

TABLE 1.1: Material properties of Si, SiC, and GaN [9], [12], [14].

Material	$E_{critical}$ (MV/cm)	μ_n $(cm^2/V.s)$	ϵ_r	V_{sat} $(\times 10^7 cm/s)$	λ $(W/cm.K)$
Si	0.3	1350	11.8	1	1.5
4H-SiC	2	720	10	2	4.9
6H-SiC	2.4	370	9.7	2	4.9
GaN	3.3	1500	9	2.5	1.3

By combining the Eq. 1.5 and 1.6 in 1.7, the following expression is obtained:

$$\frac{R_{ON,sp}}{V_{BD}^2} = \frac{4}{\epsilon_0 \, \epsilon_r \, \mu_n \, E_{critical}^3} \tag{1.8}$$

Eq. 1.8 is known as Baliga figure-of-merit (FOM) and its derivation is based on the assumption that the V_{BD} is due to the critical field [15]. The ratio R_{ON}/V_{BD}^2 remains fixed once the material is selected because it only depends on the semiconductor intrinsic properties rather than the device physical dimensions. Therefore, alternative semiconductors with higher mobility and critical electric field such as WBGS are preferred to obtain an efficient power conversion since they allow a better trade-off between the breakdown voltage and the ON-resistance.

Figure 1.10 illustrates the corresponding theoretical limits ($R_{ON,sp}$ versus V_{BD}) by considering the material properties reported in Table 1.1, which includes Si and two WBGS (SiC and GaN) for comparison. The WBGS exhibit about three orders of magnitude lower $R_{ON,sp}$ compared with Si for a fixed breakdown voltage. For voltage ranges higher than 200 V, Si-based devices dissipate more ON-state power (higher conduction losses) due to their high resistance.

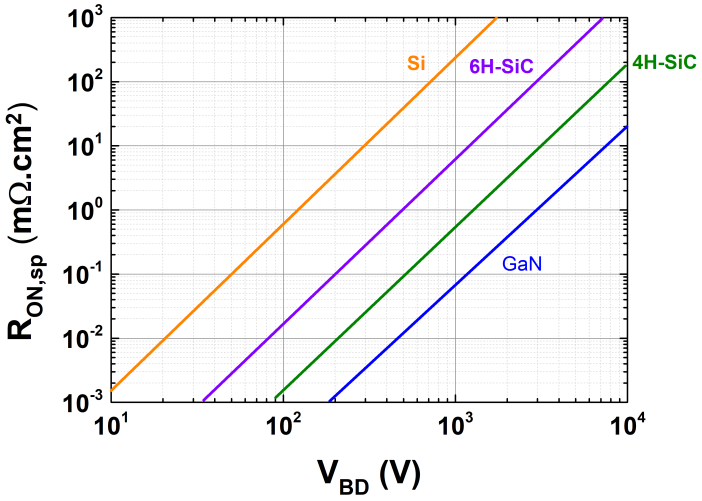

FIGURE 1.10: On-resistance versus breakdown voltage for Si, SiC, and GaN [14].

1.3.4 Saturated electron drift velocity (V_{sat})

The drift velocity is directly proportional to the semiconductor capability to switch at high-frequency. WBGS exhibit higher drift velocities compared with Si (see Table 1.1). Therefore, WBGS-based devices are expected to handle very high frequencies with smaller recovery current and shorter reverse recovery time [9]. Indeed, important achievements have been reached in the radio frequency (RF) world as reported in the literature by using these materials [16], [17].

1.3.5 Thermal Conductivity (λ)

Another advantage of these WBGS is their capability to operate at high temperatures, which allow their use in harsh environments and spread their adoption even to aerospace applications [18]. Additionally, some of the WBGS own a high thermal conductivity as in the case of the diamond (22 W/cm.K) and SiC (4.9 W/cm.K), which is translated into a low junction-to-case thermal resistance R_{th-jc}. As a result, the heat is easily dissipated out of the device and the device temperature increases slowly.

1.4 The Beginning of GaN in power electronics

Among WBG materials, Gallium Nitride has captured important attention because it fulfills most of the required properties for power applications within the III-V compounds such as higher bandgap values, critical field, electron mobility, and saturation velocity compared with other semiconductor technologies used for power electronics as previously depicted in Figure 1.7. The first RF high electron mobility transistor (HEMT) based on GaN was introduced by Eudyna Corporation in 2004 in Japan. This device was the result of the unusual high electron mobility observed in the region of an aluminum gallium nitride (AlGaN) and GaN heterostructure interface [9], [19], [20]. This GaN grown on SiC transistor was able to produce a benchmark power gain in the multi-gigahertz frequency range.

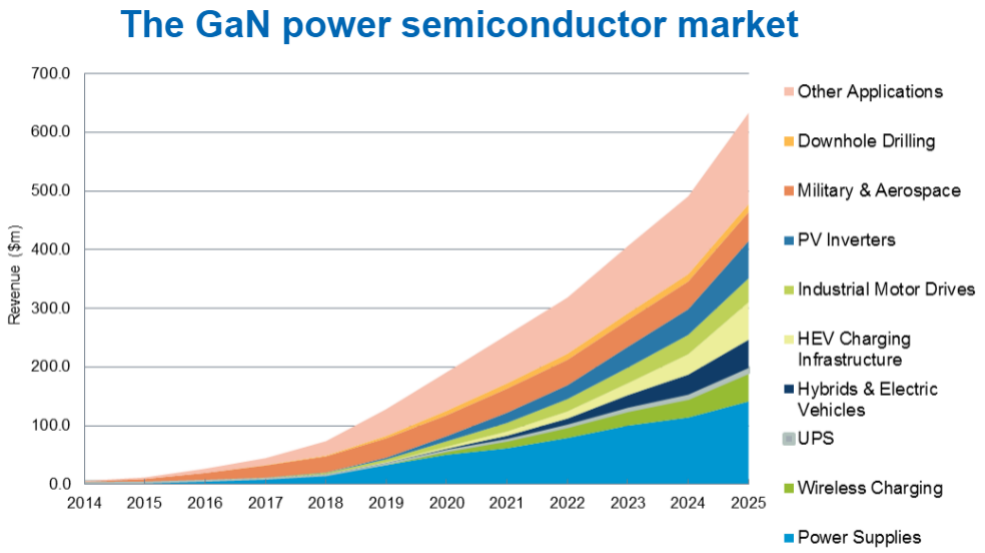

FIGURE 1.11: Increasing trend of the GaN power semiconductor market [21].

Later on, Nitronex Corp fabricated the first RF GaN-based HEMT grown on Si substrates. The journey of GaN in the RF market has been supported by several other companies. However, its adoption outside this market was limited by the fabrication cost as well as the depletion mode operation that will be discussed in detail in the next chapter. It is not until June 2009, that Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode or normally-OFF GaN FETs grown on Si wafers as a special replacement for power MOSFETs. Since then, many important companies such as Matsushita, Transphorm, Panasonic, RFMD, HRL, among others, have dedicated their manufactured GaN-based transistors to the power semiconductor market. As a result, the GaN participation in power applications has highly increased in recent years as illustrated in Figure 1.11

1.5 General limitations for a wide GaN-technology adoption

There are necessary requirements that new semiconductor technology has to fulfill for its wide adoption in power conversion systems. The first one is efficiency, and GaN has demonstrated a complete superiority over Si due to its remarkable characteristics, which results in switching devices that allow the design of high-efficient converters with low power loss [22–24].

The second one is cost-effectiveness. Although a direct cost comparison among semiconductor technologies is complicated due to all the elements that influence the final cost (epitaxial growth, wafer fabrication, and assembly) [9], we can mention that one of the drawbacks of GaN-based devices is the expensive homoepitaxy growth on GaN substrates. Therefore more affordable wafers based on Si have been used to make it more competitive for the voltage rating lower than about 600V range, but this makes the device more vulnerable to defect creation due to the difference in the thermal expansion coefficients and the lattice mismatch between both materials [25], [26]. If the voltage range target is higher, then GaN needs to be grown on SiC and diamond substrates which increase the cost with respect to its Si counterparts.

The last requirement is long-term reliability, i.e. the device probability of correctly performing under normal operating conditions for the intended lifetime [27]. The complexity of reliability studies lies in the tremendous high dependence of the device performance on the fabrication steps, the epitaxial growth, the characterization techniques and device to device variability, which complicates a complete understanding of the degradation phenomena and a consensus about the physics behind the failure mechanisms. Nowadays, discrete GaN power devices from 80 to 650 V applications have been qualified by using the JEDEC standards originally designed for Si technology. By considering that GaN-based structures differ from Si in the heteroepitaxial growth of GaN on foreign substrates and in a device operation based on intrinsic properties of heterojunctions instead of p and n dopings, they cannot be solely qualified with established silicon procedures. Therefore, more proper qualification tests that consider new possible failures modes, the associated physics and the corresponding lifetime models are urgently needed to spread the GaN adoption. Some manufacturers use their own reliability tests to qualify their GaN devices [28], but a joint effort has been recently established by the major semiconductor companies related to GaN and a working group under the framework of JEDEC to deal with this lack of qualification standards (JEDECREF). In this preamble, the reliability of GaN-based devices is an interesting and important field of research to warranty their industrial maturity and their massive adoption in the power application market.

1.6 Thesis content overview

1.6.1 Thesis objective

The remarkable electric characteristics of GaN which make it a promising candidate in the power applications market and some drawbacks that have to be overcome for its wide adoption have been reviewed. In particular, the reliability of GaN-based devices has been mention as a crucial and challenging aspect for extended use of this technology. Since it is necessary to warrant a lifetime ranged between 10 and 20 years at operating conditions in the semiconductor power devices area, accelerated test methods have to be implemented to predict the expected device lifetime in a feasible test time. By using acceleration factors (temperature, voltage, current, etc.), it is possible to induce the device failure earlier than usual and to extract the lifetime under normal conditions with the adoption of extrapolation methods. If the degradation mechanisms and the physical phenomena that induce device failure are not correctly understood, the reliability prediction could become meaningless. Therefore, this thesis focuses on the electrical characterization and exploration of degradation mechanisms which are especially observed in the ON-state operation of GaN-based transistors and the OFF-state operation of GaN-based diodes. Furthermore, two-dimensional (2D) TCAD simulations are performed in combination with experimental measurements for a better understanding of the degradation sources.

1.6.2 Thesis outline

After this first introduction about the capabilities and limitation of wide bandgap semiconductors, in special GaN, for high voltage and high current applications, following chapters describe in more detail the objectives and main results obtained from the reliability analysis in GaN-based devices. In particular, this dissertation is arranged into the following chapters:

Chapter 2: GaN technology

This chapter summarizes the GaN properties and the operating principle of devices based on this technology. Especially, the spontaneous creation of a two-dimensional electron gas channel at the AlGaN/GaN heterojunction due to intrinsic material properties is discussed. Moreover, the inconvenience of the naturally depletion-mode operation and the efforts to have truly enhanced-mode are also explained. The most common structure, i.e high electron mobility transistors (HEMT), as well as its variations based on the introduction of gate dielectrics, are also depicted. Finally, the main degradation issues and the device reliability dependence on the operating state conditions are described.

Chapter 3: Reliability study of MOS-HEMTs

Since a metal oxide semiconductor (MOS) structure has demonstrated remarkable improvements in gate leakage reduction, drain current increase and is within the framework to obtain true e-mode devices, this chapter shows the impact of inserting a gate dielectric on the device performance and reliability. Especially, the aging mechanism known as positive bias temperature instability (PBTI) which is normally observed in ON-state condition has been analyzed by using different insulators and characterization techniques (DC and pulsed measurements). In the first part of this chapter, SiO_2 as a gate dielectric has been studied by using different stress voltages and temperatures which allow describing the degradation mechanisms that are responsible for the observed instabilities. Additionally, in the second part, a comparative study between a single gate layer of Al_2O_3 and a bilayer formed by Al_2O_3 and AlN shows that the insertion of this AlN layer allows obtaining the normally-OFF operation, but it also negatively influences the electrical behavior and reliability of the device.

Chapter 4: Reliability study of GaN-based SBDs

Similarly to MOS-HEMTs, the introduction of a MOS structure to create a gated edge termination (GET) at the anode area next to the Schottky contact has resulted in significant improvements in reverse diode leakage and forward diode voltage in GaN-based Schottky Barrier Diodes (SBDs). Nevertheless, these improvements could come at the cost of device long-term reliability since additional degradation in this layer and at its interfaces with AlGaN or GaN occurs. Therefore, the first part of this chapter provides a more comprehensive analysis of the time-dependent dielectric breakdown (TDDB) observed during the OFF-state operation of AlGaN/GaN GET-SBDs fabricated in a 200-V GaN-on-Si platform technology by evaluating their dependence on the GET structure, passivation layer thickness, and preclean process. On the other hand, the second part of the chapter analyzes the influence of a thin passivation capping layer (GaN vs. Si_3N_4) in the diode degradation under OFF-state stress conditions.

Chapter 5: Conclusion and outlook

This final chapter summarizes the activity of this thesis, highlighting the main results, contributions and a brief discussion of possible future studies by taking as a baseline this work.

Chapter 2

GaN Technology

2.1 Material Properties

Gallium Nitride is a compound semiconductor formed by two elements of the III- and V-family (Gallium and Nitrogen, respectively). The ability to handle high voltage and high current density makes GaN a promising material for high power applications as previously described in chapter 1. The knowledge of the crystal structure, the intrinsic properties and the growth of GaN by using different substrates are fundamental to understand the operation of switching devices based on this material and it will be discussed in this section.

2.1.1 Crystal structure

III-N semiconductors including GaN crystallize mainly in two different structures: hexagonal wurtzite and cubic zinc-blende as depicted in Figure 2.1. Since thermodynamical stability has been demonstrated in the hexagonal wurtzite type [29], this is preferred for electronic device fabrication. This structure has four atoms per unit cell and is completely defined by the hexagonal base length (a), the cell height (c) and the III-N bond length along the c-axis (u). The structural parameters of GaN and other III-N compounds are summarized in Table 2.1.

The lack of symmetry in the wurtzite structure (different bond lengths) causes a spontaneous polarization P_{sp}, whose orientation depends on the polarity of the crystal structure. For a Ga-polarity (Ga-face), the P_{sp} points to the substrate; while for an N-polarity (N-face), it points inversely as shown in Figure 2.2. This intrinsic property plays an important role in the fabrication of High Electron Mobility Transistors (HEMTs) on Gallium Nitride as it will be explained later. The normal fabrication of GaN-based devices uses a Ga-face termination because it is easily obtained from a

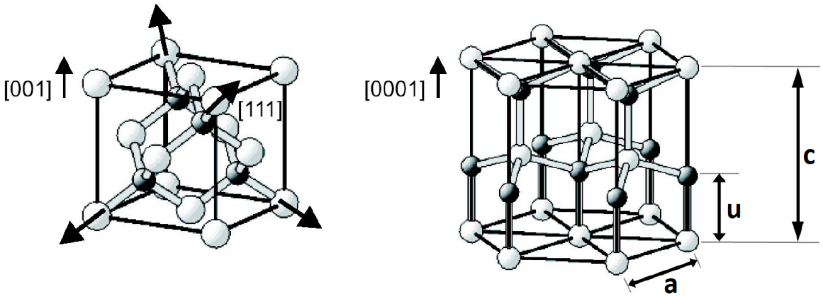

FIGURE 2.1: Cubic zinc-blende (left) and hexagonal wurtzite (right) structure in III-Nitrides. The lattice parameters a, c and u are shown for the wurtzite structure [30].

TABLE 2.1: Structural parameters of III-N wurtzite semiconductors [31]

Parameter	*GaN*	*AlN*	*InN*
a (Å)	3.197	3.108	3.580
c/a	1.6297	1.6033	1.6180
$(u - u_{ideal}) \times 10^{-3}$	1.9	6.4	3.7

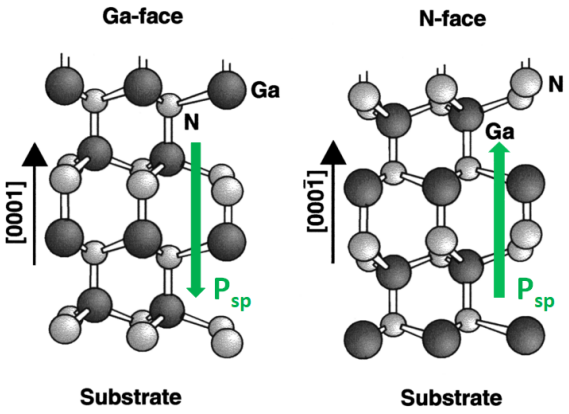

FIGURE 2.2: Spontaneous polarization orientation in Ga-face and N-face wurtzite structure [29].

metal organic chemical vapour deposition (MOCVD) process. Therefore, this thesis will only focus on Ga-face GaN-based devices.

Another interesting characteristic of GaN is that the minimal-energy state in the conduction band and the maximal-energy state in the valence band are characterized by the same crystal momentum (k-vector) in the Brillouin zone, i.e. it is a direct bandgap material, as can be seen from Figure 2.3. Hence, holes and electrons are located directly adjacent at the same momentum coordinates, which causes their easy transition by emission or absorption of light radiation. As a result, GaN is widely used in optical device fabrication.

2.1.2 AlGaN/GaN heterojunction

A heterojunction is an interface formed when a semiconductor material is grown on the top of another semiconductor that has different bandgap energy. In the specific case of the GaN technology, the AlGaN/GaN heterojunction allows the natural formation of a two-dimensional electron gas (2DEG) channel with high electron concentration due to the spontaneous and piezoelectric polarization properties of both compounds. More details about the 2DEG formation will be described in the following.

III-V materials have a strong spontaneous polarization (P_{sp}) due to the asymmetry of the bonding in the crystal structure which ultimately forms dipoles and causes the polarization. Apart from this intrinsic property, a piezoelectric polarization (P_{pz})

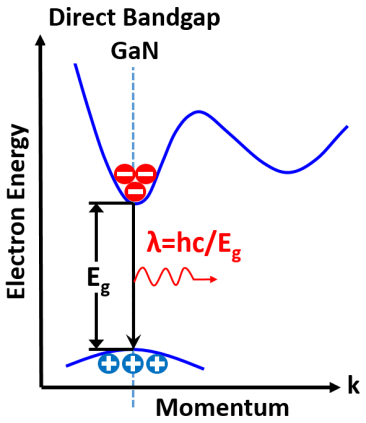

FIGURE 2.3: Energy band diagram for direct band gap GaN. The wavelength of an emitted photon is given by $\lambda = hc/E_g$ where h represents Planck's constant, c is the velocity of light, and E_g is the bandgap energy.

also appears if the materials are strained. By considering in the AlGaN/GaN heterojunction that the GaN layer is several orders of magnitude thicker than the AlGaN layer, it is assumed that the GaN layer is fully relaxed (no piezoelectric polarization), while the AlGaN layer is under tensile strain. Since the growth direction of III-V compounds is parallel (or antiparallel) to the c-axis of the crystal, the side of the hexagonal base a is the lattice constant that the AlGaN and GaN layers have to match [32] (see Figure 2.1). The strain in the basal plane (or in-plane strain) can be then calculated as:

$$\varepsilon_1 = \frac{a - a_0}{a_0} \tag{2.1}$$

where a_0 and a are the lattice constants of an unstrained and a strained structure, respectively.

If it is considered that no force is acting in the c-axis (no shear stresses), the strain along the growth direction ε_3 and in the basal plane ε_1 are related through the expression:

$$\varepsilon_3 = -2\,\frac{C_{13}}{C_{33}}\,\varepsilon_1 \tag{2.2}$$

where C_{13} and C_{33} are elastic deformation constants. As a result, the piezoelectric polarization vector has only the c-axis component and takes the following form when Eq. 2.1 and Eq. 2.2 are replaced:

$$P_{pz} = 2\,e_{31}\,\varepsilon_1 + e_{33}\,\varepsilon_3 = 2\left(\frac{a - a_0}{a_0}\right)\left(e_{31} - e_{33}\,\frac{C_{13}}{C_{33}}\right) \tag{2.3}$$

where e_{33} and e_{31} are the piezoelectric coefficients.

Table 2.2 illustrates the spontaneous polarization and the required parameters to calculate the piezoelectric polarization in AlN, GaN and AlGaN materials. It is worth noting that all parameters depend on the Aluminum concentration within the AlGaN layer. Thus, the higher the Al content, the larger the total polarization $P = P_{sp} + P_{pz}$ in tensile-strain AlGaN [33]. The piezoelectric polarization origin due to the lattice constant match of the AlGaN on top of the GaN layer is graphically

TABLE 2.2: Spontaneous polarization (P_{sp}), piezoelectric coefficients (e_{33} and e_{31}) and elastic deformation constants (C_{13} and C_{33}) for AlN, GaN and AlGaN in function of the Al content (x) [29].

Parameter	*AlN*	*GaN*	$Al_xGa_{1-x}N$
$P_{sp}(C/m^2)$	-0.081	-0.029	-0.052x-0.029
$e_{33}(C/m^2)$	1.46	0.73	0.73x+0.73
$e_{31}(C/m^2)$	-0.60	-0.49	-0.11x+0.49
$C_{13}(GPa)$	108	103	5x+103
$C_{33}(GPa)$	373	405	-32x+405

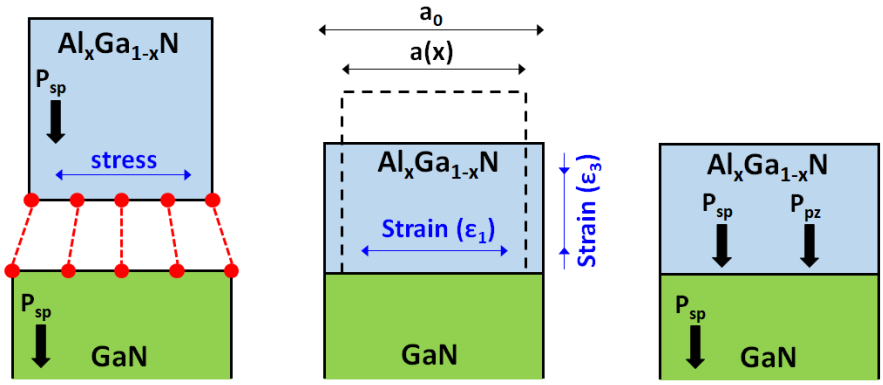

FIGURE 2.4: A simplified representation of the lattice constant match of the AlGaN on GaN layer and its induced strain in the basal plane (ε_1) and in the growth (ε_3) directions, which ultimately causes the piezoelectric polarization.

summarized in Figure 2.4.

The total polarization discontinuity at the AlGaN/GaN heterointerface induces a positive bound charge density (σ_{POL}) that scale with the Al content (x) and is described by the expression:

$$\sigma_{POL} = P_{AlGaN} - P_{GaN} = P_{sp,AlGaN(x)} + P_{pz,AlGaN(x)} - P_{sp,GaN} \tag{2.4}$$

where the argument x is the Aluminum fraction of $Al_xGa_{1-x}N$.

In addition, the bandgap difference between AlGaN and GaN originates a large conduction band offset (ΔE_c), which forms a quantum well at the interface. Due to charge compensation, free electrons attracted by positive polarization-induced charges are therefore well confined in this quantum well forming the spontaneous 2DEG as shown in Figure 2.5. The origin of these electrons has been suggested to come from the donor-like (i.e. neutral when occupied and positive when empty) surface states of the AlGaN layer when the strain-induced polarization field is high enough to modify the band profile and the charge distribution [34]. This is known as the surface model and also explain the 2DEG formation only beyond a critical AlGaN barrier thickness (t_{CR}).

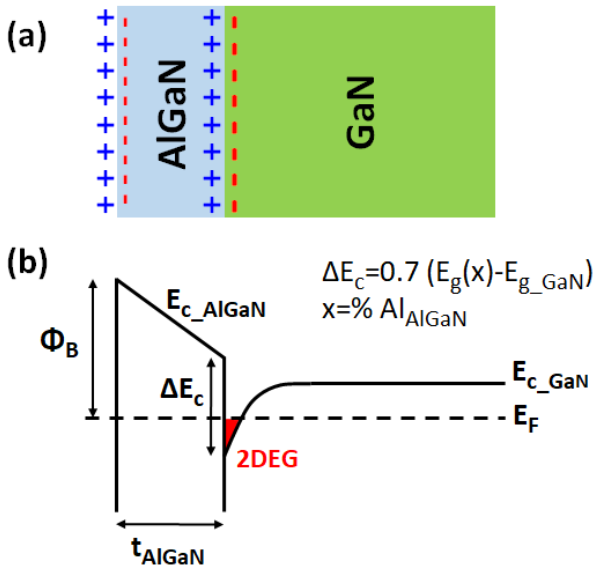

FIGURE 2.5: (a) Simplified scheme of the charge distribution in the AlGaN/GaN heterojunction and (b) the corresponding band diagram, where the interface discontinuity forms the quantum well that confines the 2DEG. Adapted from [35].

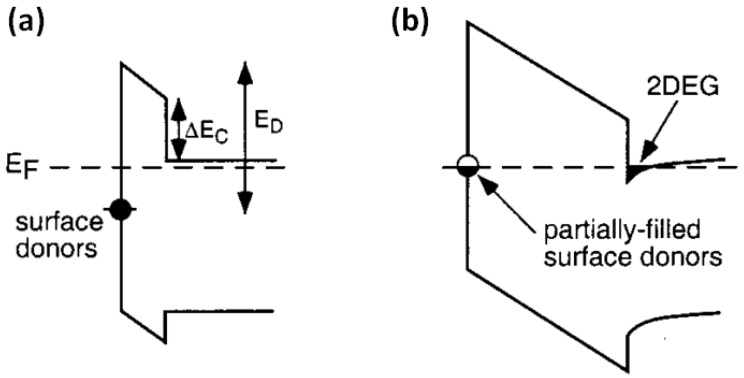

FIGURE 2.6: Schematic representation of the surface donor model when the undoped AlGaN barrier thickness is (a) less than, and (b) greater than the critical thickness for the 2DEG formation (t_{CR}) [34].

As can be seen from Figure 2.6, the surface donor states are fully occupied if the AlGaN thickness is less than t_{CR}. It is just when the AlGaN thickness exceeds the t_{CR} that the donor energy is above the Fermi level and electrons can move to the empty conduction band levels to form the 2DEG.

The t_{CR} is obtained by the following expression:

$$t_{CR} = \frac{(E_D - \Delta E_c)\,\epsilon}{q\,\sigma_{POL}} \tag{2.5}$$

where the E_D is the surface-state energy, ΔE_c the conduction band offset, ϵ the relative dielectric constant of the AlGaN barrier, q the charge of an electron and σ_{POL} the polarization-induced charge at the AlGaN/GaN interface. As can be derived

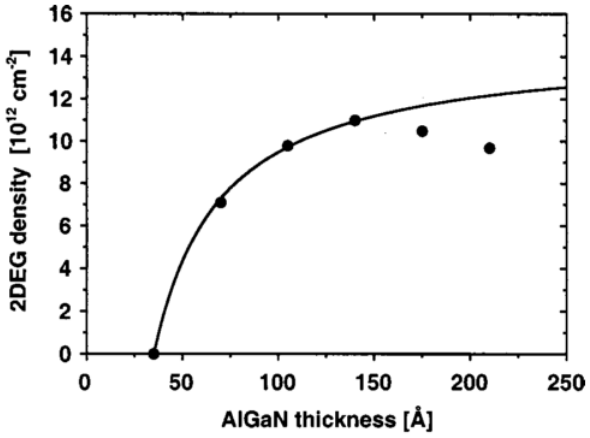

FIGURE 2.7: Room temperature 2DEG density measured as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness. The curve is the least-squares fit of Eq. 2.6 to the $t_{AlGaN} < 150$ Åata [34].

from Eq. 2.5, the larger the value of σ_{POL}, the smaller the t_{CR} that allows the 2DEG formation. In this model, it is also possible to obtain the 2DEG carrier density (n_s), as follows:

$$n_s = \frac{\sigma_{POL}}{q}\left(\frac{1 - t_{CR}}{t_{AlGaN}}\right) \tag{2.6}$$

where t_{AlGaN} is the AlGaN barrier thickness.

Figure 2.7 illustrates the 2DEG density dependence on t_{AlGaN}. Once the critical value t_{CR} is exceeded, the charge density rapidly increases but at a certain point it saturates at σ_{pz}/q for $t_{AlGaN} \gg t_{CR}$.

This model can also be extended to the ideal case with no surface states, so the only available occupied states are in the valence band. Under this assumption, the 2DEG density only appears when the AlGaN barrier thickness allows the valence band to reach the Fermi level at the surface. Hence, the electrons move from the AlGaN valence band to the GaN conduction band, which causes the formation of a surface hole gas. A similar solution of the Poisson equation is also obtained in this case, but the critical thickness is defined by E_{g_AlGaN} (AlGaN bandgap) instead of E_D in Eq. 2.5.

As can be noticed from Eq. 2.4 and Eq. 2.6, the 2DEG density is strongly dependent on the Al content and AlGaN layer thickness. Therefore, higher 2DEG density is ideally expected in a thicker AlGaN barrier with a higher Al percentage. However, the AlGaN barrier suffers from a strain relaxation above a critical thickness, which results in material cracks, and reduction of the piezoelectric component and 2DEG concentration [36]. The Al content also influences the value of this critical thickness; hence, a higher Al content decreases the critical thickness and this trade-off needs to be taken into account in the design of AlGaN/GaN devices (Figure 2.8). The typical range of values of the Al content is from 15 to 35 % for barrier thicknesses between 10 to 30 nm, which still results in a high 2DEG density (about $1 \times 10^{13}\text{cm}^{-2}$) [35].

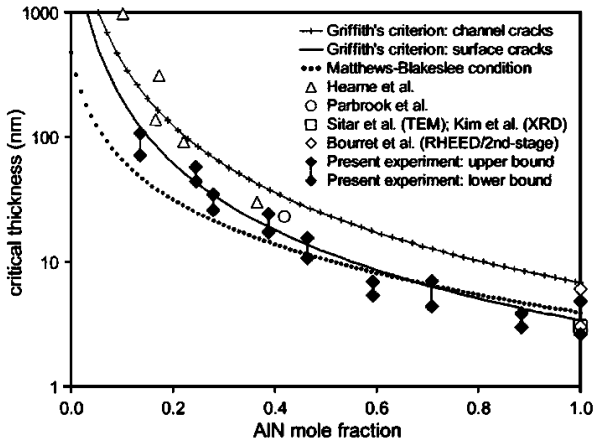

FIGURE 2.8: Comparison of measured and theoretical calculation of the critical thickness for strain relaxation in the $Al_xGa_{1-x}N/GaN$ heterostructure [36].

TABLE 2.3: Comparison of the most important substrate properties for GaN epitaxial growth. It is worth noting that the lattice and thermal mismatch are calculated taking as a reference the GaN-on-GaN substrate.

Substrate	*Lattice Constant (Å)*	*Lattice Mismatch (Å)*	*Thermal Exp. Coefficient* $(10^{-6}K^{-1})$	*Thermal Mismatch (%)*	*Thermal Conductivity (W/cmK)*
GaN	3.19	0	5.6	0	1.3
Al_2O_3	4.75	15	7.5	33.9	0.5
SiC	3.08	-3.5	4.46	-20.3	5
Si (111)	5.43	17	3.59	-35.8	1.5

2.1.3 Substrates

Although the GaN-on-GaN epitaxial growth would be the ideal option because of the lattice match, the lack of a specific technique to easily grow bulk GaN crystals (above two inches) with a competitive cost results in the use of foreign substrates for the fabrication of GaN-based devices. The most common substrates are sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si), resulting in heteroepitaxy. Diamond has also been used due to its high thermal conductivity that allows to rapidly conduct and dissipate the generated heat during device operation [32]. The substrate choice is relevant to obtain high-quality epitaxial layers with low defects concentrations and is based on the lattice mismatch and thermal properties of each material (Table 2.3).

SiC

The high thermal conductivity and the low lattice mismatch makes SiC the most attractive substrate. GaN layers grown on this substrate have demonstrated an excellent crystallographic quality with a dislocation density lower than $3 \times 10^8 cm^{-2}$ by using a nucleation layer of AlN to smooth the transition from SiC to GaN crystal structure [32]. However, SiC substrates are expensive and have low controllability

on the resistivity. Since commercial monocrystalline SiC wafers have just a 3-inch maximum diameter, this option has a less throughput of devices per wafer [37].

Sapphire (Al_2O_3)

The first GaN-based device was grown on a sapphire substrate because of its low price and availability in large-diameter wafers. Even though it is still used in optoelectronics, the poor thermal conductivity limits its use in applications where effective disposal of heat is required (power applications). As a consequence, the self-heating device is easily induced.

Si

Si has a better thermal conductivity compared with Sapphire and offers a reasonable substrate cost. Moreover, its growth process is well known and large diameter wafers are available. This eases the integration of Si-based and GaN-based devices on a single chip. Nevertheless, the large lattice mismatch and the difference of the thermal expansion coefficients cause that GaN grows with tensile stress, which results in a poor crystal quality leading to high dislocation density, pits, and cracks. Similarly to SiC substrates, the GaN-on-Si approach requires to grow an intermediate buffer to gradually accommodate the mismatch between the two different crystal structures. This latter can be done by using multiple step-graded AlGaN buffers [38] or an AlN/GaN superlattice stack [39] as observed in Figure 2.9.

The intermediate buffer is normally fabricated by means of metal-organic chemical vapour deposition (MOCVD) because it provides a relatively high-quality stack, but at the expense of high costs due to the need of additional raw materials. Despite the efforts to grow GaN-on-Si, it is still a challenging process. Therefore, different epitaxial growth approaches are still desirable. In this context, the growth technique on compliant silicon-on-insulator substrates (SOI) by MOCVD is an alternative since it releases the strain between the epilayer and the substrate. As a result, GaN layers grown on SOI exhibit improved crystal uniformity, better surface morphology, and fewer threading dislocations compared with GaN-on-Si [40]. This ultimately improves the device breakdown characteristics, enabling the use of clearly higher voltages in power electronics.

2.2 GaN-based devices architectures

2.2.1 AlGaN/GaN High Electron Mobility Transistors (HEMTs)

The AlGaN/GaN HEMT is a three-terminal device with a Schottky contact in the gate and two Ohmic contacts in the drain and source electrodes that are connected to the channel via a low-resistance path. Unlike the conventional MOSFET, where the current flows between the source and drain terminals through a surface (inversion) charge layer formed due to the electrostatic control exercised by the gate on the semiconductor; in the AlGaN/GaN HEMT, the current flows through the spontaneous two-dimensional electron gas (2DEG) channel formed at the AlGaN/GaN interface (Figure 2.10 (a)). Since high 2DEG density is obtained without adding dopants, there are no scattering phenomena; therefore, increased electron mobility is observed in these devices. The gate bias controls the channel by depleting or enhancing the

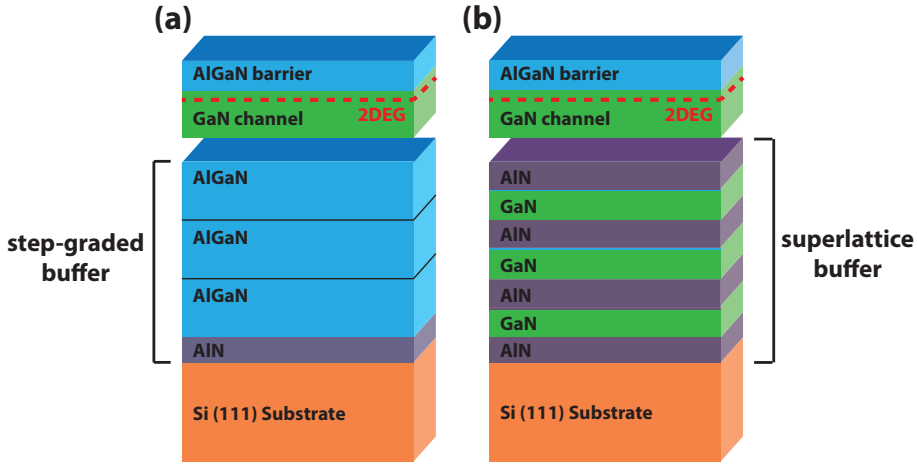

FIGURE 2.9: Structure stack schema with (a) a multiple step-graded AlGaN and (b) an AlN/GaN superlattice buffer.

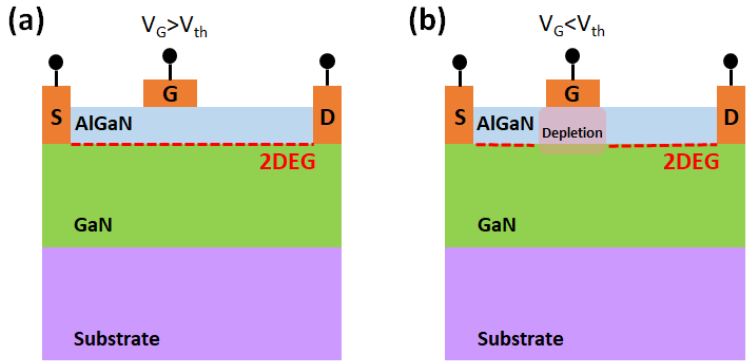

FIGURE 2.10: Simplified structure of an AlGaN/GaN HEMT during its (a) ON-state and (b) OFF-state operation. Adapted from [35].

charge density below the contact, which interrupts or allows the conduction, respectively (Figure 2.10 (b)). It is worth mentioning that GaN-based HEMT exhibits a depletion-mode characteristic (Normally-ON), i.e. it has a negative threshold voltage (V_{th}<0) and thus needs a negative gate voltage to deplete the channel.

Under high drain voltage conditions, the drain edge of the gate is reverse biased with respect to the channel. This results in electron depletion in that region, which causes the position dependence of the channel. Since the current has to remain constant, all the applied additional voltage drops in this high resistive region limiting the breakdown voltage (V_{BD}). By shifting the gate away from the drain helps to reduce the electric field peak at the edge and improves the V_{BD} (Figure 2.10). Nevertheless, a longer gate-to-drain distance negatively impacts on the high-frequency performance of the devices due to a reduced cut-off frequency [32].

Enhancement mode GaN-based devices

As previously mentioned, AlGaN/GaN HEMTs have a depletion mode (D-mode) or normally-ON operation which limit their use in power applications due to safety

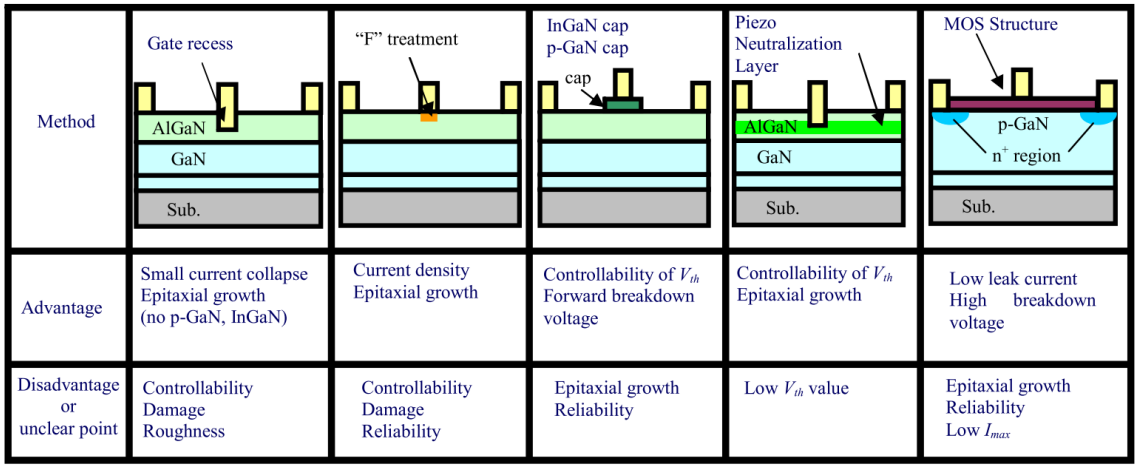

FIGURE 2.11: Aproaches to realize enhancement mode GaN-based devices [41].

reason. Since a two-dimensional electron gas (2DEG) channel is formed at the AlGaN/GaN interface due to intrinsic spontaneous and piezoelectric polarization effects, a negative bias has to be applied at the gate to switch the device off. In order to have an enhanced mode operation (normally-OFF), a possible solution is the use of a normally-ON GaN transistor with a Si transistor in a cascode configuration to benefit of its positive threshold voltage [42]. Although the feasibility of the cascode solution has been demonstrated, it did not find a wide adoption since it adds an extra level of complexity to the device fabrication and it reduces the theoretical performance of a full-GaN device. The other solution is to fabricate true e-mode devices, for instance by using a recessed gate structure [43], a fluoride-based plasma treatment [44], a piezo neutralization technique [45], a p-GaN layer beneath the gate [41], a metal-oxide-semiconductor (MOS) structure [46], among others as depicted in Figure 2.11.

2.2.2 AlGaN/GaN Metal-Oxide-Semiconductor (MOS) and Metal-Insulator-Semiconductor (MIS) HEMTs

The performance of conventional AlGaN/GaN HEMT (Figure 2.12 (a)) is limited by the high Schottky-gate leakage current, which causes the DC/RF parameters degradation. When the gate is positively biased, the high forward gate current can shunt the gate-channel capacitance and consequently limit the maximum drain current. On the other hand, high voltage drops in the region between the gate and drain under a negative gate bias, thus resulting in premature breakdown and limitation of the applied drain voltage [47]. Since AlGaN/GaN HEMTs in power switching applications require a gate bias swing as large as possible to switch rapidly from an OFF- to an ON-state, and by considering that a reduction in the gate leakage current is strictly necessary from the power consumption point of view, a gate oxide (MOS) or a dielectric (MIS) is inserted between the metal gate contact and the heterostructure to overcome these inconveniences (Figure 2.12 (b)). Interesting results in terms of leakage current reduction and drain current increase have been obtained by using different gate dielectrics, such as SiN [48], Al_2O_3 [47], HfO_2 [49], etc.

These structures are normally combined with a recess gate technique since it is considered the most straightforward approach to ensure an enhancement mode as

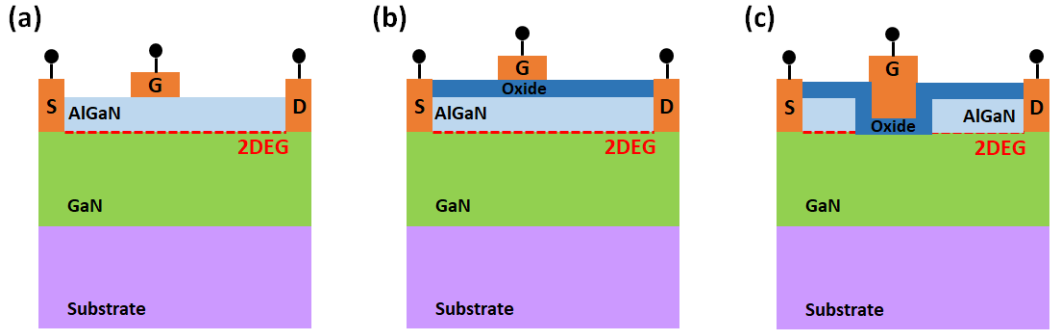

FIGURE 2.12: Schematic structure of (a) a Schottky gate AlGaN/GaN HEMT, (b) a GaN MOS-HEMT, and (c) a fully recessed GaN MOS-HEMT. It is worth mentioning that MOS-HEMT is a specific term when an oxide is used below the gate contact, while MIS-HEMT is the general term for all insulators.

shown in Figure 2.12 (c). By using an etching process, it is possible to reduce the AlGaN thickness below the critical thickness for 2DEG formation (t_{CR}) and deplete the channel. To obtain high threshold voltage (V_{th}) values, a complete etching of the AlGaN barrier and even deep into the GaN channel is preferred even though this increases the ON-resistance (R_{ON}) due to reduced 2DEG density under the gate [50], [35].

2.2.3 AlGaN/GaN lateral Schottky Barrier Diodes (SBDs)

Similarly to the GaN-based transistors, GaN-based Schottky barrier diodes (SBDs) are also promising in the power rectifier market because they benefit from all the characteristics of the GaN and offer fast switching speed, high electric field breakdown, and good thermal properties [51]. The key factors in diode fabrication are to obtain low onset voltage while keeping a low reverse leakage current with a high breakdown voltage. The device used throughout this thesis features symmetric structure with a central anode forming the Schottky contact (metal-semiconductor junction) and two separate cathodes that create the ohmic contacts to the 2DEG as illustrated in Figure 2.13.

During the ON-state operation, the 2DEG is originated due to the intrinsic properties of the AlGaN/GaN heterojunction as previously described in subsection 2.1.2 and the current flow between the anode and the cathode. Under this condition, a vertical polarization field (E_p) appears within the AlGaN barrier as illustrated in Figure 2.13 (a). On the other hand, when the anode is negatively biased (OFF-state), electrons can be injected into the surface traps which are the source of the 2DEG according to the surface-donor model. As a result, the channel is vertically depleted due to a charge neutrality condition. Moreover, the voltage between the anode and the cathode creates a constant electric field (E_x) in the neutral region and the total field in the depletion region is a combination of the lateral and vertical component ($E_{total}^2 = E_p^2 + E_x^2$) as shown in Figure 2.13 (b). When E_{total} is equal to the critical electric field of the AlGaN layer, the device breakdown occurs.

Au-free Gated edge termination (GET) SBDs

Due to the highly resistive AlGaN layer on top of the quantum well formed at the AlGaN/GaN interface, the fabrication of ohmic contacts is really challenging.

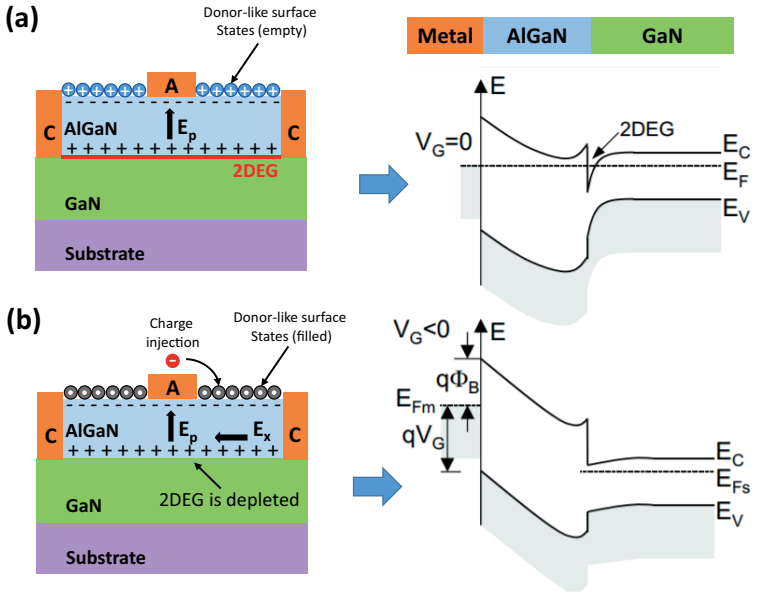

FIGURE 2.13: Schematic illustration of (a) a forward biased and (b) a reverse biased GaN-based Schottky barrier diode (SBD) with their respective band diagrams.

GaN device processing typically includes Ni/Au- or Mo/Au-containing metallization schemes to create ohmic and gate contacts [50]. Within the effort to reduce the fabrication cost of GaN power devices, it is necessary to develop a process compatible with the conventional Si CMOS fabrication flow. Hence, the implementation of Au-free metallization schemes is required to avoid contamination issues of using Au/Pt-based metals.

Au-free Ti/Al/TiN-based ohmic contacts with a low annealing temperature have been developed by imec and used in this work [52]. Since the used thermal budget can still affect the diode leakage current (ohmic contacts are processed after the anode) and by considering that the Au-free anode is not ideal for Schottky contacts, a special gated edge termination (GET) is fabricated around the Schottky junction to tackle these inconveniences [51]. As can be seen from Figure 2.14, the GET is embedded inside the anode trench, which results in a remarkable leakage current reduction at high voltage without any significant variation in the forward current compared with a conventional SBD as depicted in Figure 2.15.

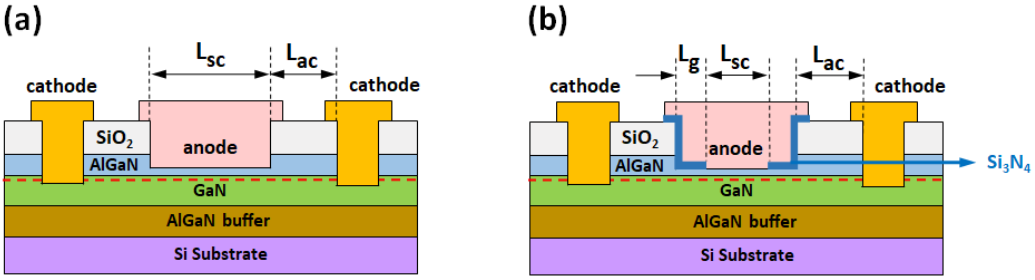

FIGURE 2.14: Schematic representation of (a) the conventional SBD and (b) the GET-SBD with a recessed AlGaN barrier to further reduce the reverse leakage current [53].

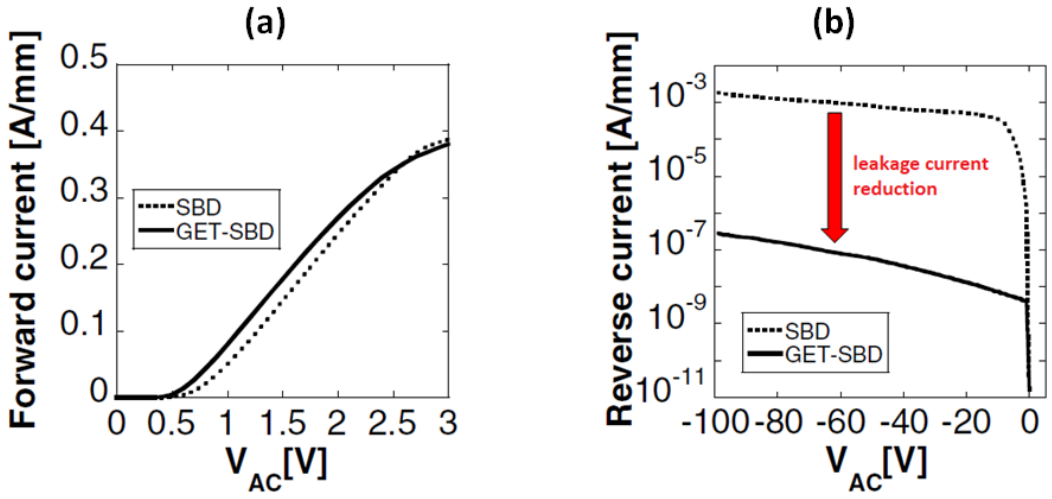

FIGURE 2.15: (a) Forward and (b) reverse DC curves of the GET-SBD (solid lines) and the conventional SBD (dotted lines), both with an anode finger width of 100 um [51].

2.3 Issues and failure mechanisms in GaN-based devices

2.3.1 Self-Heating

The strength of GaN-based devices is their capability to operate at high voltages but as a counterpart, high electrical fields and current densities are induced causing strong self-heating effects related to power dissipation problems [54]. Some of the inconveniences of device self-heating include the lattice temperature increase and the carrier mobility reduction because of the enhanced phonon scattering [55]. The substrate material determines the performance in high power operation; thus, a higher thermal conductivity is preferable to dissipate as much heat as possible.

By using micro-Raman spectroscopy [56], it was demonstrated that the temperature increase on Sapphire substrate is faster than on SiC and with a higher reached temperature. Moreover, it was found that temperature changes rapidly within sub-200 ns after switching the devices on or off, which affect not only the DC operation but also the RF or pulsed operation. A comparative study of different substrates (SiC, sapphire, Si, and GaN) by using electro-thermal Monte Carlo method showed that the SiC substrate exhibits the highest current and the lowest peak temperature, which make it more suitable for high-power applications. It was also demonstrated that the self-heating phenomenon is responsible for the observed current saturation in I-V characteristics at a much lower electric field than for the saturation of electron drift velocity in the bulk GaN [57]. Therefore, thermal effects play a significant role in the GaN-based HEMT performance for high power applications.

2.3.2 Trapping Effects

The presence of trapping states is an enormous limitation in the performance of GaN-based devices. At the early stages of GaN technology, devices exhibited a significantly reduced output power compared with the theoretical value estimated with DC data because the drain current decreases from DC to pulsed conditions. This

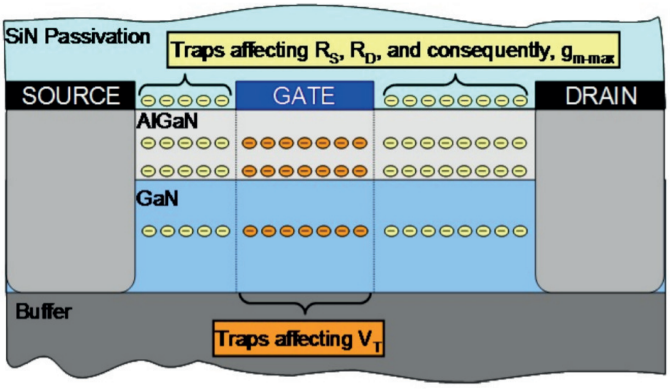

FIGURE 2.16: Possible traps position inside the AlGaN/GaN HEMT and their related effects [58].

phenomenon was attributed to parasitic traps (energy states inside the energy gap that can trap electrons or holes) within the device. The origin of these traps are related to the creation of defects in the crystal lattice during the growth process, the mismatch between the different layers, surface damages caused by process treatments, impurities in the crystal structure, etc.

Apart from the pre-existing traps, trapping states can also be created during a particular stress condition or operation point due to the presence of high electrical fields or high-energetic hot-electrons in the channel. The location of the parasitic traps is also relevant since a correlation with the type of degradation such as the reduction in the DC performance, the dynamic transconductance or the RF output power has been reported in the Literature [58]. Figure 2.16 depicts a schematic AlGaN/GaN HEMT with the possible locations of the traps and their related effects. Some of the issues derived from trapping states are the kink effect and the current collapse and they will be explained in the following.

The kink effect

The kink effect is a detrimental phenomenon in which an abrupt increase in drain current at a certain drain bias (V_{DS_kink}) is observed, possibly resulting in an output conductance increase, transconductance compression, and dispersion between DC and RF characteristics. This effect occurs at different conditions and seems to be related to carrier trapping although a complete consensus about the origin is not available yet. Some of the possible explanations are hole accumulation due to channel impact ionization, field-dependent deep level traps, or a combination of both mechanisms [59]. The strong dependence of the kink effect on the illumination and temperature supports the presence of traps in the buffer or in the AlGaN barrier beneath the gate contact [60]. Figure 2.17 illustrates the DC characteristics of an AlGaN/GaN HEMT, where the kink effect is visible when the applied V_{DS-max} is high. Another way to easily observe this phenomenon is to perform normal DC characterization by using different integration times [37].

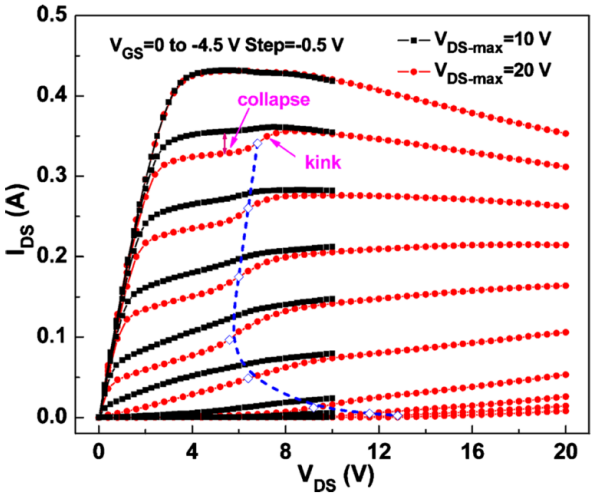

FIGURE 2.17: Transistor output characteristics measured at two different values of V_{DS-max}. The dashed line indicates V_{DS_kink} at each V_{GS} [61].

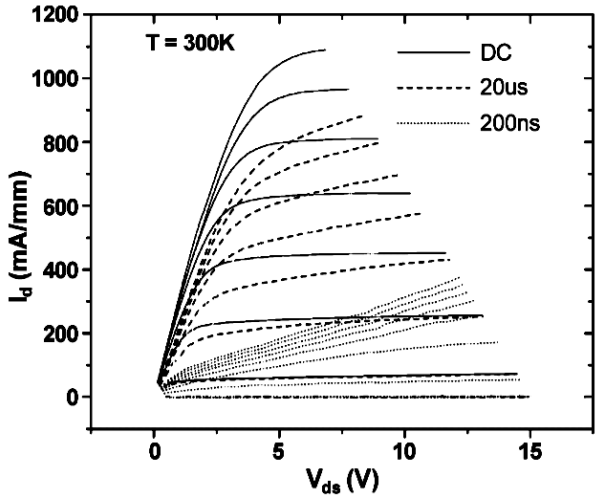

FIGURE 2.18: DC and pulsed I-V characteristics of an unpassivated AlGaN/GaN HEMT on SiC substrate. Current collapse could be observed in the pulsed mode [62].

Current collapse

Current collapse is a degradation of the drain current when pulse characteristics are compared with DC measurements as depicted in Figure 2.18. It is also known as current slump/ compression, (DC-to-RF) dispersion, or dynamic Ron since an increase of the access resistance is observed. This decrease in the drain current also leads to a reduction of the output power (P_{out}) and power added efficiency (PAE).

This degradation phenomenon has been attributed to the accumulation of negative charges on the surface traps, which causes a charge variation in the GaN channel. The negative charge could be originated from the gate by electron tunneling since a high electric field is located at the drain edge of the gate [64], or from the channel when hot electrons overcome the AlGaN barrier under high drain bias condition [65]. This negative charge is then trapped by the donor-like states (positive when empty) on the surface which makes them neutral. It is worth noting that the initial

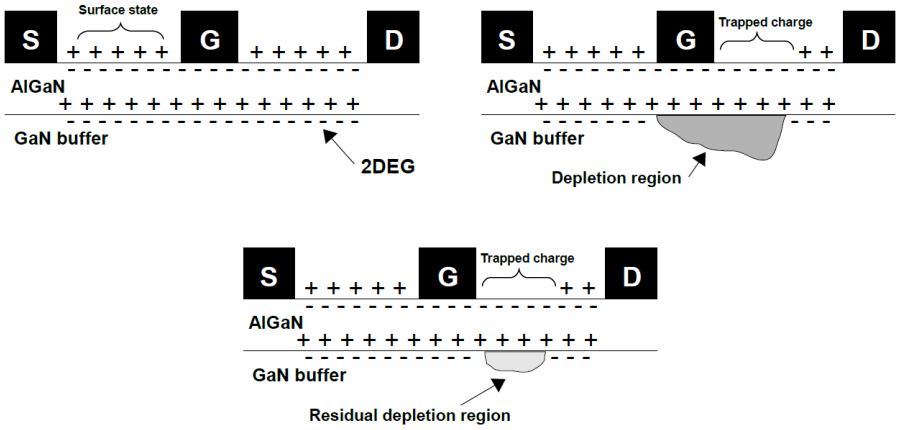

FIGURE 2.19: Schematic representation of current collapse. Initially, surface donors are positively charged (ON-state). After electron trapping, surface donors become neutral and creates an extension of the depletion region (virtual gate) (OFF-state). Finally. the captured electrons keep the channel partially depleted (ON-state) [37].

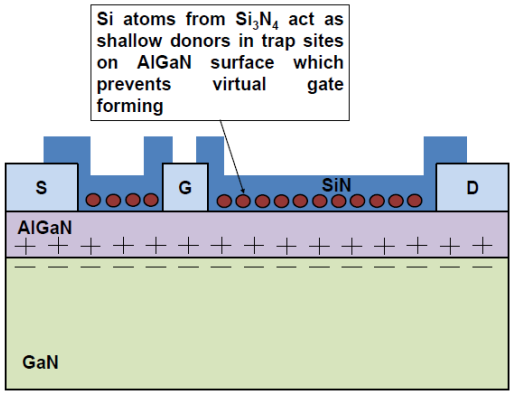

FIGURE 2.20: Schematic structure of a passivated AlGaN/GaN HEMT by using Si_3N_4 to prevent a virtual gate formation [63].

positive-charge states allow the negative charge balance of the 2DEG as explained in subsection 2.1.2. Therefore, in the absence of these positive surface charges, there is an extension of the depletion region. Under this condition, two gates control the current along the channel. The normal gate which depends on the applied gate bias and the virtual gate which is controlled by the amount of charge trapped on the surface states as observed in Figure 2.19. When the device is turned-ON, the normal gate opens the channel, but the virtual gate keeps the channel partially turned-OFF because the trapped charges are not immediately released. As a result, the virtual gate introduces a delay that depends on the de-trapping transient of the surface traps.

In order to reduce the impact of surface states that create the virtual gate, a passivation layer of dielectric material has been demonstrated as a preventative technique [64]. In special, Si_3N_4 is generally used because its Si atoms act as shallow donors in trap states on the AlGaN surface as shown in Figure 2.20. Thus, the insertion of this layer minimizes the electrons capture from the gate and enhances the 2DEG enabling larger output currents.

A second technique to reduce the current collapse due to surface states is the engineering design of the gate electrode to better distribute the electric field along the gate-to-drain region. The more complex gate configurations include a T-gate or a Γ-gate shape which extend the upper part of the gate to partially cover the gate-source and/or gate-drain regions. These configurations are also known as field plates and aim to decrease the electrical field peaks at the gate edges (especially at the drain side), which occur when the device is submitted to high voltages (OFF-state condition). Therefore, fewer electrons are captured into the surface states because of the lowered electric field [66].

Apart from the surface states, the current collapse has been also attributed to channel depletion due to injection and trapping of hot electrons in GaN buffer. Binari *et al.* reviewed bulk trapping effects in AlGaN/GaN HEMTs and reported that these bulk traps are deep and have their origin from compensation doping (carbon), which is used to make highly resistive or semi-insulating buffer [67]. Some solutions include the addition of a very thin small bandgap material (InGaN) between the 2DEG and GaN buffer for a higher back-barrier [68], N-faced HEMTs with AlN-GaN spacer to a better 2DEG-confinement [69], and improvements in growth technology.

2.3.3 Reliability-related issues in GaN-based power switching devices

The reliability of semiconductor devices strongly depends on some fabrication aspects such as undesirable impurities due to the multiple-step process, thin layers deposition, new material introduction, environmental conditions, assembly, etc., which ultimates induce or accelerate the failure mechanisms affecting the device lifetime [70].

Therefore, the design of more efficient, robust and reliable power devices requires the understanding of the different degradation and failure phenomena that take place within the GaN-based structures under operating conditions to ensure a lifetime usually ranged between 10 and 20 years. For this reason, different reliability tests have been performed by using accelerated factors (temperature, voltage, humidity) that allow extracting the expected lifetime in a feasible time with the adoption of extrapolated methods.

As previously discussed, the core of a variety of power applications is power conversion systems in which semiconductor devices are rapidly switching from an OFF-state to an ON-state condition. Consequently, the stability of GaN technology needs to be verified in these operating points including a SEMI-ON state that takes place in the transition. In the following, the impact of the device operating mode on the reliability-related issues is summarized by considering the boost converter described in section 1.2.

OFF-state related reliability issues

During the OFF-state operation mode of the converter in Figure 1.4, the transistor is reversely biased whereas the diode is in a forward regime. On the one hand, the conducting diode has to handle high forward currents, which in conjunction with the moderate electric field and high junction temperature generate repercussions on

its reliability [70].

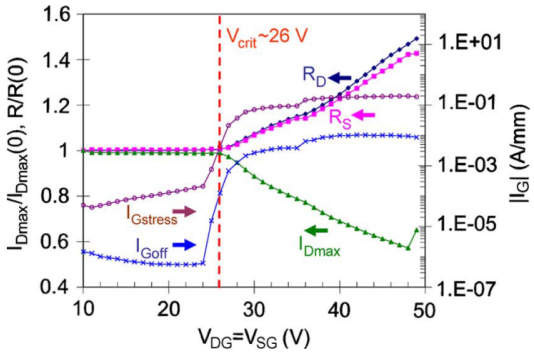

FIGURE 2.21: Normalized I_{Dmax}, R_D, R_S, $I_{Gstress}$, and I_{Goff} variation as a function of stress voltage in a step-stress experiment under $V_{DS} = 0$ ($V_{DG} = 10 - 50$ V in 1 V steps) [71].

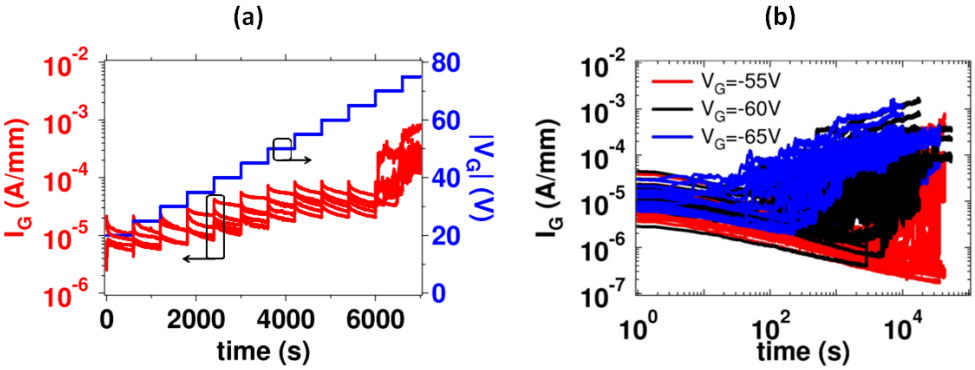

FIGURE 2.22: (a) Reverse gate step-stress test on five devices with a gate-to-drain distance of 0.7 μm where a $V_{CRITICAL} = -70$ V was measured. (b) Gate current degradation by using stress gate voltages lower than the $V_{CRITICAL}$ [72].

On the other hand, the transistor is submitted to a high drain bias, which promotes the degradation mechanisms such as the previously mentioned current collapse, high leakage current, and gate degradation. The last two are the result of applying a high reverse bias voltage to the gate since it increases the drain and source parasitic resistance causing an increment in the gate leakage and a reduction of the saturation current (I_{DSS}) as shown in Figure 2.21. This phenomenon has been mainly attributed to the defect creation below the gate edge within the AlGaN barrier, where the electric field is the highest, once the elastic energy present in this layer exceeds a critical value. This degradation mechanism is known as inverse piezoelectric effect and is studied by a step-stress test (Figure 2.22 (a)), where is possible to identify the so-called critical voltage ($V_{CRITICAL}$) under which the devices can indefinitely operate without degradation [71]. However, Marcon *et al.* [72] reported a time-dependent gate degradation even below the $V_{CRITICAL}$ (Figure 2.22 (b)), which is strongly voltage-accelerated with a weak temperature influence.

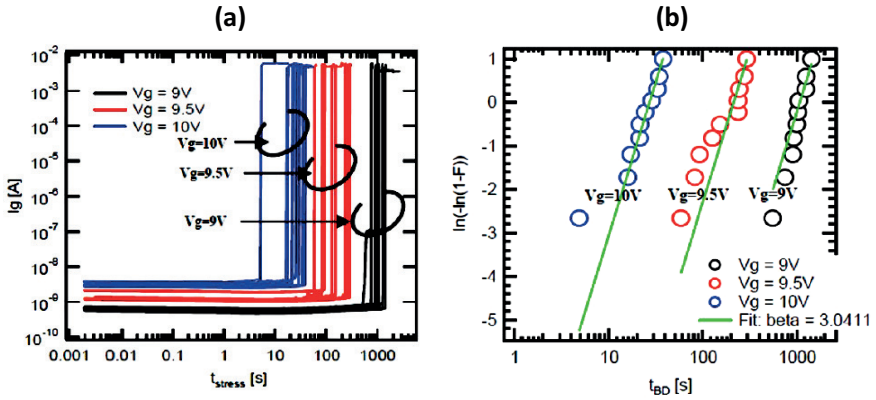

FIGURE 2.23: (a) Gate current monitored during TDDB experiments with three different stress voltages. (b) The corresponding distribution of the time to breakdown, which follows Weibull statistics [35].

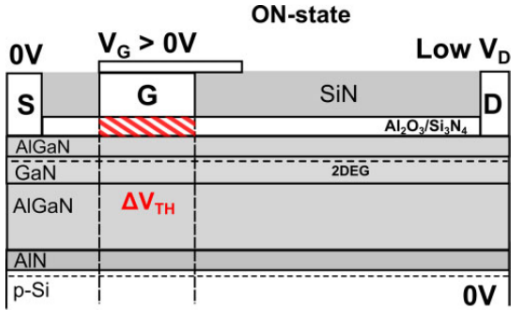

FIGURE 2.24: During ON-state regimes, the positive voltage applied to the gate stack favors the electron capture into the trap-states of the dielectric causing ΔV_{th} [73].

ON-state related reliability issues

Under this operation mode, the transistor is in an ON-state condition while the diode is reversely biased. Therefore, the diode has to tolerate a high reverse voltage in this case. Because of the high induced electric fields, similar reliability issues as in the OFF-state transistor are observed, i.e. an increase in the leakage current, defect generation in the AlGaN layer, time-dependent degradation, etc.

The reliability studies during the ON-state operation of a transistor have demonstrated that there are two important issues related to the positive bias applied at the gate electrode and the high current flow that the device tolerates during this condition. The first one is the forward gate bias time-dependent breakdown (TDDB), which especially evaluate the gate dielectric strength in the case of the MIS- and MOS-HEMTs to further estimate the device time-to-failure as depicted in Figure 2.23. The stability of the Schottky gate contact in the regular HEMTs could also be investigated, but this structure attracts little attention for efficient power converters since it exhibits a high conductive gate current even at low gate bias. The second issue is the instability of the threshold voltage (ΔV_{th}) which is related to trapping/de-trapping phenomena within the gate dielectric or at the interfaces as shown in Figure 2.24.

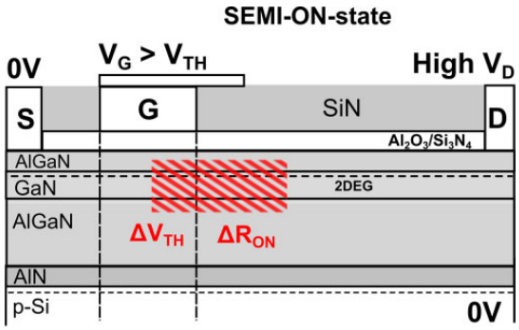

FIGURE 2.25: The combination of high drain voltage and relatively high drain current during the SEMI-ON state allows the hot-electron injection and trapping into epitaxial defect-state [73].

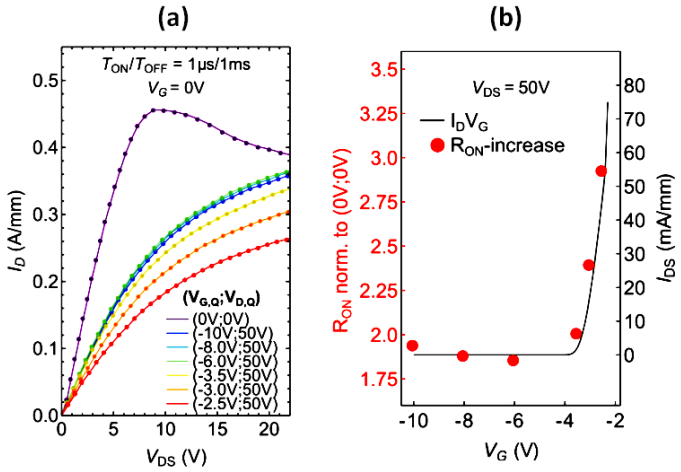

FIGURE 2.26: (a) Pulsed I_D–V_D characteristics acquired with constant quiescent V_{DS}, and multiple quiescent V_G. Dynamic R_{ON} worsens as $V_G > V_{th}$. (b) The good correlation between I_{DS} and dynamic R_{ON} increase suggests hot-electron-related trapping mechanisms [73].

SEMI-ON state related reliability issues

This condition appears during the OFF- to ON-state transition of the switching devices. Therefore, the device shortly operates at both a relatively high voltage and high current. This operating mode accelerates the electrons present in the channel due to the applied electric field, which makes them highly energetic electrons or "hot electrons" and not only causes long-term reliability issues [65] but also enhances trapping mechanisms in the gate-to-drain access region and beneath the gate region, as illustrated in Figure 2.25. It has also been demonstrated that SEMI-ON state worsens the dynamic R_{ON} above normal degradation values observed during the OFF-state, as depicted in Figure 2.26.

2.4 Summary of this chapter

Gallium Nitride is a wide-bandgap semiconductor that with an ideal fabrication offers excellent characteristics: high operating temperature, high dielectric strength, high current density, high switching speed, and low on-resistance. One of the worst inconveniences of AlGaN/GaN High Electron Mobility Transistors (HEMTs), from

the power conversion point of view, is the normally-ON operation since a two-dimensional electron gas (2DEG) channel is naturally formed at the AlGaN/GaN interface due to intrinsic spontaneous and piezoelectric polarization effects. Therefore, GaN-based devices with different process treatments and structure variations have been processed and investigated to overcome this limitation.

In the specific case of power converters, GaN-based devices are continuously switching from an OFF-state condition at high drain bias to an ON-state condition at large drain current with a transition for the so-called SEMI-ON state. Since the operation mode influences in the apparition of different degradation issues, the reliability of GaN-based devices has to be proven for the complete ON-to-OFF switching cycle. Although reliability-related issues have been widely studied in GaN transistors and diodes, the lack of consensus about the degradation phenomena requires more investigation in this field until a complete comprehension about the failure mechanisms will be well understood as in the case of Si technology.

Chapter 3

Reliability study of MOS-HEMTs

3.1 On the recoverable behavior of PBTI in AlGaN/GaN MOS-HEMT

3.1.1 Introduction and state of the art

As previously explained in section 2.2, the basic structure of an AlGaN/GaN HEMT uses a Schottky barrier at the gate to control the depletion of the 2DEG channel, which is naturally formed due to the inherent characteristics of the AlGaN and GaN materials. These devices can realize ultra high-power-density operation since high carrier mobility in the channel and high breakdown voltage due to a large critical electric field are observed. Therefore, high-efficiency power amplifiers have been demonstrated by using this structure [74].

However, for the power electronics applications, the AlGaN/GaN HEMT exhibits a high reverse Schottky-gate leakage current limiting the performance and reliability of these devices. As a result, the OFF-state loss is increased at the power supply system and the power efficiency is reduced. Furthermore, experimental results show that a larger leakage current is related to a lower breakdown voltage since an avalanche injection mechanism is enhanced [75]. The leakage current also influences the subthreshold slope and the ON/OFF drain–current ratio since a linear relationship has been observed [76]. Additionally, Schottky gated HEMTs are also limited when a forward gate bias voltage is applied because a high conductive gate current is present even under a low gate bias. The observation of a high gate leakage current has been attributed to the influence of surface charges at the AlGaN layer, which increments the electric field beneath the gate electrode, thins the AlGaN thickness and generates a large tunneling current as depicted in Figure 3.1.

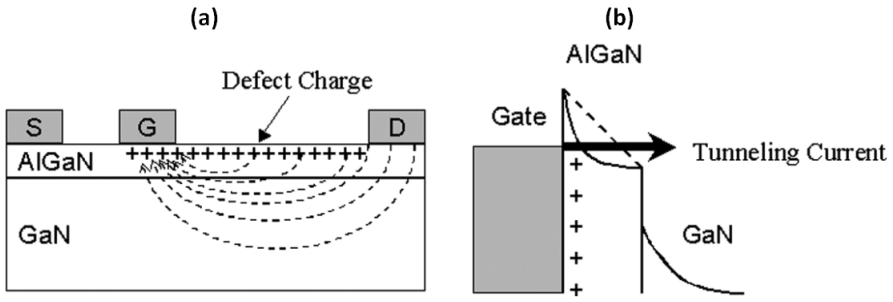

FIGURE 3.1: Physical model of the influence of surface defect charges at AlGaN/GaN HEMT. (a) Electric field concentration at the gate edge. (b) Schottky barrier thinning [75].

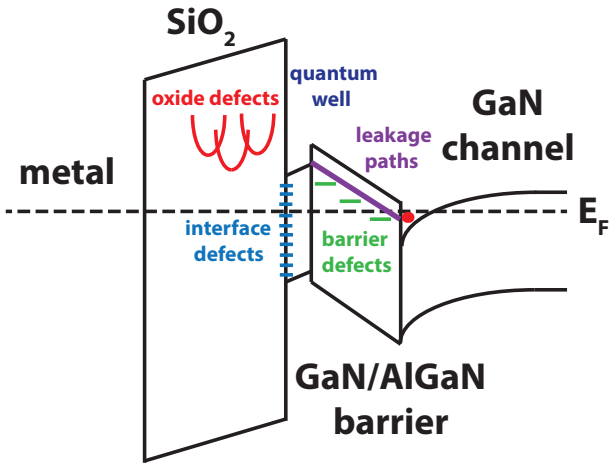

FIGURE 3.2: Overview of potential defect centers in the SiO_2/barrier gate-stack of a GaN-based HEMT device [77].

In an effort to solve the aforementioned leakage-related issues, a metal-oxide-semiconductor structure has been adopted with a recessed gate approach to additionally obtain the normally-OFF operation by reducing the AlGaN thickness below the critical value (t_{CR}) that allows the 2DEG formation. This results not only in gate leakage reduction but also in drain current increase [47].

Nevertheless, an inconvenience affecting the performance of the MOS-structure is the bias temperature instability (BTI), i.e. degradation of electrical parameters (such as threshold voltage and charge carrier mobility) induced by the application of high positive/negative gate voltages and high temperatures. This phenomenon has been extensively studied in CMOS devices for logic applications [78–80] and constitutes the foundation for reliability studies in newer III-V material systems. Some of the popular theoretical models for the negative-bias temperature instability in Si CMOS technology are the reaction-diffusion model (R-D model) [81], the elastic hole trapping [82] and switching oxide traps theory, where NBTI is attributed to charge trapping and de-trapping in the oxide during the stress and recovery phases [83]. More recently, AlGaN/GaN MOS- or MIS-HEMTs have been also analyzed showing that different bias conditions induce varying degrees of V_{th} shifts [84], [85]. CET maps have also been adopted to demonstrate traps with a broad distribution of time constants [86], [77], but a complete consensus about the nature of the defect states has not been achieved. Since the structure of the gate stack is complex due to multiple layers and interfaces, it is challenging to isolate trapping effects from different layers and trapping sites. Figure 3.2 depicts the complexity of the trapping sites located in the energy band diagram of a MIS-HEMT structure. Normally, these oxide bulk defects, oxide/GaN interface traps, and AlGaN barrier layer defects are suggested to contribute to V_{th} drift. Since parasitic transport and charge trapping mechanisms play an important role in BTI of GaN-based devices, the impact of different gate dielectrics (oxides, nitrides, and high-κ dielectrics) have been investigated in the MOS/MIS-structure to understand the physics associated with the defects responsible for this phenomenon (spatial and energy distribution) [87].

In [88], it was recently conducted a correlation study between 1/f noise and BTI degradation in AlGaN/GaN MOS-HEMTs with a SiO_2 layer deposited by plasma

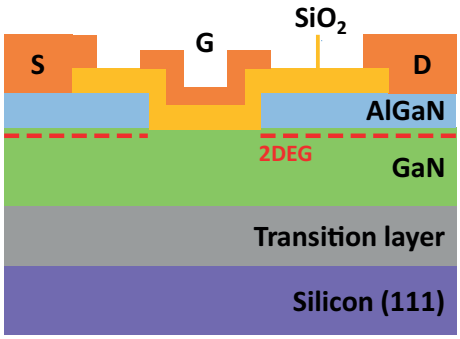

FIGURE 3.3: Schematic structure of the device under test (DUT).

enhanced chemical vapour deposition (PECVD). Crupi *et al.* found out that defects originating 1/f noise are responsible for a significant dispersion in the fresh threshold voltage, while different defects (perhaps with different energy or spatial localization) lead to BTI effect. Following these results, the first part of this chapter aims to carry out a more comprehensive analysis of BTI on such devices, by evaluating and modeling the influence of positive stress voltage and temperature on the threshold voltage shift. Moreover, time constants and activation energies of traps involved during BTI are also analyzed. Even though AC measurement techniques have been proposed to capture the behavior of fast traps [89], this work focuses on the study of the slow components of the threshold voltage degradation by using DC characterization.

3.1.2 Device structure and experimental setup

The structure of the AlGaN/GaN MOS-HEMT studied in this work is shown in Figure 3.3. It is grown $Al_{0.25}Ga_{0.75}N$/GaN heterostructure on 150 mm Silicon (111) substrates in a metalorganic chemical vapour deposition (MOCVD) reactor. First of all, the ohmic contacts were formed evaporating the Ti/Al-based metallizations and carrying out rapid thermal annealing at 850 °C [90]. After that, the recession of the AlGaN layer was performed with a dry chemical process based on chlorine to ensure a normally-off operation. The 50 nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapour deposition (PECVD) by using a tetraethyl orthosilicate precursor, followed by thermal annealing at 850 °C in N_2 [88]. Gate contacts were evaporated on the SiO_2 by using Ni-based metals [30]. The devices under test have a gate length (L_g) of 2 μm, a gate width of 400 μm, and gate-source (L_{gs}) and gate-drain (L_{gd}) distances of 1.5 μm and 16 μm, respectively.

In order to study the complete dynamics of the trapping and de-trapping process in MOS-HEMT devices, a set of stress-recovery experiments was performed at different stress voltages and temperatures with the parameter analyzer Keithley 4200-SCS. All measurements were done at high temperatures ranging from 75 °C to 190 °C and with V_{DS} = 50 mV. The threshold voltage is determined using the fixed current criterion at 10 μm. The adopted measurement procedure consists of three phases: initial stabilization, stress, and recovery.

Initial stabilization

The initial stabilization is performed by applying a negative gate bias (typically -1 V) for 3000 s at 150 °C. During this phase, the virgin device is stabilized by releasing

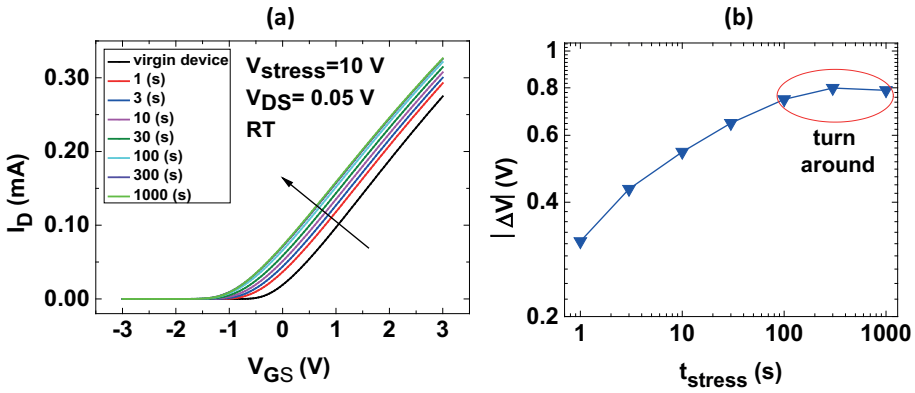

FIGURE 3.4: (a) I_D-V_{GS} curve evolution and (b) ΔV_{th} behavior during a stress test without an initial stabilization phase at room temperature (RT). It is worth noting that V_{th} initially moves to more negative values, then it saturates and turns around.

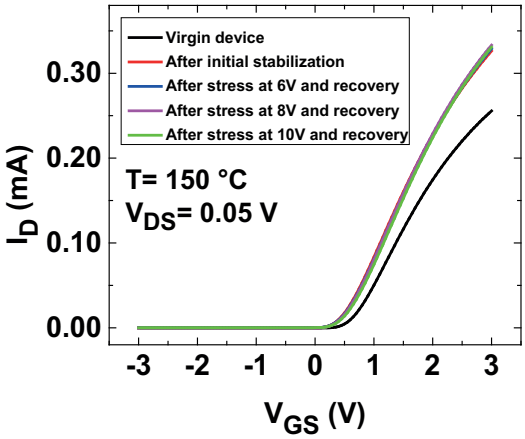

FIGURE 3.5: Transfer curves in the linear regime for a virgin device, after the initial stabilization and after successive stress-recovery experiments. No permanent damage is observed for the investigated stress voltages after the recovery phase.

the charges originally contained in trapping centers [84] [85]. It is worth noting that without applying the initial stabilization, positive and negative ΔV_{th} were observed in different samples and under different stress conditions, due to the concomitant charge trapping and releasing during the stress test. As an example (Figure 3.4), a stress voltage of 10 V was applied to a virgin device without stabilization at room temperature, the threshold voltage moves to the left side (de-trapping of electrons) until a saturation point in which the movement turns around. Therefore, this initial treatment allows us to rapidly release electrons originally trapped and have a reproducible reference curve.

After this phase, a complete I_D-V_{GS} curve sweeping V_{GS} from -3 V to 3 V is recorded. It was necessary to measure the curve up to 3 V, which is significantly higher than the V_{th} in a fresh device, in order to be able to capture the V_{th} after stress also in the case of high ΔV_{th} shifts. As shown in Figure 3.5, the I_D-V_{GS} curve after the initial stabilization is significantly different from the measured I_D-V_{GS} curve in a virgin device. This stabilization is also performed each time that we change the

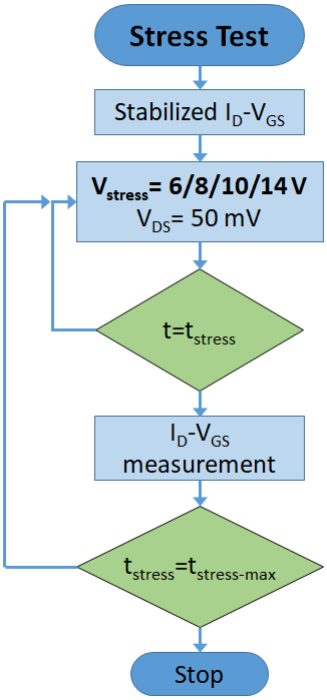

FIGURE 3.6: Testing procedure for the positive bias temperature instability (PBTI) analysis.

temperature because it allows the device to reach a reproducible reference state for the subsequent experiments. As a matter of fact, after the recovery stage following the stress phase for different stress voltages, the I_D-V_{GS} curve always comes back to this reference state.

Stress test

The stress phase begins with the measurement of the I_D-V_{GS} curve (reference) in the previously stabilized device. Secondly, the device is biased with a positive gate voltage (V_{stress}) ranging between 6 V and 14 V. Temperatures above 190 °C and higher voltages were not used in order to avoid oxide breakdown. Thirdly, in order to monitor the evolution of the stress-induced degradation, the stress is interrupted at fixed time intervals and an I_D-V_{GS} curve is measured and compared with the reference curve to calculate ΔV_{th}. Finally, the test stops when all the stressing periods of time have been completed as illustrated in Figure 3.6.

Recovery test

Immediately after the stress phase, the recovery phase is executed by biasing the device with a gate voltage ($V_{recovery}$) ranging between 0 V and -2 V for at least 1000 s. Also in this phase, in order to monitor the recovery evolution, the measurements are interrupted at fixed time intervals and an I_D-V_{GS} curve is measured and compared with the reference curve obtained in the stabilization step. Figure 3.5 illustrates that by applying the recovery procedure after the stress, the I_D-V_{GS} curve comes back to the initial stabilized state indicating that no permanent damage was introduced during the stress phase. It is worth noting that the absence of permanent damage is

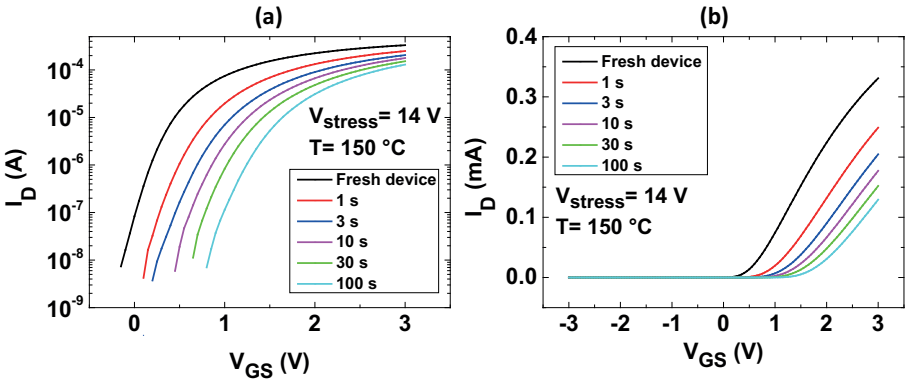

FIGURE 3.7: I_D-V_{GS} curves before (the initial stabilization was applied in the fresh device) and after successive stress experiments at V_{DS} = 50 mV and high temperature in (a) a log-linear scale and (b) a linear-linear scale. The observed positive ΔV_{th} shift indicates electron trapping.

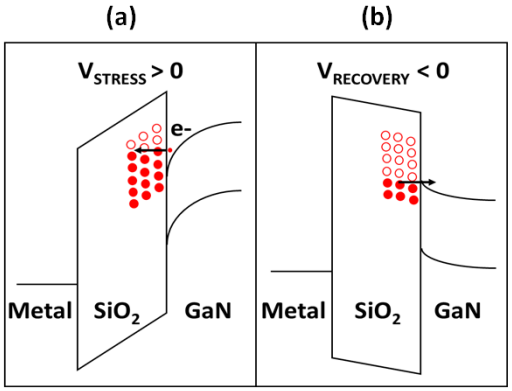

FIGURE 3.8: Sketch of the band diagram for the stress phase (a) and the recovery phase (b). During the stress phase, electrons from the 2DEG channel are trapped into the oxide traps, while during the recovery phase; electrons are released from the oxide traps.

related to the investigated gate voltage values during the stress (from 6 V to 14 V) and it cannot be extended to higher gate voltages.

3.1.3 Stress phase results and discussion

Figure 3.7 depicts the evolution of the I_D-V_{GS} curves during the stress phase in the case of a representative sample. It can be seen that after each stress interval, the I_D-V_{GS} curve moves toward the positive VGS direction, showing the notorious threshold voltage shift. The observed ΔV_{th} shift can be ascribed to the electron trapping from the channel (beneath the gate oxide) into the traps located in the SiO_2 energy gap as observed in Figure 3.8 (a)). The ΔV_{th} results during the stress at different stress voltages and temperatures are also illustrated in Figure 3.9. In order to determine the ΔV_{th} evolution, we evaluated the trapping rate parameter defined as follow:

$$b = \frac{\partial_{log}\left(\Delta V_{th}\right)}{\partial_{log}\, t} \tag{3.1}$$

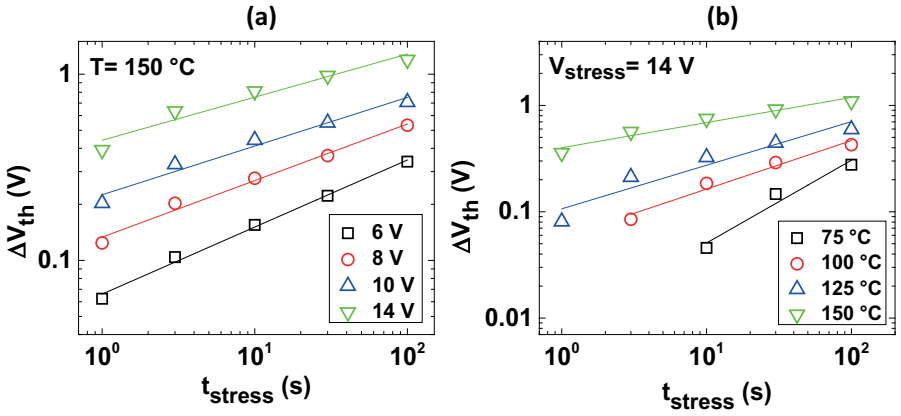

FIGURE 3.9: Experimental (markers) and power-law fitting curves (lines) of the Δ_{th} evolution during the stress phase at different stress voltages (a) and temperatures (b). In the investigated time window, an apparently good fitting with the classic power law model is observed.

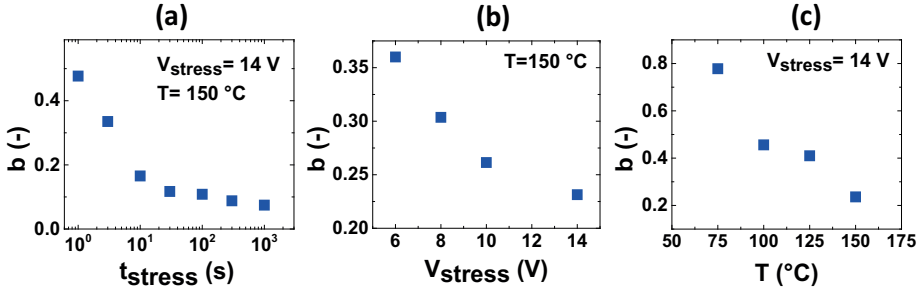

FIGURE 3.10: The trapping rate parameter (Eq. 3.2) significantly decreases during the stress time (a), and by increasing stress voltage (b) and temperature (c).

It can be noted that if b is constant, ΔV_{th} evolution follows a classic power law function, i.e. $\Delta V_{th} = a \times t_{stress}^{b}$ [91] [92]. Nevertheless, as shown in Fig. (Figure 3.10 (a)), the trapping rate parameter significantly decreases during the stress, thus indicating that ΔV_{th} evolution does not follow a power law. Fig. (Figure 3.10 (b)) and (Figure 3.10 (c)) also illustrates that b considerably declines by increasing stress voltage and temperature.

In order to understand the physics behind these phenomena, the trapping rate parameter b, which is a measure of the PBTI charging rate, is plotted as a function of the number of trapped charges per unit area ΔN_{OT}. Different experimental conditions, i.e. time, voltage and temperature, and different samples were also used as illustrated in Figure 3.11. The density of trapped charges has been estimated by using the following expression:

$$\Delta N_{OT} = \frac{(C_{OX} \times \Delta V_{th})}{q} \tag{3.2}$$

where C_{OX} and q are the oxide capacitance per unit area and the elementary charge, respectively.

The overall measurement results illustrate a universal decreasing behavior of the charging rate as a function of the number of filled traps independent of stress time,

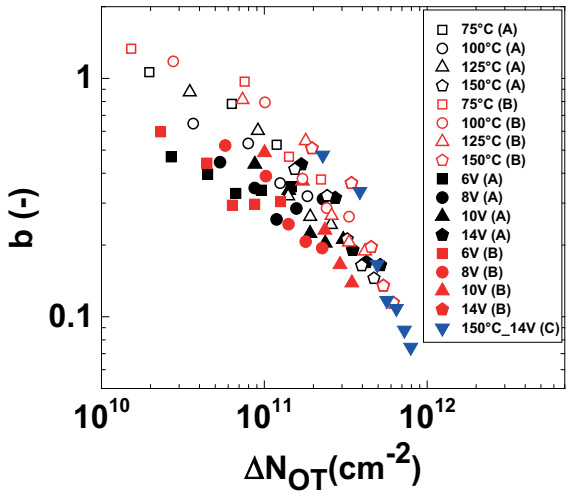

FIGURE 3.11: Trapping rate parameter $b = \frac{\partial_{log}(\Delta V_{th})}{\partial_{log} t}$ as a function of the density of trapped charges at different stress voltages and temperatures applied to different samples (A, B and C). A clear universal decreasing behavior is observed.

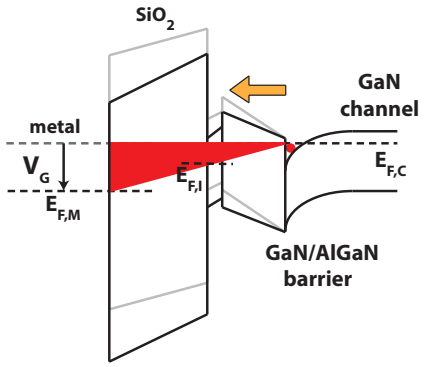

FIGURE 3.12: Band structure of a SiO_2/AlGaN-barrier/GaN-buffer stack. The AER (red area) is spanned by the applied forward gate bias and marks the energetic region, where defects can be filled due to forward gate bias [77].

stress voltage, stress temperature, and device-to-device variability. This trend suggests that the probability of charging traps is associated with the number of available empty traps that exist in the analyzed time window. As an additional cause, this decreasing tendency could be also explained by a charge feedback mechanism in which the electrons accumulated near or at the SiO_2/GaN interface during the stress increase the barrier potential and diminishes the effect of the forward bias [93].

This mechanism is based on the concept of the active energy region (AER) [94], which depends mainly on the field during stress. Lagger *et al.* illustrate the AER in a SiO_2/AlGaN-barrier/GaN-buffer stack as shown in Figure 3.12 [77]. Only defects in the active region are neutral prior to stress and can be potentially charged during stress. The size of the AER scales with $V_G > 0$ and consequently also the number of potentially accessible defects. More specifically, the AER is defined by the barrier-voltage drop V_B. During stress, electrons are captured at the interface states or at border traps and hence ϕ_B increases, which also lifts parts of the AER above $E_{F,C}$

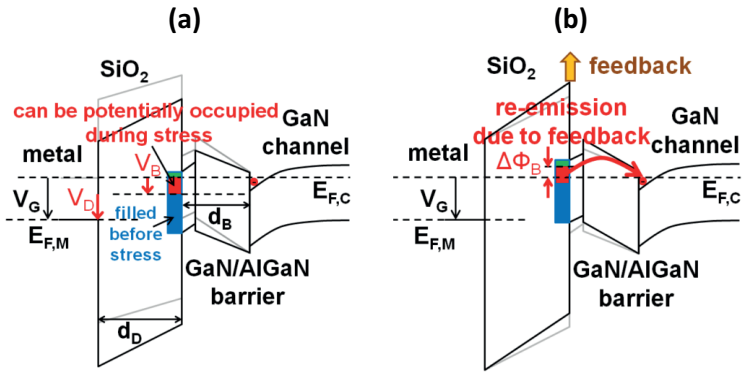

FIGURE 3.13: (a) The barrier potential is lowered from its thermal equilibrium value for $V_G > 0$, thus electrons are trapped at the interface or at border defect states in the region below the channel Fermi level $E_{F,C}$. (b) Charging of the interface increases ϕ_B and consequently, electrons can be re-emitted from the region lifted above $E_{F,C}$ [93].

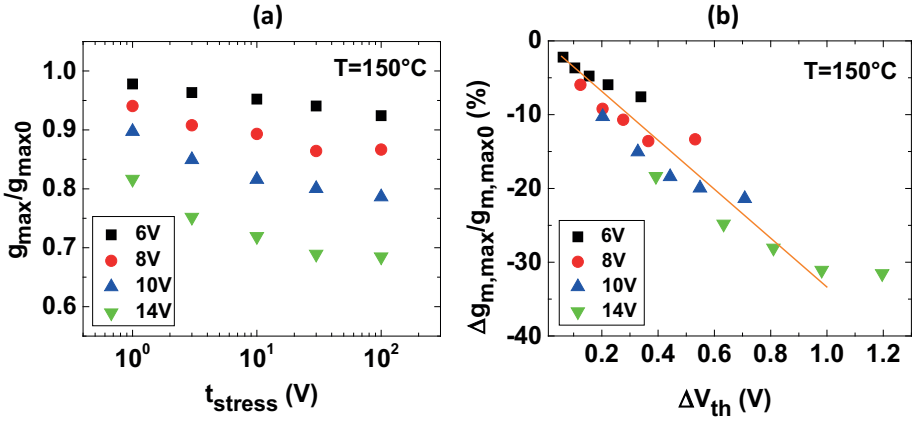

FIGURE 3.14: (a) Transconductance behavior during the stress phase by applying different bias conditions. (b) Transconductance variation vs. ΔV_{th} after different stress time and stress voltages at 150 °C. A linear correlation is observed (straight line).

and consequently electrons can be re-emitted as observed in Figure 3.13. The longer the stress, the more the barrier potential is increased and this could be related to the decreasing trend of the trapping parameter b in our stress measurements (Figure 3.10 (a)).

Additionally, the observation of a linear correlation by plotting the transconductance variation as a function of the threshold voltage shift for different stress voltages also corroborates that there is a contribution of the charge trapping at the SiO_2/GaN interface [95], [96]. This causes mobility degradation as depicted in Figure 3.14.

3.1.4 Recovery phase results and discussion

Figure 3.15 shows the relaxation data measured after different stress voltages, temperatures, and recovery voltages. For a sufficiently high recovery time, ΔV_{th} tends to zero, thus indicating that under the used stress conditions no permanent damage was introduced. In other words, the observed PBTI is fully recoverable. The

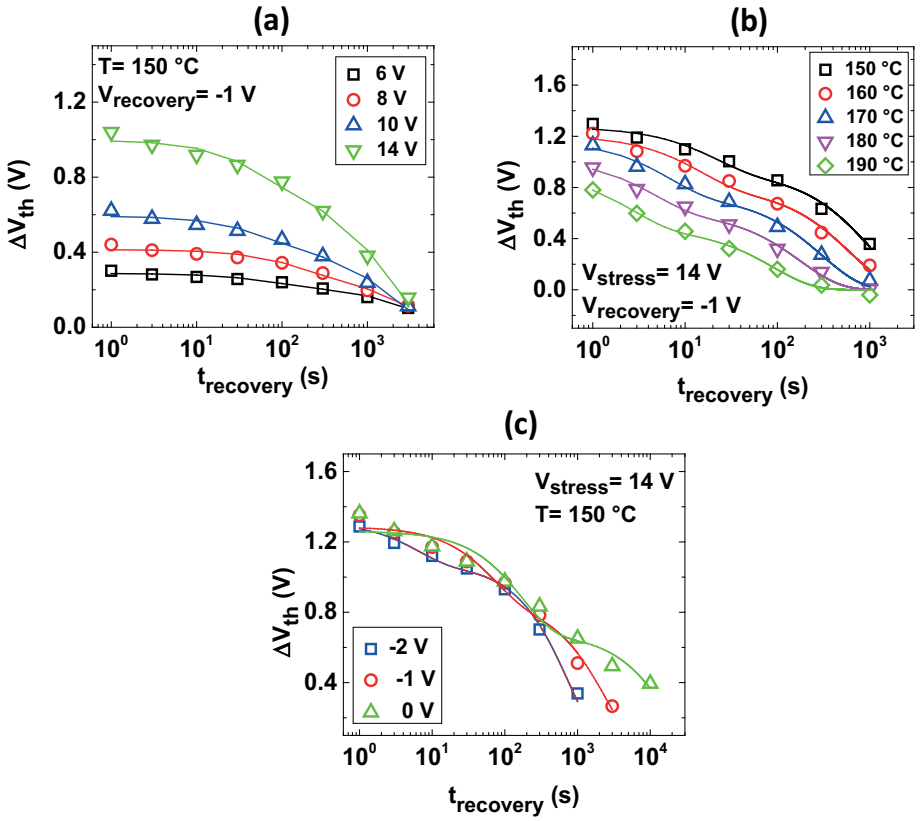

FIGURE 3.15: Experimental (markers) and fitting curves based on Eq. 3.3 (lines) of the ΔV_{th} evolution during the recovery phase for different (a) stress biases, (b) temperatures, and (c) recovery voltages. The fitting curves consist of the superimposition of two exponential functions.

observed ΔV_{th} evolution during the recovery phase is ascribed to the release of electrons from the energy states of the SiO_2 band-gap into the GaN layer (Figure 3.8 (b)). Several models have been proposed to describe the BTI relaxation dynamics [97–99]. As shown in Figure 3.15, it was considered a simple model based on the superimposition of two exponential functions given by the expression:

$$\Delta V_{th} = A_1 \times exp\left(\frac{t}{\tau_1}\right) + A_2 \times exp\left(\frac{t}{\tau_2}\right) \tag{3.3}$$

where A_1 and A_2 represent the amplitudes and t_1 and t_2 are the time constants. The good agreement between experimental data and fitting lines indicates that in the observed time window (between 1 s and thousands of seconds), the recovery dynamics under different conditions is well described by two effective sets of oxide traps located at different energy and/or position [100]. As an example, we can observe the final fitting and the individual contribution of trap 1 and 2 for the recovery data after V_{stress} = 14 V in Figure 3.16.

As can be seen from Figure 3.17 (a), both time constants depend weakly on the the stress voltage (between 6 V and 14 V). This result suggests that similar sets of traps have been filled independently of the applied stress voltage. On the contrary, Figure 3.17 (b) depicts that the two-time constants strongly decrease with temperature. Furthermore, both time constants decrease with more negative recovery (gate) voltages (Fig. Figure 3.17 (c)). As previous studies indicate [78], [101], a reverse

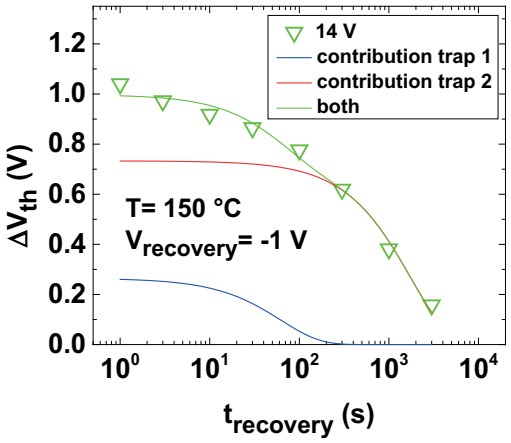

FIGURE 3.16: Final fitting and individual contribution of trap 1 and 2 for the recovery data after a stress phase at V_{stress} = 14 V.

electric field accelerates the de-trapping process of the charges by enhancing the electron tunneling back to the semiconductor layer. The main limitation of using a negative gate voltage for the recovery is to find the appropriate value to rapidly release charges from the traps without inducing additional stress.

In addition, the ratio between the two amplitudes exhibits an independent behavior of the stress voltage (Figure 3.17 (d)) and gradually increases with temperature (Figure 3.17 (e)) and recovery voltage (Figure 3.17 (f)). It is worth noting that an amplitude ratio less than one implies a dominant trap characterized by a time constant t_2.

Since a Gaussian distribution of the energy barrier is generally foreseen for the emission of single defects, a wide distribution of time constant is expected for a such behaving device. Therefore, the relaxation data were also fitted by using a higher number of time constants. By comparing these results with the ones obtained by using only two exponentials, it is observed that the data fitting is only slightly improved, but the trends of the time constants are quite noisy and unstable due to the limited set of experimental points. For this reason, we prefer to adopt the parsimonious model with only two effective time constants, but this is a simplified and purely empirical description of the underlying complex physical mechanism behind the BTI relaxation phase.

Furthermore, the fitting of the recovery data was also evaluated by adopting the universal relaxation law with the assumption of a negligible permanent component [102] (more details of this model will be discussed in subsection 3.2.6). The used relaxation function is described for the following stretched- exponential:

$$r(\xi) = exp\left(-B\,\xi^{\beta}\right) \tag{3.4}$$

where ξ is the relaxation time divided by the stress time, while B and β are the scaling and the dispersion parameter, respectively.

The results using this approach are illustrated in Figure 3.18. The trends of the β

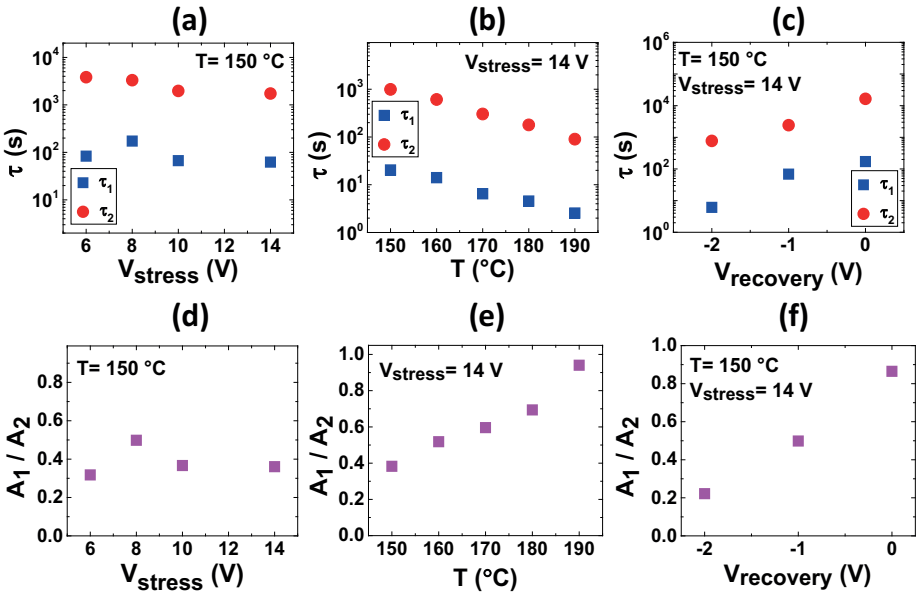

FIGURE 3.17: Both recovery time constants are independent of (a) stress voltage, (b) decrease with temperature, and (c) increase with recovery voltage. The ratio between the two amplitudes is also (d) stress voltage independent, and gradually rises (e) with temperature and (f) recovery voltage.

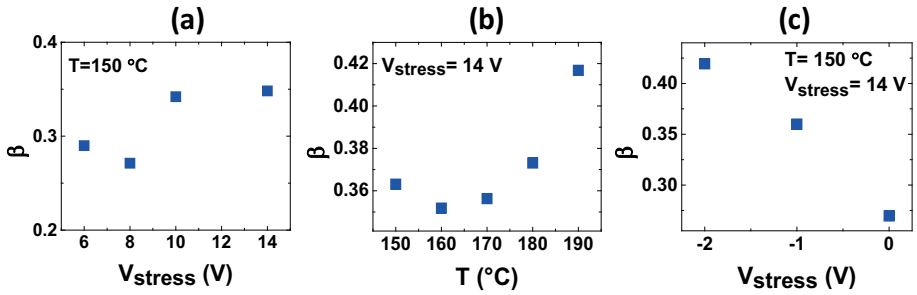

FIGURE 3.18: β parameter evolution as a function of (a) stress voltage, (b) stress temperature and (c) recovery voltage.

parameter as a function of the experimental parameters (stress voltage, stress temperature, and recovery voltage) completely agree with the results obtained by using the sum of two exponentials (clearly, since β measures the recovery speed, the observed agreement means that b shows the opposite behavior of the two-time constants). However, the two-time constants model is adopted since it shows a better match with the experimental data.

In order to determine the apparent activation energies for the two sets of traps, we used the Arrhenius plot reported in Figure 3.19. The two extracted activation energies, E_{a1} and E_{a2}, in diverse samples and by applying different recovery voltages can be found in Figure 3.20. It is worth noting that these values include the acceleration of trapping and de-trapping at the same time while the chuck is maintained at the same temperature during the whole measurement. On the one hand, the average activation energy of the slower trap (E_{a2}) is 0.93 eV and this value is almost independent of the recovery voltage and the investigated sample. On the other hand, the estimated value of the activation energy of the faster trap (E_{a1}) exhibits a significantly higher dispersion, falling in the range between 0.45 eV and 0.82

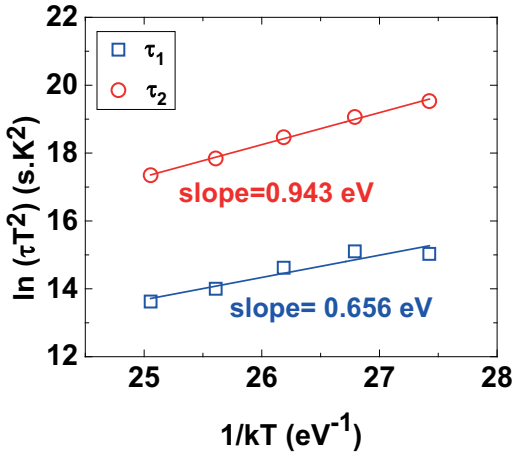

FIGURE 3.19: Arrhenius plot of the recovery time constants extracted from the exponential fitting during the recovery phase. The two activation energies are obtained by the slope of the fitting lines.

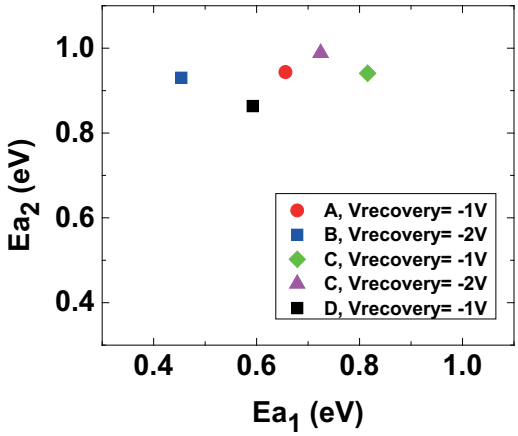

FIGURE 3.20: Apparent activation energy of the two traps (E_{a1} and E_{a2}) obtained in different samples (A, B, C, and D) at different recovery voltages. The activation energy of the faster trap (E_{a1}) exhibits a lower mean value and a higher dispersion.

eV. The larger energy spread is ascribed to the lower accuracy in the evaluation of the time constant of the faster trap, due to the lower amplitude. It is important to highlight that the extracted activation energies are related to the traps that are observable in the analyzed time window (1–100 s) and cannot be extended to fast traps in the regime of ms and ns.

3.1.5 Conclusions

The observed completely recoverable PBTI in AlGaN/GaN MOS-HEMT is ascribed to the initial trapping of electrons from the GaN layer into the traps located in the SiO_2 energy gap (stress phase) and the successive electron de-trapping (recovery phase). The PBTI trapping rate parameter exhibits a universal decreasing behavior during the stress phase as a function of the number of filled traps, independently of stress time, stress voltage, stress temperature, and device-to-device variability. In the observed time window (between 1 s and thousands of s), the recovery dynamics

is well described by the superimposition of two exponential functions. Both time constants decrease for more negative recovery voltages and for higher temperatures, while they are stress-voltage independent. Relaxation measurements at different temperatures indicate that the slower trap, which is dominant, exhibits an average activation energy of 0.93 eV, while the average activation energy of the faster trap shows a large spread in the interval between 0.45 eV and 0.82 eV.

3.2 Reliability impact of AlN layer sandwiched between the GaN and the Al_2O_3 layers in recessed AlGaN/GaN MOS-HEMTs

3.2.1 Introduction and state of the art

In GaN technology, insulators have demonstrated to be very important constituent materials because allow suppressing the current collapse effect (section 2.3) when they are used as surface passivation layers. Additionally, insulated-gate HEMTs or metal-insulator/oxide-semiconductor (MIS/MOS) HEMTs have also attracted significant interest due to the observed improvements in terms of gate leakage reduction and drain current increase. Many studies have been proposed with insulators such as SiO_2 [103], SiN_x [104], HfO_2 [105], Sc_2O_3 [106], ZrO_2 [107], among others, for both passivation and gate stacks fabrication, but this dielectric insertion also induce a reduction in the device transconductance and more severe threshold voltage instabilities. To face these inconveniences, dielectrics with a larger dielectric constant are preferred since they offer a more efficient gate modulation [108]. As a consequence, a smaller decrease in transconductance and a moderate increase in the threshold are observed.

Additionally, large band-offset energy is also required at the insulator/AlGaN interface for the suppression of the leakage current. From this point of view, the band gaps of materials such as Si_3N_4, ZrO_2, and HfO_2 are relatively small compared to AlGaN as depicted in Figure 3.21. On the other hand, in the case of the SiO_2, its dielectric constant (ε = 3.9) is not high enough as AlGaN compounds ($\varepsilon \sim 9.5$) causing some of the aforementioned problems. Figure 3.22 specifies the relative band energy position between the insulators and AlGaN/GaN (band lineups), which is essential to determine the 2DEG density N_s and to visualize the insulator/(AlGaN/GaN) system.

The use of materials with high dielectric constant (high-κ) dates back to studies in CMOS technology, whose main purpose is to extend Moore's law as Si-based devices continue to scale down. These dielectrics pose new concerns for the BTI understanding because of the presence of pre-existing traps mainly in the oxide bulk [111]. The possible locations of these traps are at the interface of the thin SiO_2 layer (normally used to conserve high channel mobility) and the high-κ dielectric, or in the bulk of the high-κ film. Moreover, the adoption of these dielectrics in other III-V devices, e.g. InGaAs MOSFETs, has demonstrated that electron trapping at the pre-existing oxide defects results in a fast and recoverable positive V_{th} shift under positive gate stress voltages [111]. Additionally, other studies indicate that stress-activated defects can also be locate in the near-interface region (border traps) of the Al_2O_3 in InGaAs n-MOSFETs [112]. Therefore, identification and deposition of suitable dielectrics that play a similar role to that observed in Si-based devices are still

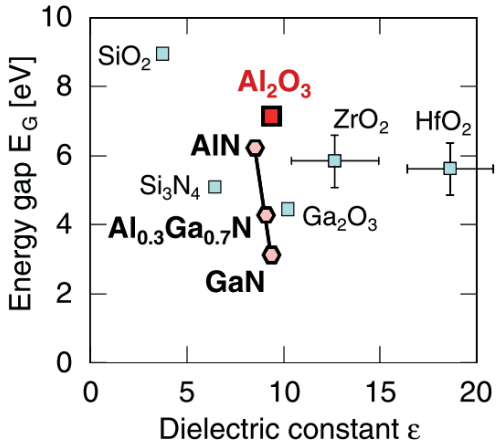

FIGURE 3.21: Energy gap E_g versus dielectric constant ϵ for various insulators and AlGaN compounds [109].

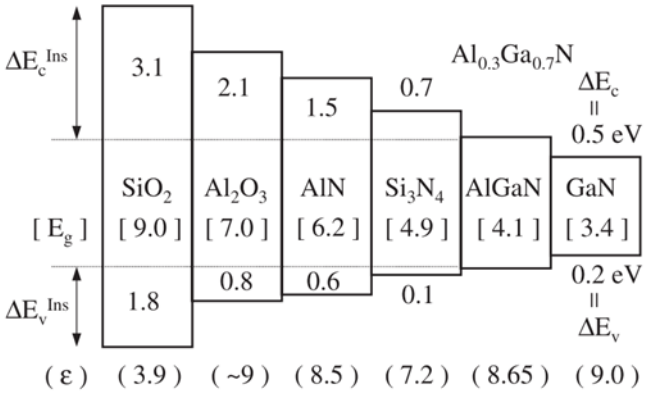

FIGURE 3.22: Band lineups for SiO_2, Al_2O_3, AlN, Si_3N_4, $Al_{0.3}Ga_{0.7}N$, and GaN [110].

challenging since the III-V/oxide interfaces normally exhibit a much lower quality than their Si counterpart.

Recently, in GaN-based technology, the superior quality of atomic layer deposition (ALD) due to high uniformity over sputtering and electron-beam deposition in conjunction with the larger band-gap (E_g=6-8 eV), high dielectric constant (ε=8-10), high breakdown field strength ($\geq$10MV/cm), high thermal (amorphous up to at least 1000 °C), and chemical stability of ALD-grown Al_2O_3 makes it an attractive option as a gate insulator [113].

However, a significant amount of defective bonds, such as Al-Al and Al-O-H, has been normally reported in ALD-Al_2O_3 films, especially when H_2O is used as oxygen precursor, resulting in high-density positive fixed charges and acceptor-like border/interface traps [114]. The existence of these positive charges hinders the formation of the normally-off channel, while the charging/discharging process of border/interface traps also induce V_{th} instability, compromising the safety of power switching devices. Additionally, Ooyama *et al.* reported in [115] that the defect level densities of Al_2O_3 on AlGaN were about 10 times higher than those of GaN, probably due to high densities of defects associated to nitrogen vacancy, oxygen impurity,

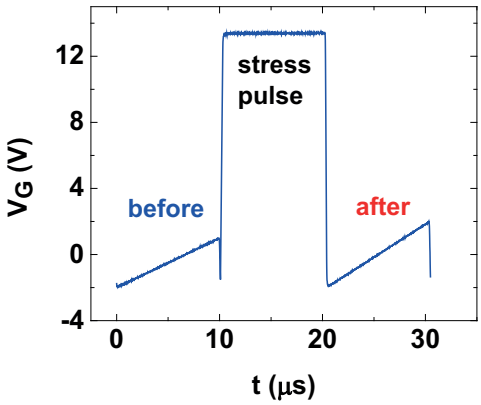

FIGURE 3.23: Voltage signal applied to the gate contact during the stress test

and their complexes. In order to reduce the interface states, Hori *et al.* [116] proposed an N_2O-radical treatment to the AlGaN surface just prior to the Al_2O_3 insulator deposition, which results in a decrease of the interface states and improvements in the electrical properties of the Al_2O_3/AlGaN/GaN. To have a better interface quality, another approach is to employ a bilayer insulator technique. By considering that Si_3N_4 demonstrates a high-quality insulator/nitride interface [110], it is normally used as a thin intermediate layer before the deposition of high resistive and high dielectric constant materials such as Al_2O_3. This also allows obtaining a significant increase in the 2DEG density (N_s) and a decrease in the sheet resistance [110].

Some studies also show that nitride-based insulators are compelling candidates as interfacial passivation layers (IPL) for normally-OFF MIS-HEMT power devices. In particular, AlN is used because it has high electrical resistivity (10^{14} Ω/cm), larger bandgap (6.05 eV), higher breakdown electric field (10^7 V/cm), high dielectric constant (k=9), and smaller lattice mismatch with GaN compared to SiN_x [117], [118]. Moreover, it is expected to reduce the formation of Ga-O bonds in the Al_2O_3/GaN interface and to enhance the current densities because, in this polar material, there is the presence of polarization fields [119]. Because the performance of GaN-based devices depends critically on the dielectric/GaN interface and following our previous study in SiO_2 [103], we analyze the general performance and the behavior during the stress/relaxation phase under different conditions in AlGaN/GaN MOS-HEMTs with two different gate dielectrics: a single layer of Al_2O_3 and a bilayer consisting of AlN and Al_2O_3.

3.2.2 Experimental setup for the stress phase

All the measurements were carried out by means of a parameter analyzer Keithley 4200-SCS equipped with the 4225-PMU ultra-fast I-V module and two 4225-RPM remote amplifier/switch modules. Before each stress, an initial stabilization at $V_G = -1V$ for 3000 s is performed. As a result, the virgin device releases charges originally contained in trapping centers [84], [85] and reaches a reproducible reference state for all the successive tests. It is worth noting that the stress and recovery behavior were analyzed separately by using a fast pulse measurement technique in order to avoid trapping of charges during the characterization. As shown in Figure 3.23, a complete pulsed I_D-V_{GS} measurement is performed before and after applying the pulse in order to extract the stress-induced threshold voltage shift ΔV_{th}

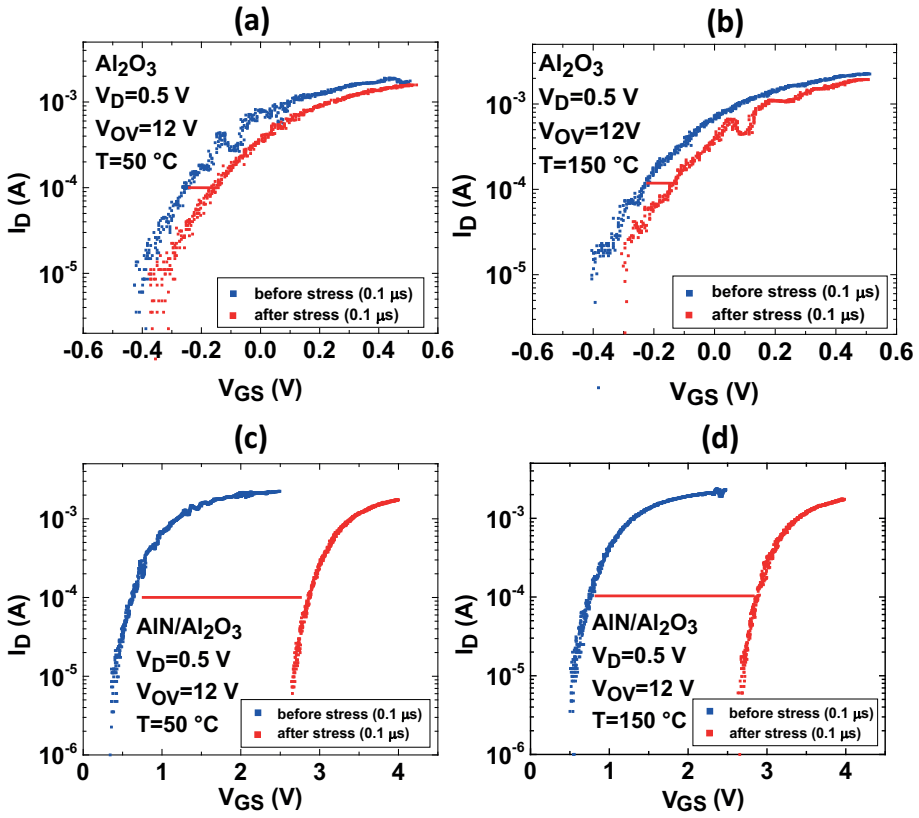

FIGURE 3.24: I_D-V_{GS} curves before and after applying a pulse width of 0.1 μs in (a), (b) the single layer stack (Al_2O_3) and in (c), (d) the bilayer stack (AlN/Al_2O_3) at 50 °C and 150 °C, respectively. The ΔV_{th} is slightly influenced by the temperature during the stress phase.

during the stress phase. It is important to highlight that all the stress-sense-stress sequence was carried out without interruption . Moreover, since the temperature almost does not affect the measured ΔV_{th} during the pulsed test as depicted in Figure 3.24 and in order to reduce the long recovery time, all the experiments were performed at 150 °C. By applying a drain voltage at 50 mV and using a current criterion of 10 μA for V_{th} estimation, the results exhibit dispersed values around the reference current that inhibit to precisely calculate the ΔV_{th} (Figure 3.25 (a)). However, a more accurate extraction with almost the same results can be obtained with a drain voltage at 500 mV and a current criterion of 100 μA as depicted in Figure 3.25 (b).

Once the device recovers from the stress by applying a negative voltage between -1 V and -3 V, the cycle is repeated by gradually increasing the width of the pulse from 100 ns to 300 μs and for different stress gate voltage overdrives ($V_{OV} = V_{GS} - V_{th}$) from 12 V to 16 V in both samples. Figure 3.26 gives an example of the observed positive ΔV_{th} ascribed to charge trapping for 1, 30, and 100 μs for the single layer device.

3.2.3 Experimental setup for the recovery phase

In the recovery test, the first two steps described in the stress phase are again performed, i.e. a complete pulsed I_D-V_{GS} curve followed by a stress pulse, but the gate

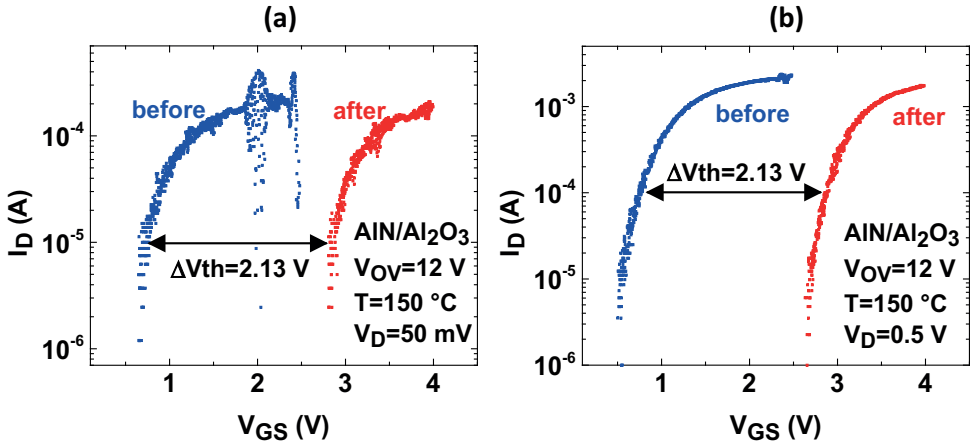

FIGURE 3.25: I_D-V_{GS} curves before and after applying a pulse width of 0.1 μs in the AlN/Al_2O_3 sample by using (a) a current criterion at 10 μA and V_D=50 mV and (b) a current criterion at 100 μA and V_D=500 mV. Similar behavior is observed in the Al_2O_3 sample.

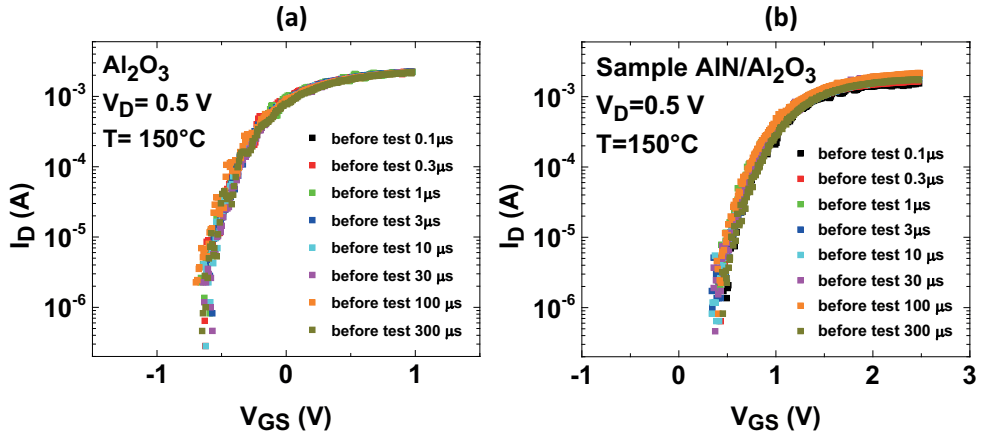

FIGURE 3.26: I_D-V_{GS} curves before and after applying a pulse width of 1, 30 and 100 μs (Al_2O_3). The ΔV_{th} was evaluated by using the current criterion at 100 μA.

voltage is maintained at a fixed value (V_{sense}) at the end of the stress pulse instead of performing an entire I_D-V_{GS} sweep (see Figure 3.27 (a)). From the stress phase, we knew the V_{th} after each stress pulse ($V_{th,after}$). Therefore, V_{sense} is selected around this value to perform the recovery experiments. Figure 3.27 (b) depicts an example of the transient drain current during the recovery test for two different pulse widths in the single layer device. The ΔV_{th} recovery evolution has been extracted from the drain current transient by horizontally shifting the unstressed I_D-V_{GS} characteristics measured at the beginning of the sequence [86]. It is important to clarify that at $V_{sense} \sim V_{th,after}$ the variations in the measured current are assumed to be only related to ΔV_{th}. Additionally, we consider only recorded currents greater than 10 μA since smaller values are extremely noisy in the unstressed I_D-V_{GS} curve to get a reliable measurement.

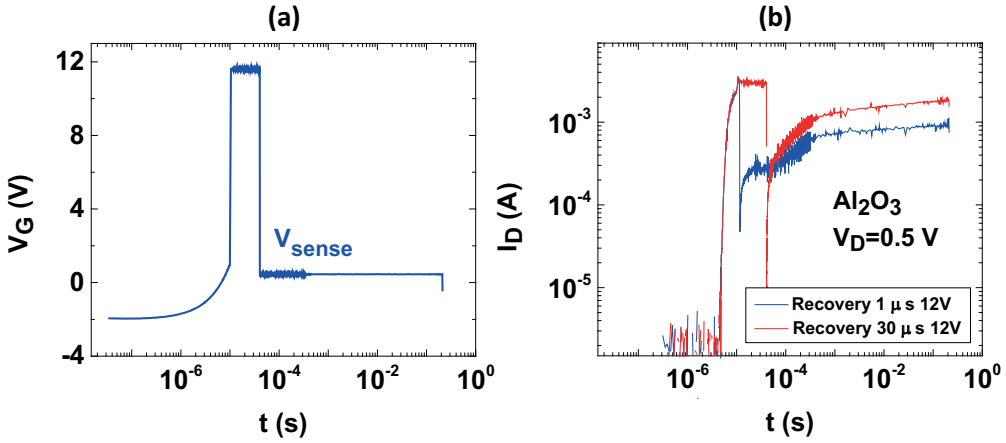

FIGURE 3.27: (a) Voltage signal applied to the gate contact during the recovery test and (b) the respective drain current measurements for the two different pulse widths (1–30 μs) at 12 V in the single layer sample.

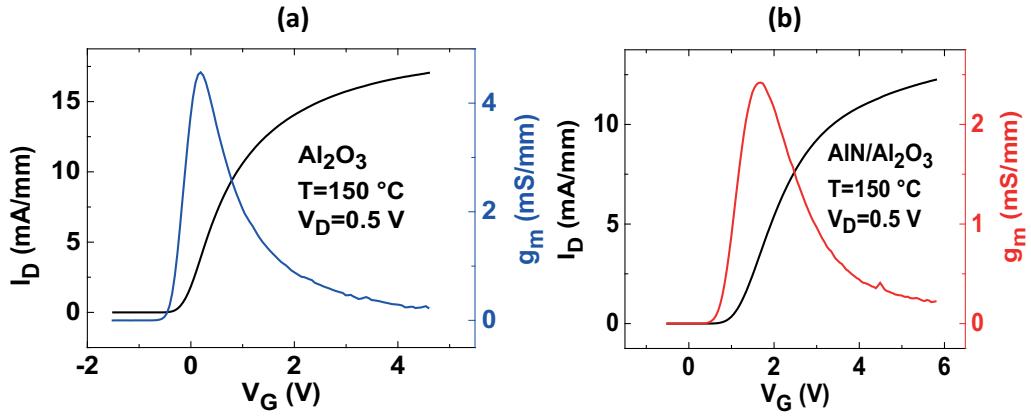

FIGURE 3.28: Transfer characteristics in (a) AlN/Al_2O_3 MOS-HEMT and (b) Al_2O_3 MOS-HEMT.

3.2.4 General characteristics comparison

The I_D-V_{GS} characteristics of the devices are illustrated in Figure 3.28. As shown, the V_{th} of the device with a single dielectric is -0.27 V and with the double layer dielectric is 0.95 V. From this result, a clearly normally-OFF operation is observed only in the bilayer sample. This is ascribed to the positive polarization charge induced by the AlN layer at the Al_2O_3/AlN interface [120] which can deplete the 2DEG channel. Added to that, the maximum transconductance $g_{m,max}$ is reduced from 4.6 mS/mm to 2.4 mS/mm when the AlN layer is introduced. This fact suggests a poor quality in the interface and a worse gate modulation than the single stack. At the same V_{OV}=4 V, the drain current of the single layer device exhibits a greater value ($\sim$ 6.7 mA) than the bilayer device ($\sim$ 4.4 mA). Comparing the ON-resistance at V_{OV} =8 V in Figure 3.29, the AlN/Al_2O_3 has a greater value of 42.9 Ω.mm while the Al_2O_3 device exhibits a resistance of 28.5 Ω.mm. On top of that, Figure 3.30 (a) shows a greater degradation in the AlN/Al_2O_3 device based on the clockwise hysteresis that is frequently attributed to acceptor-like traps states at the dielectric/III nitride interface [114] or in the bulk region [121]. From Figure 3.30 (b) it can be seen that in a log-linear scale, ΔV_{th} is almost the same in the window from units to hundredths

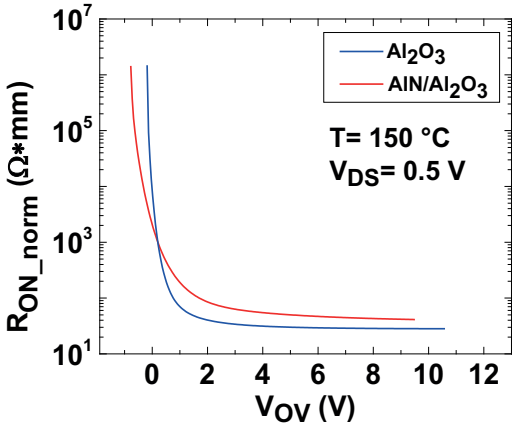

FIGURE 3.29: Normalized R_{ON} resistance as a function of the overdrive voltage V_{OV}. The Al_2O_3 MOS- HEMT exhibits a lower resistance than the AlN/Al_2O_3 device.

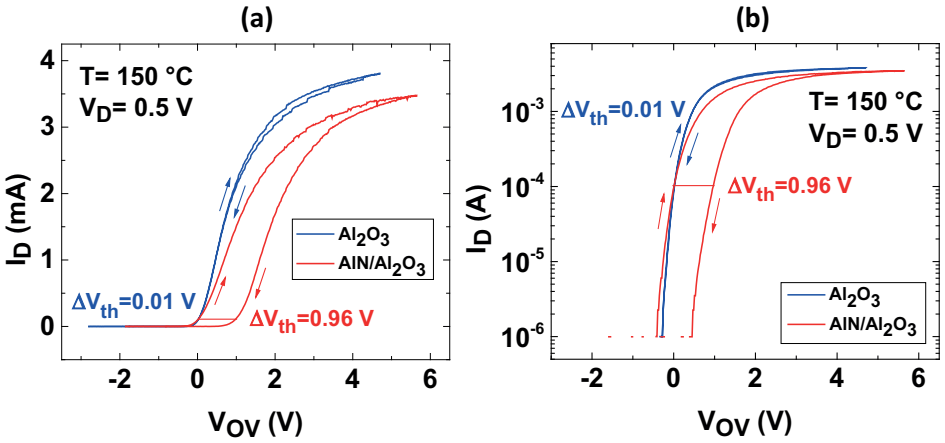

FIGURE 3.30: I_D-V_{OV} curve in (a) a linear-linear and (b) a log-linear scale obtained by applying a train of pulses with a period of 300 μs and width of 30 μs at the gate and drain terminals. The hysteresis observed was quantified by evaluating the shift at 0.1 mA.

of μA which favors our measurement methodology during the recovery phase.

3.2.5 Stress phase results and discussion

The ΔV_{th} due to the single stress pulse for three different overdrive voltages is reported in Figure 3.31. In both devices, the shift follows the saturating log-time dependence model [122] given by the expression:

$$\Delta V_{th} = \Delta V_{max} \times [1 - exp\,(-(t/\tau_0)^{\gamma})] \tag{3.5}$$

where ΔV_{max} is related to the total trap density and the centroid of the trap-charge distribution in space, γ is a measure of the width of the trap energy distribution and τ_0 is the time constant of the traps. For all the stress conditions, it has been found that the AlN/Al_2O_3 sample exhibits higher ΔV_{max} which indicates a larger trap density than in the single dielectric stack. Besides, the time constants of the bilayer device

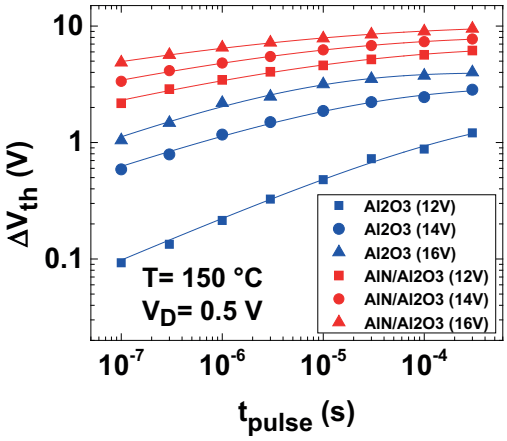

FIGURE 3.31: Experimental (markers) and fitting curves (lines) of the ΔV_{th} evolution as a function of the width of the BTI stress pulse. These measurements were performed by following the procedure for the stress experiment described in subsection 3.2.2

TABLE 3.1: Fitting parameters of the ΔV_{th} degradation during the stress phase.

Device	$V_{OV} = 12$ V			$V_{OV} = 14$ V			$V_{OV} = 16$ V		
	ΔV_{max}	τ_0	γ	ΔV_{max}	τ_0	γ	ΔV_{max}	τ_0	γ
Al_2O_3	1.74 V	2.03e-4 s	0.37	2.96 V	1.07e-5 s	0.31	3.97 V	2.70e-6 s	0.34
AlN/Al_2O_3	6.58 V	4.14e-6 s	0.23	8.13 V	1.72e-6 s	0.21	9.99 V	8.20e-7 s	0.18

are significantly lower when we compared with the single layer device, thus indicating a faster charge trapping process. Moreover, the bilayer device exhibits a wider trap energy distribution since the γ values are smaller than the Al_2O_3 device. All the model parameters for the different stress conditions for both devices are listed in Table 3.1.

This model described by Zafar *et al.* [122] for high-κ dielectrics predicts that ΔV_{th} would increase with a power law dependence on time and injected charge carrier density during the initial part of the stress test ($t \ll \tau_0$). On the other hand, the model also indicates that ΔV_{th} would become constant after prolonged stress time ($t \gg \tau_0$) provided that no new traps are created. By considering that the subthreshold slope remains constant with stressing independently of the stress voltage and since this parameter is a measure of the interfacial trap density, it is concluded that no new interfacial traps are created during the stress phase. Therefore, the observed shift in threshold voltage is ascribed to the trapping of electrons from the channel into the existing traps located in the gate dielectrics. However, this model is not applicable to stress conditions that result in significant creation of new traps as in the case of hot electron stressing.

3.2.6 Recovery phase results and discussion

Even though the described pulse measurement technique has a sample time in the order of tens of nanoseconds, the partial recovery once the stress is removed to perform the characterizing I_D-V_{GS} curve cannot be neglected since it results in an underestimation of the PBTI degradation. The universal relaxation model is based on the observation of certain common features through different studies [101], [102] and appears in response to the difficulty to minimize the measurement delay even at ultra-fast measurement techniques. Firstly, the relaxation data $R(t_{stress}, t_{relax})$ captured at different t_{stress} need to be normalized to the first available point, which is recorded after a measurement delay t_M. This is called *fractional recovery* and is given by the following expression:

$$r_f(t_{stress}, t_{relax}) = \frac{R(t_{stress}, t_{relax})}{R(t_{stress}, t_M)}. \tag{3.6}$$

The real accumulated damage during the stress phase $S(t_{stress})$ is the sum of the recoverable component $R(t_{stress}, t_{relax} = 0)$ at a relaxation time t_{relax}=0 and a permanent component $P(t_{stress})$ taking in account that in some cases not all damage can be recovered. The universal relaxation function is then described by

$$r(\xi) = \frac{R(t_{stress}, t_{relax})}{S(t_{stress}) - P(t_{stress})} = \frac{R(t_{stress}, t_{relax})}{R(t_{stress}, t_{relax} = 0)}. \tag{3.7}$$

where ξ is t_{relax}/t_{stress}.

Since the term $R(t_{stress}, t_{relax} = 0)$ is unknown and one only has the $R(t_{stress}, t_M)$ data captured after a short relaxation period t_M, it is necessary to employ the following relation between the universal recovery function and the fractional recovery

$$r_f(t_{stress}, t_{relax}) = \frac{r(\xi)}{r(\xi_M)} \tag{3.8}$$

where $\xi_M = t_M/t_{stress}$. Therefore, by replacing Eq. 3.6 in Eq. 3.8, the final expression to adjust the relaxation data is obtained

$$\frac{r(\xi)}{r(\xi_M)} = \frac{R(t_{stress}, t_{relax})}{R(t_{stress}, t_M)}. \tag{3.9}$$

Several empirical expressions have already been proposed to fit the measured relaxation data [102], but in this work, the generalized form given by

$$r(\xi) = \frac{1}{(1 + B\,\xi^{\beta})} \tag{3.10}$$

is used because it covers a larger range of measurement data and exhibits an asymptotic limit for large and/or small ξ. By introducing the above function into Eq. 3.9, the scaling B and the dispersion parameter β can be easily obtained. Once the relaxation data is fitted, it is possible to get a rough estimation of $R(t_{stress}, t_{relax} = 0)$ as illustrated in Figure 3.32.

The BTI relaxation property of scaling with the universal relaxation time, ξ, allows fitting the complete ΔV_{th} recovery with a single set of parameters B and β by using the expression:

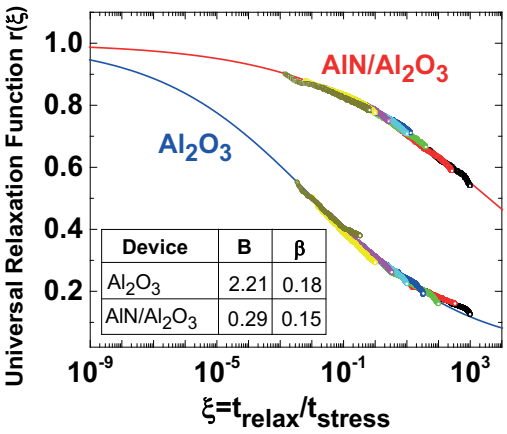

FIGURE 3.32: Experimental (markers) and fitting curves (lines) of the measured transients fitted with the universal relaxation function (Eq. 3.10).

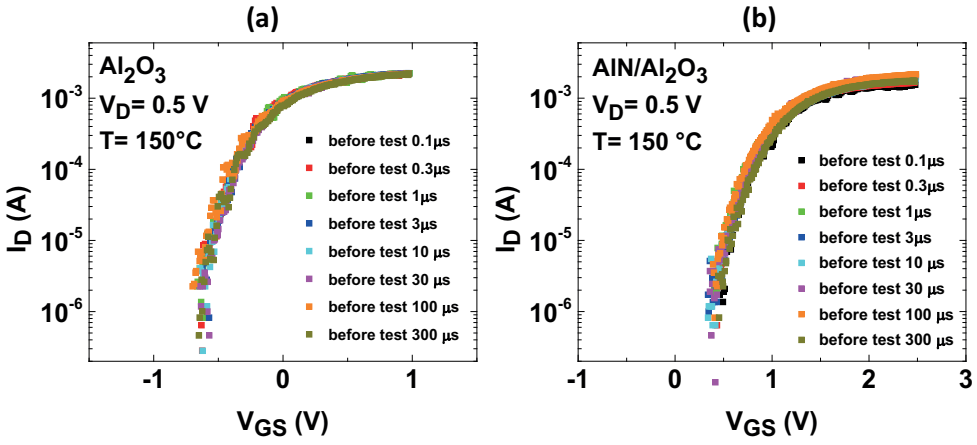

FIGURE 3.33: Initial I_D-V_{GS} curves (recovery sequence) before the application of each stress pulse at V_{OV}=12 V in (a) the single and (b) double layer. The overlapping of all the initial curves confirms that no permanent degradation was observed during the experiments.

$$\Delta V_{th}(t_{stress}, t_{relax}) = R(t_{stress}, t_{relax} = 0) \times r(\xi) + P(t_{stress}). \tag{3.11}$$

As depicted in Figure 3.33, the I_D-V_{GS} curve always comes back to the original reference state after the stress phase under different stress conditions. Therefore, a permanent degradation is discarded ($P(t_{stress})$=0) in Eq. 3.11 for the analyzed stress gate overdrive voltage. Nevertheless, it could be not extended if higher stress voltages or longer stress time are used.

Figure 3.34 illustrates the ΔV_{th} evolution during the recovery tests for different stress overdrive voltages and pulse widths. It can be observed that all transients are well described by the universal relaxation model and can be explained by the electron de-trapping from the defect sites located in the gate dielectrics.

It is worth noting that the use of this empirical model provides just qualitative information, but it perfectly fits in the approach of this comparative PBTI behavior

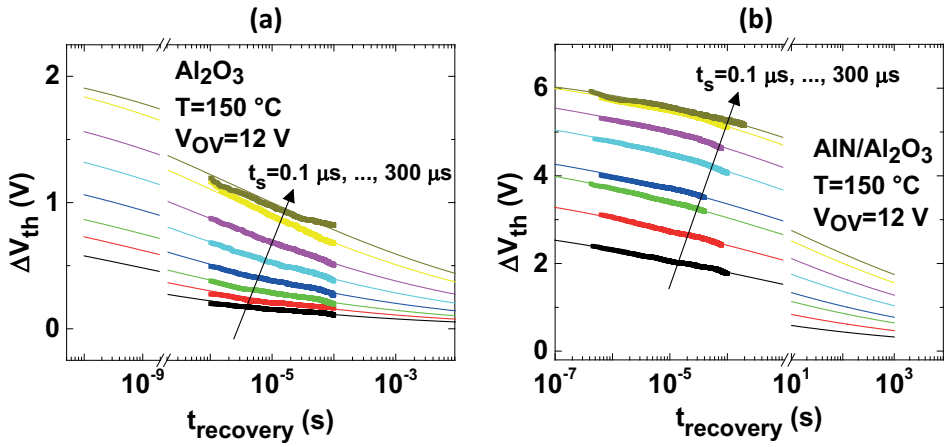

FIGURE 3.34: Experimental (markers) and fitting curves (lines) of the ΔV_{th} recovery evolution after applying a single stress pulse. The experiments were performed at 12 V and pulse widths from 0.1 to 300 μs.

of the two dielectrics. By comparison, the fitting parameters of the single layer device (B = 2.21 and β = 0.18) exhibit greater values than the bilayer device (B = 0.29 and β = 0.15) which results in a more rapid release of trapped charges during the recovery phase.

The low γ in the bilayer stack (stress phase) in conjunction with the slower charge emission (recovery phase) could be related to a wide distribution of defect levels close to the Fermi level in the GaN channel as suggested in preceding works [123]. This mechanism is consistent with the easy charge capture in the gate dielectric defects even at low-stress voltages and short-stress times. On the other hand, the high γ and the faster charge emission in the Al_2O_3 sample suggest a narrow distribution of defects levels located away from the channel Fermi level. In contrast with previous studies with AlN layer [120], [124], our work shows that the PBTI reliability and the general characteristics are poor compared with the single layer stack.

3.2.7 Conclusions

This experimental study shows that the insertion of an AlN layer sandwiched between the GaN and the Al_2O_3 layers allows obtaining the normally-OFF operation, but this benefit is paid in terms of performance and reliability. AlN/Al_2O_3 samples exhibit higher ON-resistance and significantly faster charge trapping compared with Al_2O_3 devices, as highlighted by the larger hysteresis in the I_D-V_{GS} curve and the BTI evolution. The observed PBTI is ascribed to electron trapping and de-trapping in defect sites located in the gate dielectrics. The more pronounced charging phenomena in the bilayer devices could be ascribed to the low value of γ observed in the saturating log-time model which results in a wider distribution of defect levels compared with Al_2O_3 device. From the relaxation measurements, we found that the recovery evolution for both devices is well fitted by the empirical universal relaxation law. In addition, the slower charge emission observed during the recovery phase in the sandwiched AlN device could suggest that the distribution defect levels is centered close to the channel Fermi level which favors the charge capture in the dielectric even at low-stress voltages and short stress times.

3.3 Summary of the chapter

In this chapter, the MOS/MIS structure has been analyzed since the provided improvements in gate leakage reduction and drain current increase by the introduction of a dielectric could come at the cost of device long-term reliability. To study the degradation in this layer and at its interfaces with AlGaN or GaN, different dielectrics and characterization techniques have been employed. In special, a more comprehensive analysis of the reliability issue known as PBTI, which is related to the degradation of electrical parameters when high positive gate voltages and temperatures are applied, has been studied by using different stress/recovery conditions.

The presented results show that MOS-HEMTs with a SiO_2 as a gate dielectric exhibit a slow trapping-process during the stress phase, which does not follow the conventional power law model and is related to charge trapping not only in the SiO_2 but also at the SiO_2/GaN interface since mobility degradation has been observed. The trapping rate parameter in these devices exhibits a universal decreasing behavior as a function of the number of trapped charges per unit area and could be related to a charge feedback mechanism or/and a direct relation between the probability of charging traps with the number of available empty traps. The recovery dynamics is thermally accelerated and is associated with two sets of oxide traps located at different energy levels or/and positions.

On the other hand, devices with Al_2O_3- and AlN/Al_2O_3-gate stacks show a more rapid charge trapping, which requires a pulsed measurement characterization. The degradation in this relatively high-κ materials is mainly attributed to charge capture in the pre-existing dielectric traps with a negligible interface state generation. The relaxation data are well described by using the empirical universal relaxation model, whose fitting parameters indicates a faster de-trapping process during the recovery phase in gate stacks with Al_2O_3. Finally, it has been observed that the insertion of a thin AlN layer impacts on the device reliability due to a larger trap density, faster charge trapping, wider trap energy distribution and slower charge release compared with devices without this layer.

Chapter 4

Reliability study of GaN-based SBDs

4.1 Methodology for time-dependent dielectric breakdown analysis

4.1.1 General background in dielectric breakdown

Dielectric breakdown occurs when the potential across the dielectric is high enough to accelerate the injected electrons leading to an abrupt or progressive formation of a conductive path, which results in the loss of insulating properties as shown in Figure 4.1. This is a stochastic process. Therefore, statistics are indispensable for data analysis and model fitting. Typically to tackle the issue of the inevitable wafer location variability, reliability test structures are grouped very close together in a minimal wafer area in order to minimize the impact of local variability; eventually the test is repeated also on other groups of structures at different locations, to assess the variability across wafer. Once the test data are obtained, a probability distribution functions (PDF) with the best fit is used to interpret the results. Since the dielectric breakdown analysis is one of the required reliability evaluations in different technologies, e.g. Si-based, III-V, SiGe, etc., and by using different dielectrics, more details about the time-dependent dielectric breakdown mechanism (TDDB) including the related model, the test methodologies, the statistical data analysis, and the lifetime calculation are presented in the subsequent subsections.

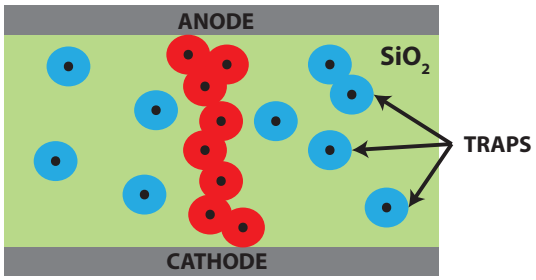

FIGURE 4.1: Schematic illustration of intrinsic oxide breakdown (SiO_2) based on trap generation and conduction via traps (conductive path) [125].

4.1.2 Time-dependent mechanism

The time-dependent dielectric breakdown mechanism is based on the random generation of traps within the oxide until a conduction path is formed causing a sudden

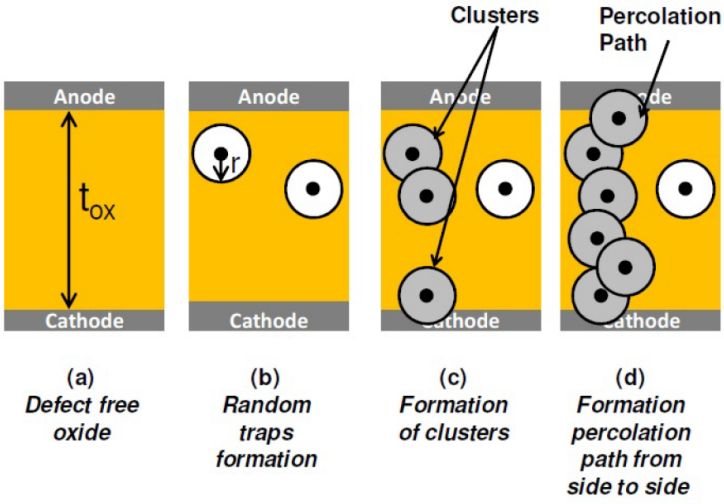

FIGURE 4.2: Description and modeling of the oxide breakdown phases during a CVS [126].

increase in the current normally indicated as time-to-breakdown (t_{BD}). This mechanism is known as percolation model [127] and its different stages are well illustrated in Figure 4.2. Initially, the defect density within the dielectric is relatively low (or negligible), therefore, the conduction mechanism is based on Fowler–Nordheim (FN) tunneling or direct tunneling of electrons. During the stress test, electron traps are created inside the oxide/dielectric at random positions in space. The model defines a sphere of radius r around the generated traps. When the spheres of two neighboring traps overlap, trap-related conduction takes place between them. As previously mentioned, this trap generation mechanism continues until a conductive path is formed between the electrodes or interfaces (see Figure 4.2 (d)).

An important characteristic of this model is that it quantitatively describe the experimental results wherein the oxide-trap density needed to cause the breakdown, N_{min}, decreases with the oxide thickness (t_{ox}) due to the formation of the conductive path with just a few traps. Additionally, the percolation model also predicts that the statistical distribution of t_{BD} becomes more spread when the t_{ox} is reduced. This has been experimentally confirmed [127], which further supports the validity of this model.

Several models have been proposed to explain the generation of traps on SiO_2 or on high-κ itself. Degraeve *et al.* summarize three of the most mentioned ones in the Literature [127]. The first one is the "anode hole injection model", which describes that holes are created by electron energy released at the anode, then these holes tunnel back to the cathode creating electron traps in the oxide as observed in Figure 4.3 (a). In the second model, it is suggested that the energy release from incoming electrons at the anode can, besides hole creation, also activate hydrogen release leading to the neutral electron trap generation (see Figure 4.3 (b)). This mechanism, which is better known as the "hydrogen release model", explains that the electron tunneling through the oxide potential barrier can reach the anode with enough energy to release hydrogen from the anode/oxide interface. Subsequently, this hydrogen diffuses within the oxide generating electron traps. The last one is the "electric field energy model". In this case, it is suggested that the electric field induces sufficient

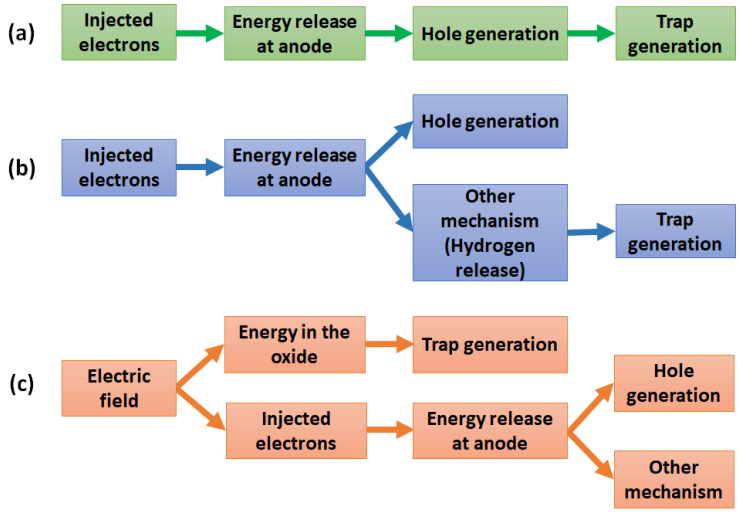

FIGURE 4.3: Schematic flow-chart describing the three lines of thought on neutral electron generation describe in the Literature [127].

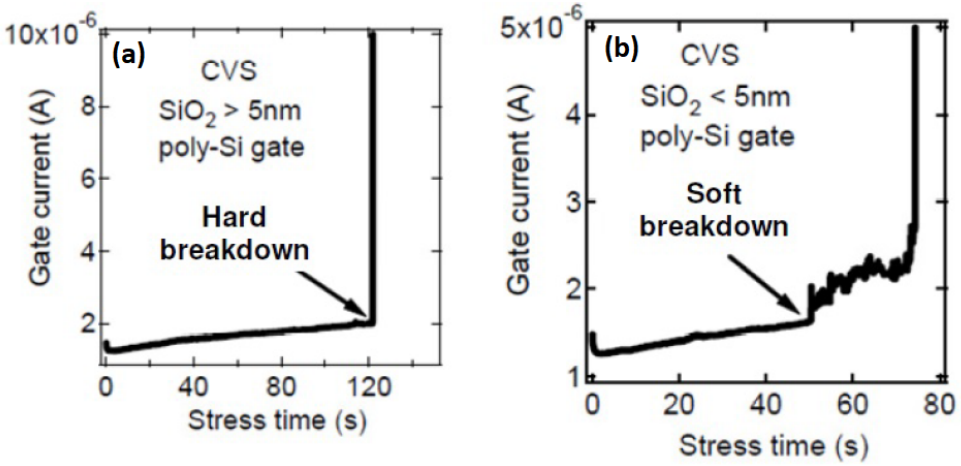

FIGURE 4.4: Monitored current through an oxide during CVS experiment in the case of oxide thickness (a) larger and (b) smaller than 5 nm [128].

energy directly into the oxide to provoke electron trap generation as illustrated in Fig. Figure 4.3 (c).

4.1.3 Stress experiments for TDDB data extraction

There are two common test methodologies to perform TDDB analysis. In the first one, a constant voltage is applied to the transistor or capacitor while the current is monitored (constant voltage stress-CVS). This method is normally used in thin oxides where N_{min} and t_{BD} depends on gate voltage and oxide thickness. On the contrary, in the second method, a constant current is applied during the stress while monitoring the voltage (constant current stress-CCS). Since N_{min} and t_{BD} depends only on current density (independent of thickness), this test is more suitable for thick oxides.

It is worth noting that the breakdown signature varies with the dielectric thickness as depicted in Figure 4.4. For thick oxides ($t_{ox} > 5$ nm), the gradual oxide

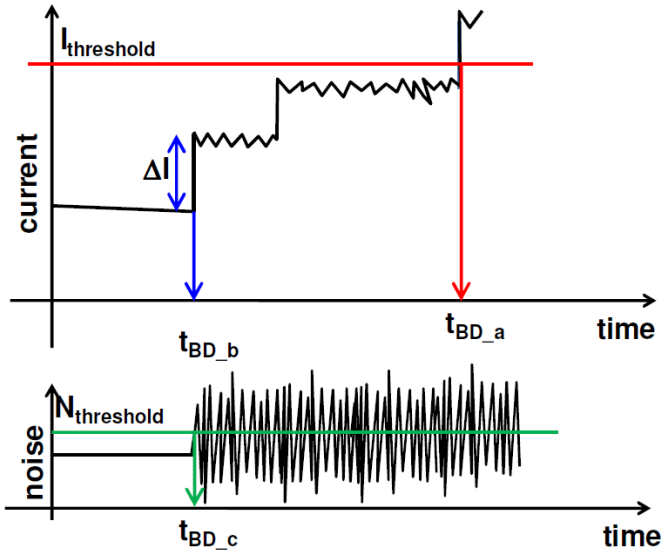

FIGURE 4.5: Schematic representation of the *I-t* traces and its noise during a CVS. Different time-to-breakdowns (t_{BD}) can be extracted based on different criteria. t_{BD_a} is extracted when the current exceeds a threshold ($I_{threshold}$), t_{BD_b} is extracted when a current jump is larger than a defined value (ΔI) and t_{BD_c} is extracted when the noise of the current goes beyond a threshold ($N_{threshold}$) [126].

degradation provokes the immediate destruction of the dielectric (hard breakdown) because of thermal damage. In contrast, the degradation of thin oxides ($t_{ox} < 5$ nm) is first observed through an increase in the leakage-current noise (soft breakdown) followed by the dielectric destruction [35].

The t_{BD} is extracted from the current-time (*I-t*) trace in the case of CVS experiments. This parameter can be defined by using three different criteria as illustrated in Figure 4.5 [126]. In the first one, t_{BD} is defined when the monitored current exceeds a threshold value ($I_{threshold}$), i.e. (t_{BD_a}) in Figure 4.5. This is the most straightforward method, but it allows detecting the hard breakdown phenomenon while the time at which single or multiple breakdown paths are formed cannot be properly captured. The second option is to extract the t_{BD} when the current exhibit a step (ΔI) greater than a defined value. When an appropriate criterion is used (step-height), this method is useful for identifying the time at which the first percolation path (t_{BD_b}) is formed. The third detection method is the most complicated one since it analyzes the noise of the *I-t* trace. Hence, the t_{BD} is obtained when the noise amplitude is greater than a defined threshold value ($N_{threshold}$).

4.1.4 Statistical TDDB data analysis

Even when the t_{BD} is extracted in identical devices in the same wafer, the percolation path does not appear at the same moment. Therefore, the t_{BD} is a statistically distributed parameter. Although a histogram plot can be used to represent the t_{BD} values, a cumulative failure distribution function (CDF) $F(t)$ is more suitable since it enables further in-depth analysis. $F(t)$ is the probability that a randomly chosen device will fail by time t and is related to the reliability function $R(t)$ through the following expression:

$$F(t) = 1 - R(t) \tag{4.1}$$

where R(t), also called as the survivor function, is defined as the probability of operating without failure to time t.

Specifically, in the dielectric degradation, $F(t)$ indicates the probability for the formation of a percolation path before or at the time t under a defined stress condition.

There are many reliability distribution functions such as Poisson, Exponential, Normal, Log-Normal, Weibull, Multi-Model, and Bi-Modal distributions. Nevertheless, the Log-Normal and the Weibull distributions are frequently more considered for situations in which a skewed distribution for a nonnegative random variable is needed. For instance, in the case of dielectric reliability, it has been demonstrated that the statistical distribution of the t_{BD} in TDDB data by using SiO_2 dielectric follows a cumulative Weibull distribution function [127], [128] given by the equation:

$$F(t) = 1 - exp\left[- \left(\frac{t - \gamma}{\eta} \right)^{\beta} \right] \tag{4.2}$$

where β is the shape parameter, η is the scale factor or 63.2% value and γ is the time delay or burn-in time (normally assumed $\gamma = 0$). By rewriting the Eq. 4.2, the Weibull failure distribution can be expressed as:

$$ln[-ln(1 - F(t))] = \beta\, ln(t) - \beta\, ln(\eta). \tag{4.3}$$

A plot of $ln[-ln(1 - F(t))]$ vs. $ln(t)$ is commonly called Weibull plot and yields a straight line with a slope β and an intercept $ln(\eta)$. The corresponding probability density function $f(t)$ and the hazard rate or failure rate $\lambda(t)$ can be calculated as follow:

$$f(t) = \frac{dF(t)}{dt} = \frac{\beta}{\eta} \left(\frac{t}{\eta} \right)^{\beta - 1} exp\left[- \left(\frac{t}{\eta} \right)^{\beta} \right], \tag{4.4}$$

$$\lambda(t) = \frac{f(t)}{1 - F(t)} = \frac{\beta}{\eta} \left(\frac{t}{\eta} \right)^{\beta - 1}. \tag{4.5}$$

The plot of the failure-rate changes over the lifetime of the device/product is normally called the bathtub curve because it starts high, then is reduced, and finally increases towards the end of the product life. Depending on the β parameter in Eq. 4.5, one can identify three categories in the curve as shown in Figure 4.6 [6].

1. A decreasing failure rate ($\beta < 1$) indicates that the population will have defective items that will fail within the first few weeks to months of the product lifetime (infant mortality). This is mainly attributed to extrinsic failures (manufacturing defects and structural weakness).

2. A constant failure rate ($\beta = 1$) corresponds to the useful life of the device with random failure over time.

3. An increasing failure rate ($\beta > 1$) shows the "wear-out" region attributed to the accumulated damage. Therefore, devices start to fail with increasing frequency.

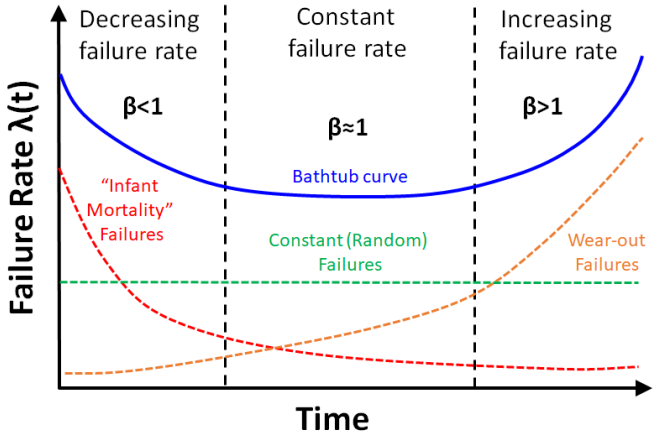

FIGURE 4.6: The bathtub curve showing three categories over the device lifetime

To estimate the cumulative failure distribution $F(t)$, the t_{BD} data are initially sorted from the smallest to the largest value. Subsequently, a ranking algorithm is applied. The most appropriate one is the median ranking [128], but its exact calculation is rather complicated. However, enough good results are obtained by using the Benard's approximation below:

$$F(t_{BD_i}) = \frac{i - 0.3}{n + 0.4} \tag{4.6}$$

where i is the number of the failed device and n is the total number of tested devices.

Additionally, it is possible to evaluate whether the data follow the Weibull distribution or not by using the aforementioned Weibull plot $(t_{BD\_i}, F(t_{BD\_i}))$. Figure 4.7 summarizes the data analysis procedure for TDDB experiments, where it is required 1) the extraction of the t_{BD} from each *I-t* trace during a CVS test, 2) the ordering from the smallest to the largest the t_{BD} values followed by the extraction of the $F(t_{BD\_i})$, and 3) a suitable fitting procedure of the $F(t_{BD\_i})$ in a Weibull plot.

Figure 4.8 depicts an example of a Weibull plot of the cumulative density function vs. measured t_{BD}. Two different slopes appear in the plot and are associated with two failure modes. The early failures have a more spread distribution characterized by a small β value due to extrinsic breakdown, as shown in the bathtub of Figure 4.6. This signature indicates that defects, which can be related to process-induced damage or weak spots, are present in the structure before the stress test starts. On the other hand, the t_{BD} of intrinsic failures exhibits a narrow distribution with a large β value. The intrinsic breakdown is caused by electrical stress instead of pre-existing defects and represents the real lifetime of the device.

It is worth noting that in TDDB analysis, a low β parameter ($\beta < 1$) could still refer to intrinsic failures since it is strongly related to the number of defects involved in a percolation path (N_{min}) [128], as shown in the following:

$$\beta = m \times N_{min} \tag{4.7}$$

where m is the trap generation rate and N_{min} is the minimum number of traps to

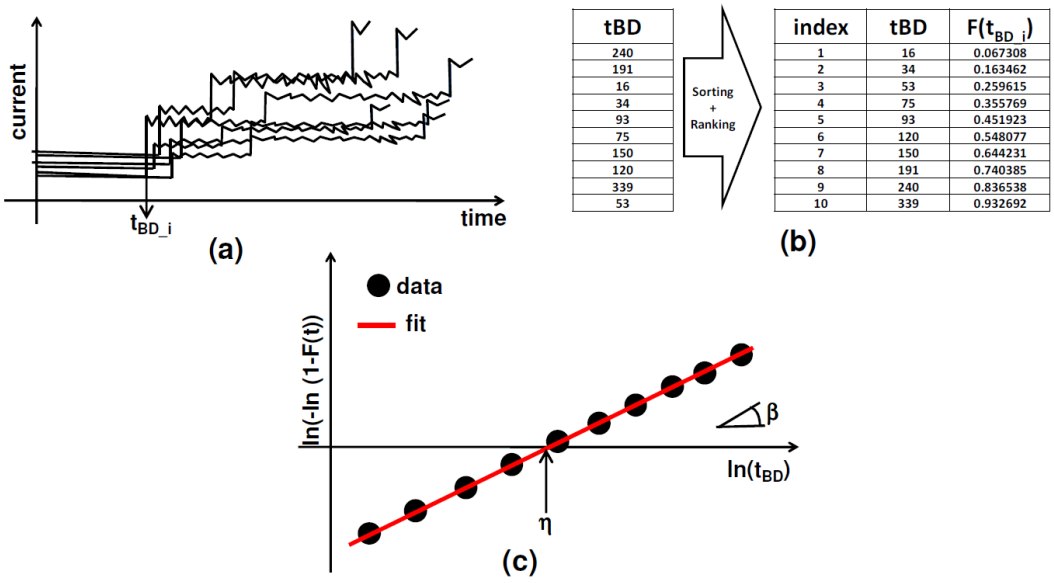

FIGURE 4.7: Analysis of a TDDB experiment: (a) The t_{BD} is extracted from the *I-t* traces; (b) the t_{BD} values are firstly ordered from the smallest to the highest, then the cumulative failure distribution $F(t_{BD\_i})$ is calculated; (c)$F(t_{BD\_i})$ is visualized in a Weibull plot to verify if the data are Weibull distributed and finally, the fitting parameters β and η are obtained [126].

form the percolation path. Moreover, m relates at any time the oxide defect density. By considering the ideal case of zero initial defects, m is given by the following expression:

$$D_{ot} = c \times t_{stress}^{m} \tag{4.8}$$

where c is a parameter function of the stress condition and t_{stress} is the stress time.

It has been demonstrated that m is in a range between 0.35 and 0.4 and does not depend on dielectrics (SiO_2, SiON, HfSiON and HfO_2) [129]. Therefore, by considering Eq. 4.7 with $m < 1$, β can be below 1 despite the mechanism is intrinsic. Figure 4.9 illustrates the expected intrinsic β as a function of the number of traps needed to form the percolation path (Eq. 4.7).

By considering the time-dependent breakdown theory, the percolation path is randomly created in the device area. Therefore, devices with identical dielectric thickness, but with a large area fail earlier than devices with a small area. If it is considered that a large area capacitor A_1 is formed by n small area capacitors A_2, and by using the property of series reliability systems (i.e. a system fails if any of its components fails), $F(t)$ of capacitors with area A_1 ($F_{A_1}(t)$) can be related to $F(t)$ of capacitors with area A_2 ($F_{A_2}(t)$) as follows:

$$ln[-ln(1 - F_{A_1}(t))] = ln\left(\frac{A_2}{A_1}\right) + ln[-ln(1 - F_{A_2}(t))] \tag{4.9}$$

where it is easy to obtain the equation:

$$\eta_1 = \eta_2 \left(\frac{A_2}{A_1}\right)^{1/\beta}. \tag{4.10}$$

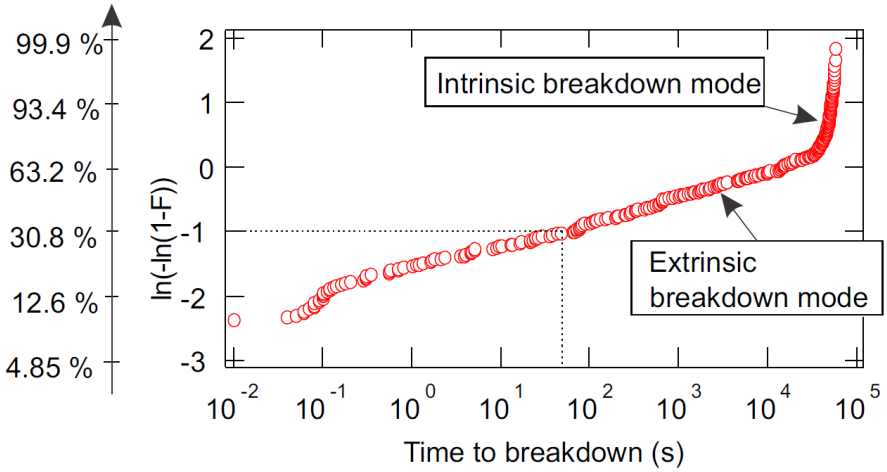

FIGURE 4.8: Weibull plot with two slopes (β) corresponding to the extrinsic and intrinsic failure modes [6].

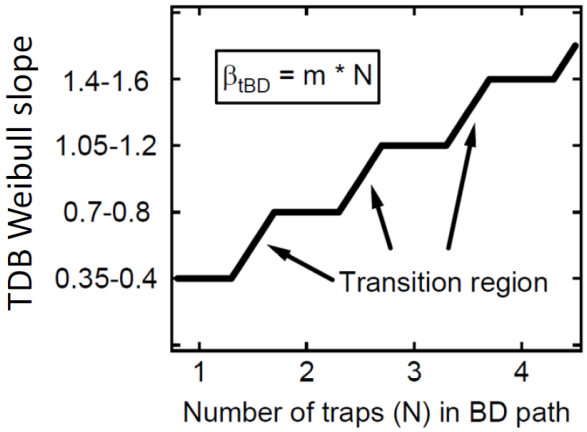

FIGURE 4.9: The t_{BD}-Weibull slope (β_{tBD}) vs. the number of traps N to form the percolation path. Since certain event to form percolation path could be caused by either N or N+1 traps, a transition region between the different levels is observed [128].

Consequently, $F(t)$ follows the area scaling law in devices with the same dielectric thickness and different areas, i.e. the Weibull plot shows parallel failure distributions (similar β) that are laterally shifted by the $(A_2/A_1)^{1/\beta}$ factor. Additionally, $F(t)$ of any A_i area device can be referred to a common reference area A_1 by means of Eq. 4.9. As a result, under homogeneous stress and degradation, the distributions vertically scale and line up as observed in Figure 4.10 [128].

TDDB experiments in devices with different areas are helpful to analyze whether extrinsic or intrinsic failures provoke the time-dependent breakdown. If the percolation path is created due to process-induced defects or weak spots in devices (extrinsic failures), the distributions do not vertically align when they are referred to a common area showing that the area scaling law is not applicable. On the contrary, if the distributions are nicely lined up, the breakdown could be related to intrinsic defects even when β exhibits low values [128], [126].

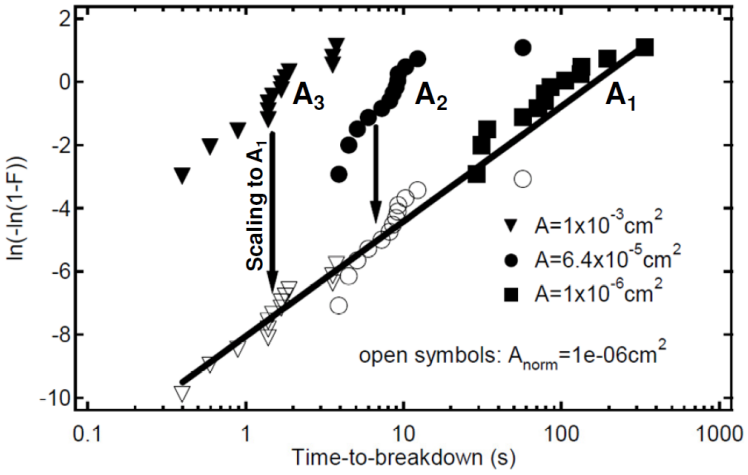

FIGURE 4.10: Area scaling example. Under uniform degradation, the t_{BD} distribution measured on devices with different areas (A1, A2 and A3), nicely line up when they are scaled to a reference area (A1 in this case) [128].

4.1.5 Lifetime extrapolation

In order to predict the device lifetime, accelerated stress conditions (temperature, voltage, humidity, etc.) are used to induce the breakdown time in a feasible time. In the specific study of dielectric reliability by using TDDB data, each stress condition leads to a Weibull failure distribution from which β and η parameters can be obtained.

By considering a common breakdown mechanism for all stress conditions, the Weibull plot depicts failure distributions $F(t)$ with similar slopes (parallel to each other) and only shifted by the η factor as shown in Figure 4.11 (a). It is worth noting that η is clearly a function of the stress condition while, on the contrary, β is intrinsically related to the dielectric thickness.

Once the η parameter (i.e. the lifetime of the 63.2% of the device population) is extracted from all the failure distributions under different stress conditions, it is possible to plot these values as a function of the applied conditions as illustrated in Figure 4.11 (b). Subsequently, an appropriate model can fit this relation and allow predicting when 63.2% of the devices will fail under operating/normal conditions. By adopting the area scaling law (Eq. 4.10), the lifetime of any arbitrary area device can also be predicted. Additionally, Figure 4.11 (b) also depicts the easy scaling of the device lifetime to a different fraction (x%) of the population for a given operating condition. Conversely, the operating condition that guarantees a given expected lifetime for x% of the population can also be extracted.

As previously mentioned, the lifetime extrapolation strongly depends on the fitted model. When voltage-accelerated tests are used, the t_{BD} is measured at very high fields while the device normally operates at a much lower field. Therefore, the accuracy of the dielectric reliability prediction at operating conditions is based on the correctness and validity of the extrapolation law. Two models have been proposed for thick oxides ($t_{ox} > 5$ nm). They are known as "E-model" and "1/E-model" because, for that thickness, the electrons are injected into the conduction band of the

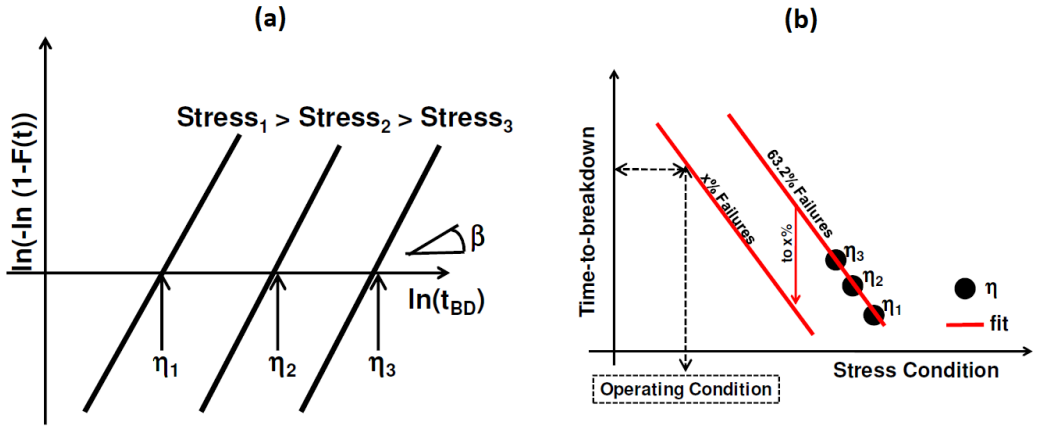

FIGURE 4.11: (a) Schematic Weibull plot under 3 different stress conditions resulting in η_1, η_2 and η_3. (b) Illustration of the long-term extraction of the t_{BD} showing the easy scaling to any x% failure level to know the probability that x% of population fail under operating condition and vice-versa [126].

oxide through the Fowler-Nordheim tunneling mechanism. Consequently, the electric field within the oxide (E_{ox}) determines the energy of the electrons at the anode which is assumed to induce the oxide breakdown.

The E-model predicts a linear relationship between the logarithm of the t_{BD} and the oxide field [127], as follows:

$$t_{BD} = \tau_0 \, exp(-\gamma \times E_{ox}) \tag{4.11}$$

where τ_0 and γ are constants. This model assumes that there is a direct correlation between the electric field and the oxide degradation, but disregards the injected electrons as a previous step for creating oxide traps [127].

On the other hand, the 1/E model , which is based on the anode injection mechanism, follows an exponential law with a reciprocal field dependence:

$$t_{BD} = \tau_0 \, exp\left(\frac{G}{E_{ox}}\right) \tag{4.12}$$

where τ_0 and G are constants.

Both models correctly fit the accelerated-test results. However, they differ in the long-term prediction, which cannot be experimentally measured and validated (e.g. 10 to 20 years). The discussion between both models is normally valid for oxide thickness greater than 5 nm, where the non-ballistic Fowler-Nordheim phenomenon dominates the electron injection. On the contrary, for ultra-thin oxides ($t_{ox} < 5$ nm), the lifetime modeling starts to show a voltage dependence since the injected electrons can directly tunnel through the oxide to the conduction band of the semiconductor. Therefore, the electron energy at the anode is given by the anode-to-cathode voltage difference, which corresponds to the applied gate voltage. As a result, the electric field-based models need to be replaced by voltage-based models such as the "exponential V_G model" and "V_G power law model" [127], [129]. The exponential V_G model is described by:

$$t_{BD} = t_0\, exp(-\gamma \times V_G) \tag{4.13}$$

where t_0 and γ are constants. Initially, this model has been adopted to predict device lifetime of thin oxides. Nevertheless, it presents an inconsistency by predicting a finite lifetime at $V_G = 0$ V (in contrast with the reasonable expectation of an infinite lifetime).

On the other hand, the V_G power law model avoid the aforementioned inconsistency and properly fit the experimental data. This model is defined as:

$$t_{BD} = k_0 \times V_G^{-n} \tag{4.14}$$

where k_0 and n are constants.

As can be seen from Eq. 4.14, the V_G power law model appropriately predicts an infinite lifetime at $V_G = 0$ V. Additionally, this model is supported by the fact that the trap generation also follows the same power law [128]. It is worth noting that temperature plays a relevant role because accelerates the degradation mechanisms. For instance, the scale parameter η (63.2% value) obtained from the Weibull distribution at room temperature is larger than η at elevated temperature [130]. Moreover, the exponent of the V_G power law model n (Eq. 4.14) has also been demonstrated to change [72]. Hence, since the relationship between t_{BD} and the temperature is not so clear, TDDB experiments are normally performed at the target temperature to ensure a proper lifetime extrapolation.

4.2 Reliability Improvements in AlGaN/GaN GET-SBDs

4.2.1 Introduction and state of the art

Nowadays, there are many efforts focused on minimizing losses and saving energy in power electronic applications. Therefore, improvements at the semiconductor level are required to obtain more compact, efficient and reliable systems. Devices based on gallium nitride represent an appropriate choice due to their wide bandgap ($\sim$ 3.4 eV), high operating temperature range [18], high breakdown voltage ($\sim$ 3MV/cm), and the formation of a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN interface which is attributed to the spontaneous and piezoelectric polarization effects [33]. GaN-based devices also benefit from an intrinsic better trade-off between ON-resistance and breakdown voltage, enabling the operation at very high frequencies [16], [17]. Due to all these characteristics not only AlGaN/GaN-based transistors, but also Schottky barrier diodes (SBD) have attracted attention for a variety of applications such as converters, inverters, UPS systems, among others [131–133].

Nevertheless, as mentioned in Chapter 1, power diodes require low turn-on voltage (V_{TON}) and specific on-resistance ($R_{ON,sp}$), low reverse leakage current but high breakdown voltage (V_{BD}) in order to reduce power losses during operation and potential reliability issues. Additionally, the monolithically integration of GaN-HEMT and SBD together in GaN-on-Si technology is still challenging because a high-performance diode with low leakage and low forward voltage is needed to achieve an efficient power system.

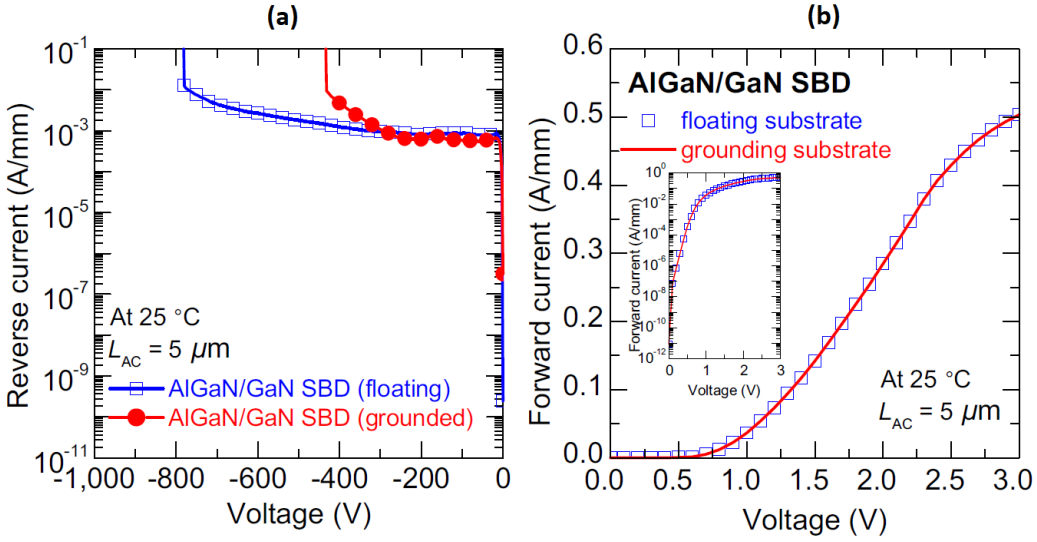

FIGURE 4.12: (a) Leakage current and (b) forward characteristics of AlGaN/GaN SBD in floating and grounded substrate configurations [6].

In this preamble, several approaches have been tried to improve the performance of GaN-on-Si rectifier in the past years. For instance, it was reported that using a recessed anode is possible to decrease the V_{TON}, thus, the specific on-resistance of SBDs [134]. However, the anode-recess technique can also impact on the electrical properties of diodes because it activates traps with relatively short capture and release times leading to a higher degradation of the *I-V* characteristics in short reverse stress experiments [135]. Furthermore, single and multi-field plate structures have been adopted to boost the breakdown voltage in SBDs to avoid premature breakdown due to the electric field concentration at the edge of the Schottky barrier electrode [136], [137]. A combination of both techniques (recessed anode and field plates) has also been implemented in AlGaN/GaN SBDs with an excellent power figure-of-merit (FOM) $V_{BD}^2/R_{ON,sp}$ [134]. For the special case of leakage current reduction, several studies were focused on the design of device architectures [138], new alternatives for the anode metal [139], and various cleaning process steps [140].

In the Au-free CMOS compatible process developed by imec, the SBDs fabricated initially exhibited a high leakage current of 1 mA/mm and a lower V_{BD} (400 V) with a grounded substrate, while excellent forward characteristics were observed independently of the substrate connection due to the low voltage bias at the surface as depicted in Figure 4.12. This high leakage current was attributed to the presence of a high electric field at the perimeter of the Schottky contact in the off-state [141]. Hu [6] investigated two device architectures to achieve a low leakage current and demonstrated that the peak electric field located at the corner of the Schottky contact is reduced by introducing a Si_3N_4 layer to create a gated edge termination (GET) at the anode area next to the Schottky contact [51]. As a result, the leakage current, which is highly dependent on this peak electric field, decreases around four orders of magnitude as shown in Figure 4.13. Moreover, an AlGaN barrier recess process was also adopted in these GET-SBDs to decrease the tunneling distance. Therefore, electrons can easily overcome or tunnel through the energy barrier resulting in low ON-state voltages.

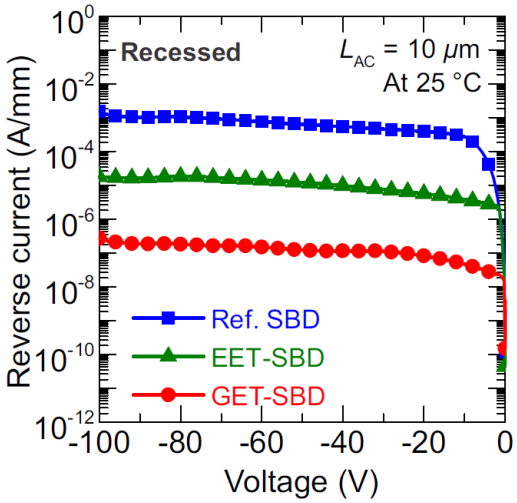

FIGURE 4.13: Leakage characteristics comparison of two device architecture (EET-SBD and GET-SBD) in the Au-free CMOS process developed by imec. A significant drop in leakage can be achieved by using the GET-SBD architecture [6].

Although GaN-based transistors and diodes exhibit superior characteristics and have improved in performance over the years, widespread adoption in power applications is still limited, because the product-level reliability has not been fully verified. Several studies on the main failure mechanisms and long-term reliability have been performed [88, 103, 142–144]. Specifically, GET-SBDs have shown good device reliability under ON-state stress [145]. By using different stress conditions and considering a variety of geometries [146], [147], the degradation mechanisms responsible for the turn-ON voltage (V_{TON}) and ON-resistance (R_{ON}) shift have been reported. Nevertheless, the response to the OFF-state stress of the GET technology has not yet received sufficient attention and only a few works are presented in the literature [148]. This study aims to provide a more comprehensive analysis of the time-dependent breakdown in AlGaN/GaN GET-SBDs fabricated in a 200-V GaN-on-Si platform technology by evaluating their dependence on the GET structure, passivation layer thickness, and preclean process. The time-dependent dielectric breakdown (TDDB) method was adopted since the leakage degradation follows the same behavior as observed in gate oxide layers [72].

4.2.2 Device fabrication

The simplified structure of the AlGaN/GaN diodes studied in this paper is sketched in Figure 4.14 (a). The epitaxial stack is grown on Si (111) substrate by means of metal- organic chemical vapour deposition (MOCVD). It features a 2.9-μm-thick superlattice buffer designed for a 200-V platform technology with a 300-nm-thick GaN channel, a 0.5-nm-thick AlN spacer, a 10-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier, and a 5-nm-thick *in situ* Si_3N_4 cap. The epitaxial stack is passivated with a SiO_2 layer by using high-temperature oxide deposition.

In the anode region, the passivation layer is removed by dry etch and the barrier is recessed by about ∼6 nm by atomic layer etching leaving an AlGaN thickness of ∼4 nm. The GET structure is obtained by depositing a 45-nm-thick Si_3N_4 layer by means of plasma-enhanced atomic layer deposition (PEALD) with a subsequent

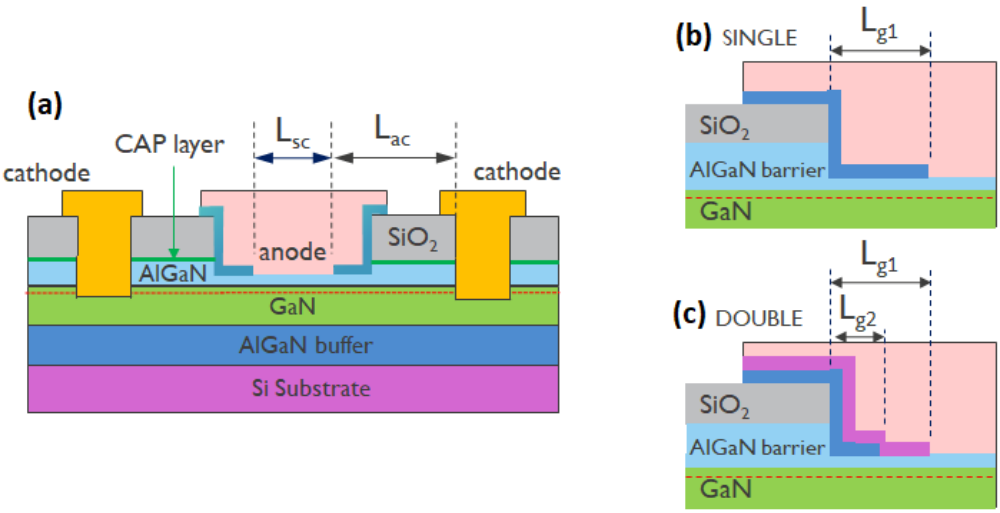

FIGURE 4.14: (a) Simplified schematics of AlGaN/GaN GET-SBDs used in this study. The detailed cross sections show GET with (b) single and (c) double structures.

TABLE 4.1: Summary of important device characteristics

Device denomination	*Passivation thickness*	*GET structure*	*Preclean treatment*
REF	140 nm SiO_2	45 nm Si_3N_4	Dilute HCl
DOUBLE GET	140 nm SiO_2	45 + 45 nm Si_3N_4	Dilute HCl
THIN PASS	45 nm SiO_2	45 nm Si_3N_4	Dilute HCl
THIN PASS (preclean)	45 nm SiO_2	45 nm Si_3N_4	SPM + APM

opening by dry etch in the central region with length $L_{sc} = 5\ \mu$m, which results in an edge termination length $L_{g1} = 1\ \mu$m [see Figure 4.14 (b)]. The recess process of the AlGaN barrier and the gated areas provided by the GET layer result in an effective reduction of the leakage current in reverse operation [53]. Before the deposition of the anode metal, a cleaning treatment based on dilute HCl is used to remove any residual material from the AlGaN surface. An Au-free TiN-based metal stack is deposited and etched to form the Schottky contact at the anode region. It worth noting that two-level anode field plates (FPs) are also fabricated on the SiO_2 passivation layers toward the cathode as depicted in the cross-sectional SEM image of the anode region in GET-SBD (see Figure 4.15). Finally, the ohmic contacts are fabricated using a Ti/Al-based metal stack with alloy temperature of 565 °C. As a result, the diode features a symmetric structure with a central anode contact (Schottky contact to the AlGaN) surrounded by two separate cathodes (ohmic to the 2DEG). A more detailed description of the diode layout and processing steps is reported in [51] and [149].

As summarized in Table 4.1, the reference device structure (REF) has a 140-nm-thick SiO_2 passivation layer, a single-GET layer, and an HCl-based preclean treatment. To study the GET structure dependence, an extra Si_3N_4 layer with the same

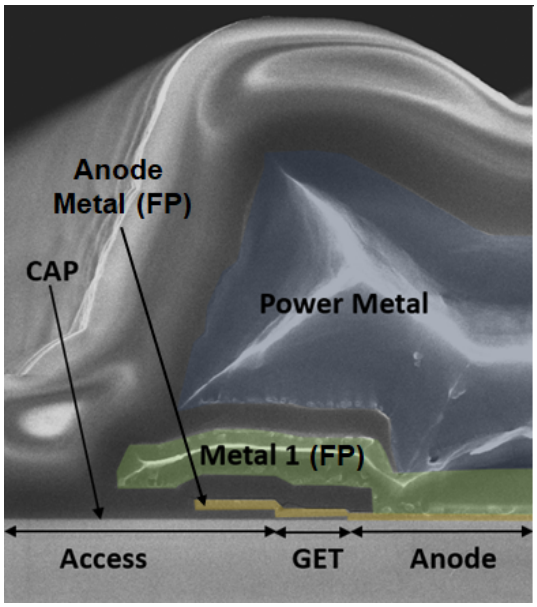

FIGURE 4.15: Cross-sectional SEM image of the fabricated GET-SBD.

thickness is deposited and etched before the main GET layer with $L_{g2} = 0.5$ μm as illustrated in Figure 4.14 (c). To analyze the passivation thickness dependence, an additional split with 45-nm-thick SiO_2 was fabricated. Additionally, a more aggressive preclean process based on sulfuric acid and hydrogen peroxide mixture (SPM) and ammonia and hydrogen peroxide mixture (APM) was used before the GET layer deposition in one of the wafers to compare its influence on the time to failure.

4.2.3 Experimental procedure

The I–V characteristics of the reference devices during the ON-state and OFF-state demonstrate excellent DC performance as observed in Figure 4.16 (a) and (b). The values of turn-ON voltage V_{TON} (i.e., V_{ac} extracted at 1 mA/mm), forward voltage V_F (i.e., V_{ac} at 100 mA/mm), and leakage current (i.e., I_{ac} at $|V_{ac}| = 99$ V) are around 0.6 V, 1.25 V, and 10 nA/mm at room temperature, and 0.55 V, 1.4 V, and 0.1 μA/mm at 150 °C, respectively. The pulsed I–V measurements by switching the device from OFF-state to ON-state show a remarkable low R_{ON} dispersion (less than 10%) at 25 °C and 150 °C as depicted in Figure 4.17 (a) and (b). Such low dispersion values can be attributed to a comparatively low gate fringing capacitance [150–152] and low electron conduction through surface trap states [153] when SiO_2 is used as a passivation layer. Starting from this state-of-the-art reference structure, the time-dependent breakdown has been analyzed for the splits described in Table 4.1 to further optimize the long-term reliability of the device.

Figure 4.18 illustrates the I_{ac}–$|V_{ac}|$ curve during the reversed sweep for all devices described in Table I. With the substrate floating, the reverse bias was applied at the cathode while the anode was connected to ground. Initially, when a reverse bias is applied to the diode, the voltage drops mainly within the barrier and the leakage current is due to vertical tunneling. Once the channel is completely depleted, the resistance between anode and cathode increases and the additional voltage drops in the anode-cathode region. This results in a slow increase of the current with weak reverse-bias voltage dependence. It is worth noting that all devices exhibit similar

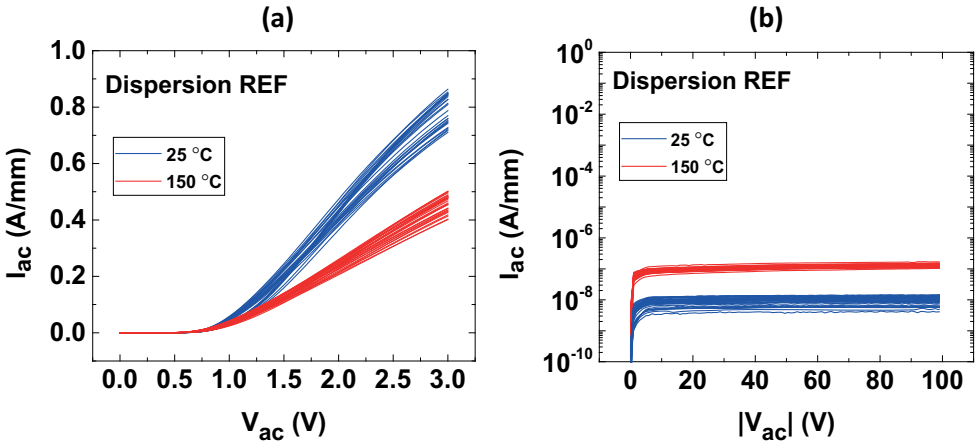

FIGURE 4.16: (a) Forward and (b) reverse characteristics of the AlGaN/GaN GET-SBD.

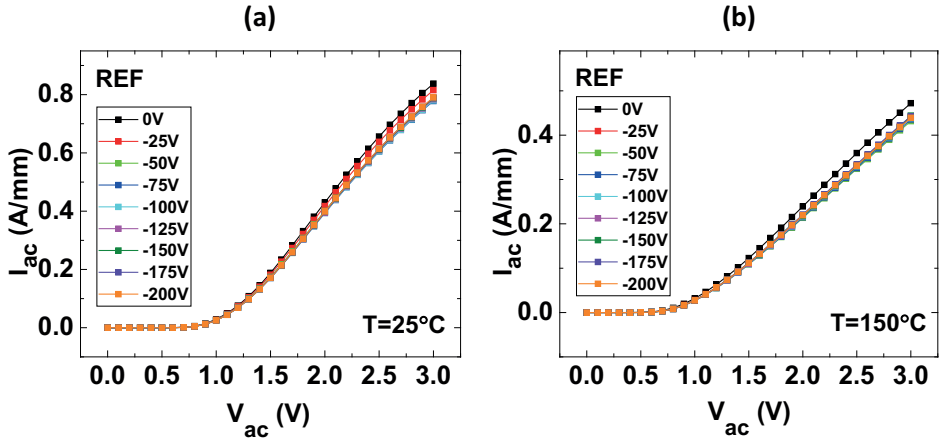

FIGURE 4.17: Dispersion measurement at (a) room and (b) elevated temperatures. Pulsed I–V measurements were performed with a Keysight B1505A. Graph legend: OFF-state biases.

leakage currents; thus, premature failures due to higher initial leakage values as in [154] are not observed in this paper. Based on Figure 4.18, the stress voltage conditions for the TDDB measurements were selected sufficiently close to the DC breakdown voltage to induce the breakdown within a feasible time frame. The selected stress voltages vary between 375 V and 625 V, well above the intended operating voltages of the technology.

The TDDB experiments were performed on devices with an anode-to-cathode distance $L_{ac} = 6$ μm and width $W = 100$ μm by using a constant voltage stress approach (CVS) in which a high voltage is applied to the device, while the current variation is monitored (Subsection 4.1.3). In all the presented measurements, the stress voltage was applied at the cathode, while the anode was grounded and the substrate was kept floating. The time to breakdown t_{BD} is defined when a variation in the current is greater than 1 μA. Furthermore, higher temperatures (150 °C and 200 °C) were used to accelerate degradation.

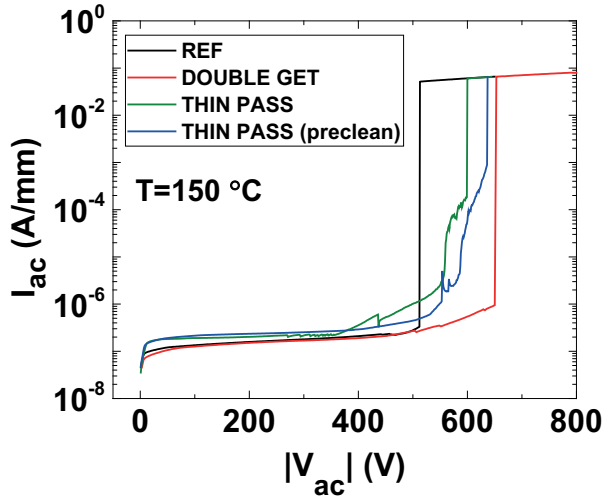

FIGURE 4.18: Typical results of DC breakdown measurements in the analyzed samples where the double-GET structure shows the highest V_{BD}.

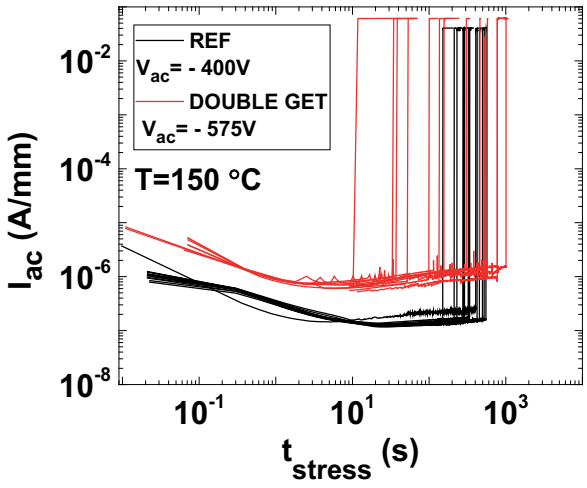

FIGURE 4.19: Results of CVS experiments for one stress condition in single- (REF) and double-GET (DOUBLE GET) structures.

4.2.4 Results and discussion

Structure dependence (GET region)

As can be seen from Figure 4.18, the double-GET structure region exhibits a remarkable improvement in the breakdown voltage V_{BD} with a difference of more than 100 V compared to the single-GET structure reference (REF). The selected stress voltages for the double-GET structure are, therefore, also significantly higher (575 – 625 V) than those for the single-GET structure (350 – 450 V). The evolution of the current at one specific stress condition for both structures is shown in Figure 4.19.At the beginning of the stress, the leakage current exponentially decreases and this could be attributed to electrons injected from the anode into the AlGaN layer [155]. After a certain stress period, the current starts to increase and becomes noisy, which is frequently attributed to the generation of defects at gate edges due to high electric fields [156] or the creation of donor defects in the GaN buffer [157]. Figure 4.20 (a) and (b)

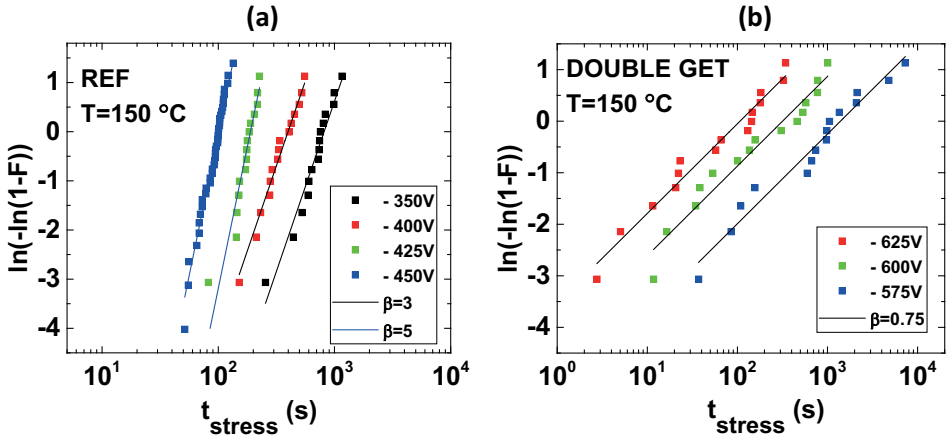

FIGURE 4.20: Weibull distribution for different stress conditions in (a) single-GET (REF) and (b) double-GET (DOUBLE GET) devices.

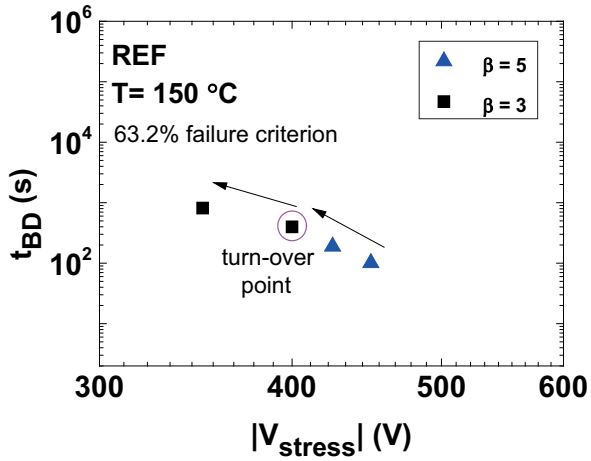

FIGURE 4.21: Time to have 63.2% failures in the single-GET structure for the breakdown mechanisms with $\beta = 3$ and $\beta = 5$.

shows that t_{BD} follows a Weibull distribution with a cumulative failure function:

$$F(t) = 1 - exp\left[- \left(\frac{t}{\eta} \right)^{\beta} \right] \tag{4.15}$$

where the time, scale, and shape parameters are t, η, and β, respectively. This expression is derived from the general form (see Eq. 4.2) by assuming the burn-in time $\gamma = 0$.

On the one hand, the reference device with a single-GET structure shows a t_{BD} distribution with two large shape parameters ($\beta = 3$ and $\beta = 5$) as observed in Figure 4.20 (a), which suggest that the breakdown is related to the intrinsic properties of the material rather than extrinsic failures [158]. By plotting the time corresponding to 63.2% failures in the device population (η) as a function of the stress voltage in the single structure as shown in Figure 4.21, it can be seen that the $\beta = 5$ mechanism exhibits a slightly stronger voltage dependence and the turn-over point from one mechanism to the other is around 400 V.

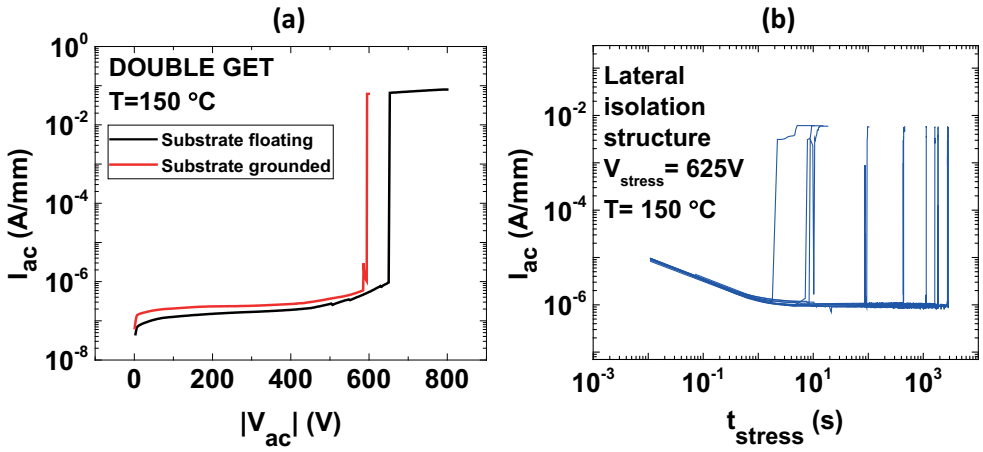

FIGURE 4.22: (a) Reverse DC bias sweep with the substrate floating and grounded in double-GET devices. (b) CVS experiments in lateral isolation structures.

On the other hand, the double-GET devices do not break in the defined time window (50000 s) at the stress voltages used for the single-GET structure. When stressed at very high voltages in the 575 – 625 V range, they exhibit spread t_{BD} distribution with $\beta < 1$ (see Figure 4.20 (b)), which is a characteristic signature for extrinsic failure mechanisms and indicates that the failure rate decreases with time [158]. To understand the origin of this wide distribution, first, a reverse DC bias sweep was performed with the substrate floating and grounded, and lower V_{BD} was observed when the substrate was grounded (see Figure 4.22 (a)).

Additional CVS experiments were performed on a different structure where two electrodes located in separate active islands are connected to the 2DEG with the same anode-cathode distance of 6 μm. By keeping the substrate floating, the time to reach lateral breakdown was measured and similar spread values were observed under the same stress conditions (See Figure 4.22 (b)). Thus, the spread t_{BD} distribution when double-GET devices are submitted to high-stress voltages ($|V_{ac}| > 550$ V) suggests a lateral breakdown through the buffer layers or/and breakdown through the surface [159], but additional investigation is still needed.

2D simulations at the normal operating voltage comparing the single-GET (REF) and double-GET structures show two regions with a high absolute electric field, which act as critical points for the breakdown as illustrated in Figure 4.23. One of them is located at the edge of the Schottky contact and the other at the corner of the GET structure. By adding the second GET layer, a new electric field peak within the AlGaN barrier is formed. This not only alleviates the electric field at the first GET corner but also results in a broad and uniform electric field distribution, which may further improve the breakdown voltage and the time to failure [160], [161].

Passivation thickness dependence

From Figure 4.18, it can be observed that the reduction of the passivation thickness has a positive impact on the DC breakdown voltage with values close to $\sim$ 600 V. The CVS experiments were performed at 200 °C to compare the same stress voltages in the reference and in the thin passivation devices in a reasonable time. One stress

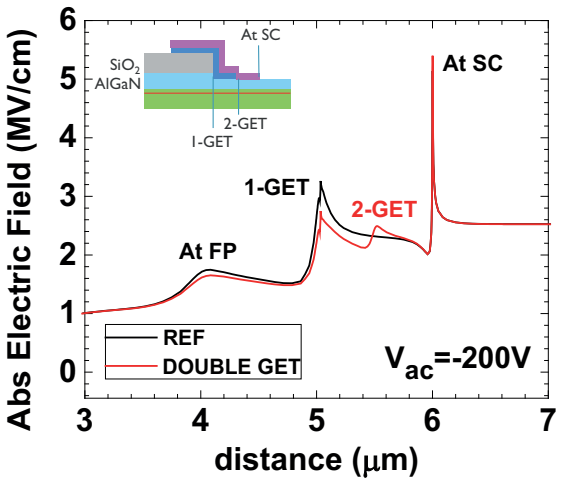

FIGURE 4.23: Line profile of the absolute electric field within the AlGaN barrier (3 nm below the top surface in the recessed portion). The double-GET structure adds a new peak which alleviates the peak at the GET corner.

condition for each structure is shown in Figure 4.24. In both cases, the trapping of negative charges at the beginning of the stress test is again observed, but a more rapid increase in the leakage current is observed in the thin structure. At the same stress conditions (375 and 400 V), t_{BD} in both cases has similar shape parameters ($\beta \sim 3$) as illustrated in Figure 4.25 (a) and (b). Thus, the failure mechanism seems to have a common origin. An additional mechanism with $\beta = 5$ is observed in the thin passivation structure, which was also present in the previous structure-dependence analysis at 150 °C in the single-GET (REF) structure. The change from one mechanism to the other also takes place around 400 V. Considering the low-stress voltage range ($\beta \sim 3$) which is closer to the operating voltage, the thin structure shows a significant improvement in the time to failure as depicted in Figure 4.26.

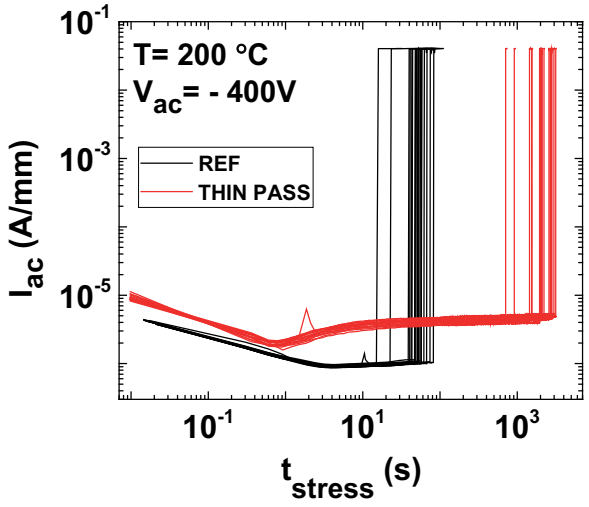

FIGURE 4.24: Results of CVS experiments for one stress condition in thick- (REF) and thin-passivation (THIN PASS) structures.

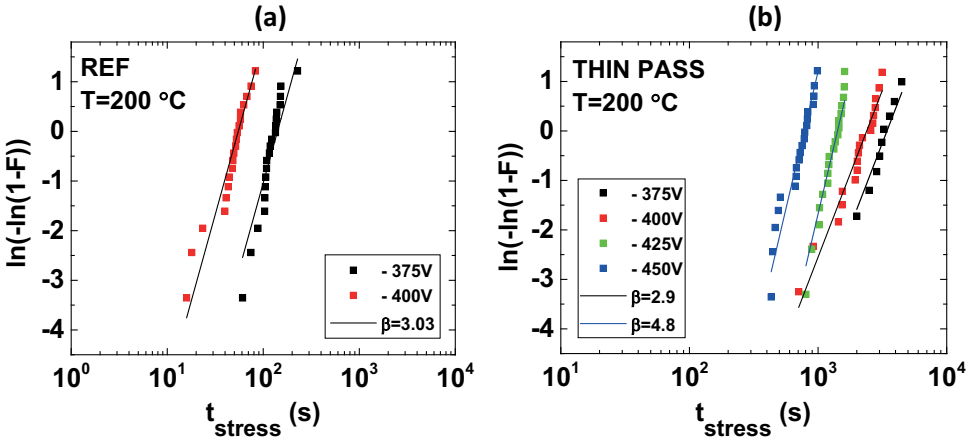

FIGURE 4.25: Weibull distribution for different stress conditions in (a) thick- (REF) and (b) thin-passivation (THIN PASS) devices.

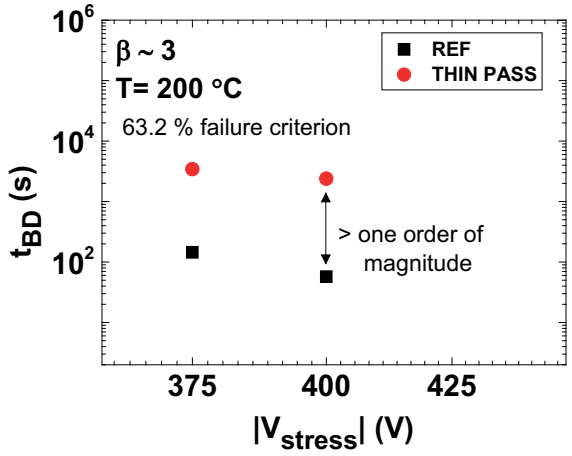

FIGURE 4.26: Time to have 63.2% failures in thick- (REF) and thin-passivation (THIN PASS) diodes for the breakdown mechanism with $\beta \sim 3$.

The TCAD simulation shows how the decrease in the passivation thickness results in a reduction of the peak at the GET corner and an increase in the electric field at the field plate edge while the value at the Schottky contact remains the same (see Figure 4.27). The significant increase of this peak makes the electric field distribution more uniform in the barrier, which improves V_{BD} compared with the reference structure. However, this peak also indicates that the layers beneath the field plate edge are submitted to high electric fields especially if high voltages are applied. Therefore, this could be a limitation to obtain DC V_{BD} values as high as the ones observed in the double-GET devices.

Additionally, both mechanisms ($\beta \sim 3$ and $\beta \sim 5$) follow an Arrhenius law with relatively weak temperature dependence as shown in Figure 4.28, thus suggesting a degradation mainly induced by electric field rather than by temperature. Some previous studies in Schottky-gated high-electron-mobility transistors (HEMTs) have demonstrated that gate degradation has weak temperature dependence with a gradual increase in the leakage current [72]. This behavior has been attributed to the generation of defects in the AlGaN barrier at the gate edge and is possibly induced by

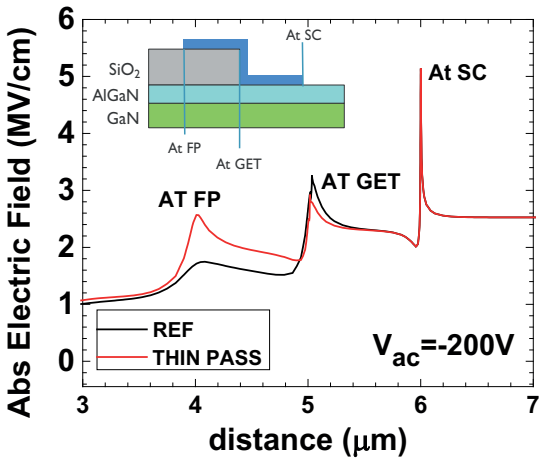

FIGURE 4.27: Line profile of the absolute electric field within the AlGaN barrier (3 nm below the top surface in the recessed portion). The thin-passivation structure reduces the peak at the GET corner.

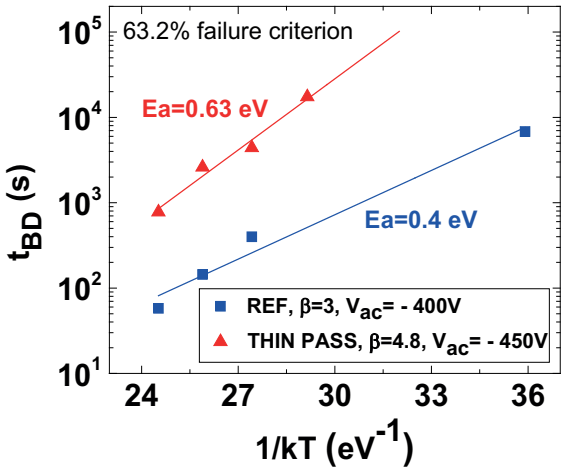

FIGURE 4.28: Arrhenius plot of t_{BD} of the 63.2% of the population (η) in thick- (REF) and thin-passivation (THIN PASS) devices.

the inverse piezoelectric effect [162], a defect/generation percolation process [155], and/or an electrochemical degradation [156]. This could suggest that the observed breakdown takes place around the Schottky contact edge where the maximum electric field is located.

However, low activation energies have been also reported in SiN capacitors [163] and metal-isolator-semiconductor (MIS) HEMTs with this gate dielectric [144]. If it is also considered that the uniform electric field distribution is mainly due to the reduction in the peak at the GET corner and results in a longer t_{BD}, a breakdown through the GET layer could not be discarded. In fact, the observed transition between mechanisms could be related to permanent damage in any of these critical locations, but further investigation is necessary to gain a better understanding of this phenomenon.

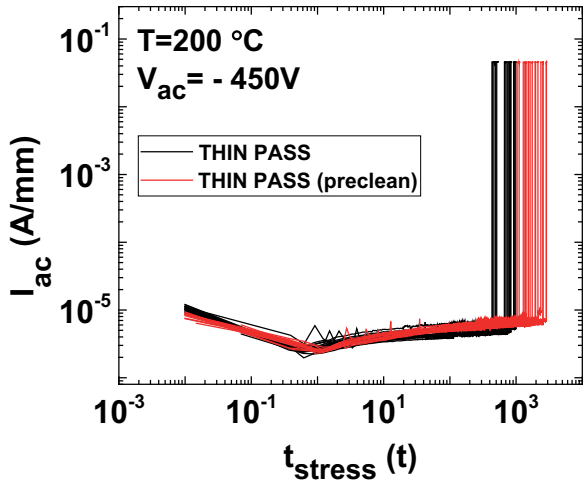

FIGURE 4.29: Results of CVS experiments for one stress condition in diodes with a more aggressive preclean treatment.

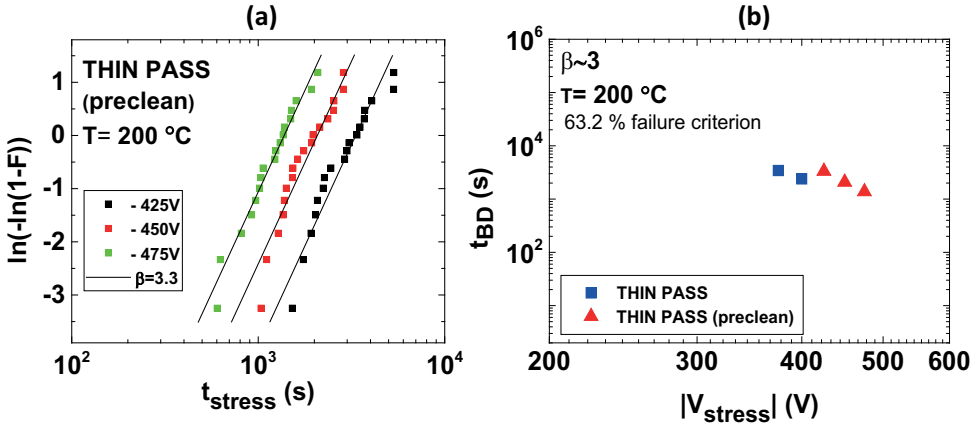

FIGURE 4.30: Weibull distribution for different stress conditions in (a) thick- (REF) and (b) thin-passivation (THIN PASS) devices.

Preclean process dependence

A second generation of thin passivation devices was fabricated with a preclean treatment based on SPM and APM in the recessed AlGaN barrier before the deposition of the Si_3N_4 GET layer. The leakage current remains the same after this treatment (see Figure 4.29) and the shape parameter that better fit the t_{BD} distribution is $\beta = 3.3$ as depicted in Figure 4.30 (a), which is very close to the value extracted in the low-stress voltage range in devices without this preclean process. t_{BD} remains in the same range, but high-stress voltages could be applied without moving to another breakdown mechanism as illustrated in Figure 4.30 (b). Consequently, this preclean process has also a positive influence in terms of reliability and this could be attributed to the reduction of any residual organic material at the SiN/AlGaN interface and at the Schottky contact.

TABLE 4.2: Device characteristics

Device denomination	*Passivation thickness*	*GET structure*
1 GET-THIN	45 nm SiO_2	45 nm Si_3N_4
2 GET-THICK	140 nm SiO_2	45 nm + 45 nm Si_3N_4

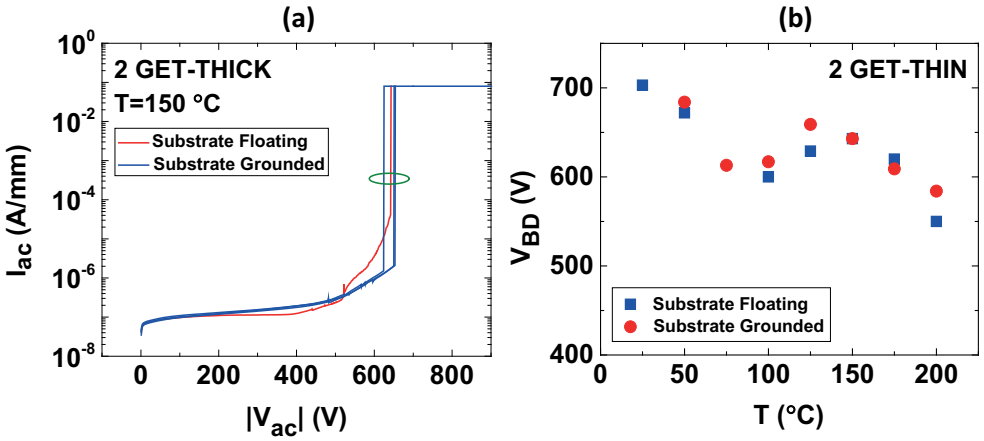

FIGURE 4.31: (a) Reverse DC bias sweep and (b) temperature dependence of the VBD by keeping the substrate floating and grounded in 2 GET-THIN devices.

Buffer impact on TDDB

To be able to determine the intrinsic t_{BD} distribution of the double-GET structure and compare it to the single GET, both architectures have been fabricated on a buffer designed for a 650 V technology. Furthermore, the better results obtained in the single GET structure by thinning the passivation layer and with a more aggressive preclean treatment have also been taken into account during the process steps. The main characteristics of both architectures - the single GET structure with thin passivation (1 GET-THIN) and the double GET structure with thick passivation (2 GET-THICK) - are summarized in Table 4.2.

Figure 4.31 depicts reverse DC sweep results at 150 °C and the V_{BD} as a function of the temperature by keeping the substrate floating and grounded in the 2 GET-THICK. The almost overlapping of the curves and data points indicates that the connection of the buffer does not impact the breakdown mechanism even at different temperatures. Similar behavior was also observed for the 1 GET-THIN devices (not shown). Thus, the use of a 650 V buffer seems indeed to remove the limitations imposed by the 200 V buffer in the previous structure dependence analysis. This result also allowed to do all further measurements from here on (except where specified) with the substrate grounded.

It can be seen from Figure 4.32 that the t_{BD} in all the tested devices still follows a Weibull distribution with a cumulative failure function described by Eq. 4.15. By

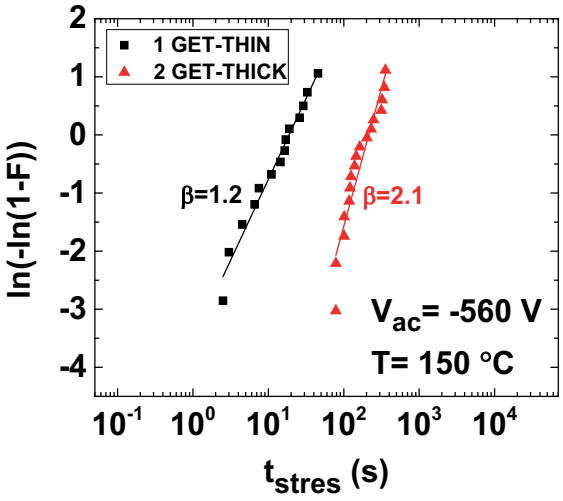

FIGURE 4.32: t_{BD}-distribution obtained from the CVS measurements under the same stress condition for devices described in Table 4.2.

comparing the measurements in the 2 GET-THICK devices with a buffer designed for 650 V with the results in a buffer for 200 V (see Figure 4.20 (b)), a significant improvement in the value of β is observed (from 0.75 to 2.1). Therefore, the extrinsic characteristic of the t_{BD}-distribution when the device was submitted to high-stress voltages was indeed related to a limitation due to the buffer as previously suggested. Therefore, one can now compare directly the two architectures without interference from buffer limitations.

Under the same stress conditions, the 1 GET-THIN devices also show an intrinsic signature, but with a lower shape parameter value ($\beta = 1.2$). The value of η (t_{BD} of 63.2% of the population) is equal to 19 s for 1 GET-THIN and 215 s for 2 GET-THICK devices. This difference in more than one order of magnitude convincingly indicates the advantage of the 2 GET-THICK architecture.

Additionally, 2D-TCAD simulations show a slight decrease of the electric field peak at the first GET corner (1-GET), and a much more reduced peak under the field plate (see Figure 4.33), which ultimately causes a more uniform distribution of the electric field in 2 GET-THICK devices and improves their OFF-state stress behavior.

4.2.5 Conclusions

In this section, the results of the time-dependent breakdown in AlGaN/GaN GET-SBDs have been presented. The starting point of this analysis is a reference structure (REF) with excellent performance under DC and pulse characterization. To study the device reliability, variations in the GET structure, the thickness of the passivation layer, and the use of a preclean process based on SPM+APM have been investigated. The results show that devices with a single-GET structure exhibit intrinsic failure mechanisms with similar shape parameters ($\beta \sim 3$ and/or $\beta \sim 5$). The exponential dependence of t_{BD} on the stress voltage in conjunction with the low activation energy indicates that the degradation process is field dependent while the temperature has a slight influence. The double-GET structure exhibits significantly higher breakdown voltages, owing to the uniform distribution of the electric field by an

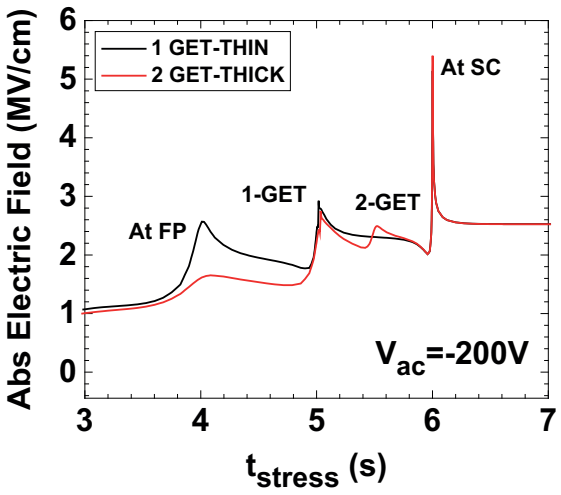

FIGURE 4.33: Absolute electric field within the AlGaN barrier (3 nm below the top surface in the recessed portion). The 2GET-THICK structure distributes the electric field more uniformly by adding a new peak (2-GET) and by reducing the peak beneath the field plate (FP).

additional peak close to the Schottky contact edge. Its Weibull distribution is characterized by a shape parameter $\beta = 0.75$, which is related to breakdown limitation through the buffer. Reducing the thickness of the passivation layer also results in a more uniform distribution of the electric field and a significant improvement in t_{BD}. Moreover, a preclean treatment (SPM + APM) before the GET layer deposition is also observed to improve the time to failure.

Since the double-GET architecture seems to be more promising for long-term reliability but it is limited by the substrate, this structure and its single-GET counterpart have also been fabricated on a 650 V buffer for a direct comparison. TDDB results indeed demonstrate that a more robust buffer can improve the Weibull slope by moving from an extrinsic to an intrinsic signature of the t_{BD}-distribution. Under the same conditions, the double-GET structure with a thick passivation exhibit a narrower Weibull distribution, and a longer t_{BD} compared with the single-GET structure with thin passivation. Finally, the results described within this study can be used as a baseline to increase the long-term reliability in GET-SBDs by combining the advantages of the double-GET structure and the longer time to failure in devices with a thin passivation layer and more aggressive preclean process.

4.3 Influence of GaN- and Si_3N_4- passivation layers on the performance of AlGaN/GaN GET-SBDs

4.3.1 Introduction and state of the art

The relevant characteristics of GaN-based devices (large breakdown field strength, high saturation velocity, high sheet carrier density and electron mobility in 2DEG channel) make them excellent candidates for the next generation of high-power and high-temperature applications. In spite of their potential, widespread adoption is still limited because of several not-fully-understood reliability problems. Many studies have been performed in different structures with the aim of understanding

the phenomena present in these devices: current collapse, large leakage currents, bias temperature instability are a few among many others [88, 103, 142–144]. The understanding of these phenomena is progressing together with the development of engineered structures which aim to improve the device performance.

In particular, in the development of lateral AlGaN/GaN Schottky Barrier Diodes (SBDs), a structure based on the introduction of a thin Si_3N_4 behaving as a gated edge termination (GET) for the anode has demonstrated low leakage current and high breakdown voltage in a CMOS compatible Au-free fabrication process [51]. Recent studies on this structure have demonstrated a reliable behavior during different ON-state stress conditions and by using diverse geometries [146], [147]. In [148], the device reliability has been improved by using metal organic chemical vapour deposition (MOCVD)-Si_3N_4 as edge termination dielectric because of its better bulk quality compared to plasma-enhanced atomic layer deposition (PEALD)-Si_3N_4. Additionally, the behavior during the OFF-state stress has also been reported and identified as a field-related breakdown due to electric field concentration in critical areas such as the GET dielectric corner and the Schottky contact edge. A better distribution of the electric field provided by a thinner passivation layer, a second GET layer and a better preclean process at the Schottky contact region have resulted in a longer time to failure [164] as previously analyzed in Section 4.2.

In order to reduce the electric field crowding and the current collapse in GaN-based devices, surface passivation and field plates are generally adopted [87], [165]. However, the choice of the passivation (or "cap") layer on top of the AlGaN barrier has also been reported to play a significant role, because this layer effectively reduces the dispersion effects by screening the collapse-related surface states/traps from channel [166], [167]. Normally, a thin GaN cap layer is used to avoid the oxidation and damage of the AlGaN surface [168], [169]. Nevertheless, doped and thick GaN cap layers have also been demonstrated to effectively suppress the current collapse [170]. In the same way, SiN_x-based passivation has been reported to reduce the current collapse because of the low state density at the SiN_x/III-N interface [171]. Especially, in situ MOCVD-SiN_x deposited on AlGaN surface has improved the DC performance and dynamic response of AlGaN/GaN HEMTs and MIS-HEMTs [166], [172].

This section discusses the influence of the GaN and Si_3N_4 cap layer on top of the AlGaN barrier layer on the performance and reliability of GET-SBDs. It has been demonstrated that both, GaN cap and Si_3N_4 cap devices, exhibit similar DC characteristics. Nevertheless, a higher density of traps at the SiO_2/GaN interface or/and an increase of the total dielectric constant in the access region result in higher R_{ON}-dispersion in GaN cap devices. The leakage current at medium/low temperatures in both type of devices shows two low voltage-independent activation energies, suggesting thermionic and field-emission processes to be responsible for the conduction. It is also observed voltage-dependent activation energy in the high-temperature range even from low voltages in the GaN cap devices, which limits their V_{BD}. Furthermore, TDDB measurements show a tighter distribution in Si_3N_4 cap devices compared to GaN cap devices. By performing additional measurements in PEALD-Si_3N_4 capacitors with different cap layers and TCAD simulations, it is possible to ascribe the breakdown even at low-stress voltages in GaN cap SBDs to the strong electric field peak within the PEALD-Si_3N_4 at the GET corner, which ultimately accelerates the formation of a percolation path in this dielectric.

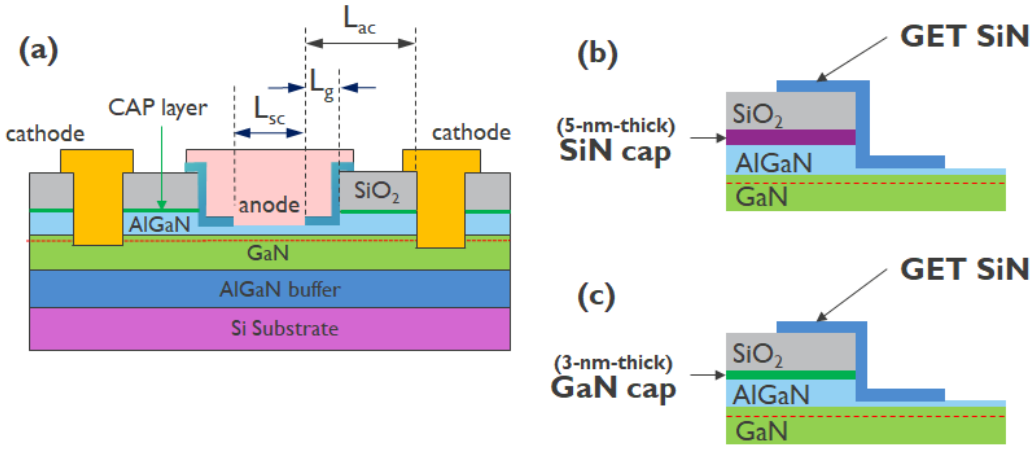

FIGURE 4.34: (a) Simplified schematics of AlGaN/GaN GET-SBDs used in this study. The detailed cross sections show GET with (b) single and (c) double structures.

4.3.2 Device fabrication

For this comparative study, two wafers were processed with the same epitaxial stack, but different cap layers: either a 5-nm-thick Si_3N_4 cap or a 3-nm-thick GaN cap. The device structures were grown on Si (111) substrates by means of MOCVD. The epitaxial structure consists of a 200 nm AlN nucleation layer, a 2800 nm AlGaN buffer, a 150 nm GaN channel, a 0.5 nm AlN spacer, a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier, and finally the cap layers as mentioned above.

The device fabrication starts with the deposition of a 45 nm SiO_2 layer by a high-temperature oxidation process (HTO). Then, this passivation layer is removed in the anode region by dry etch and the barrier is recessed by atomic layer etching until a thickness of ~4 nm is left. A 45 nm PEALD-Si_3N_4 layer is deposited and subsequently opened by dry etching in the central region, which results in the GET formation with length $L_g = 1\ \mu$m. The Schottky contact is obtained after the deposition of an Au-free TiN-based metal stack with length $L_{sc} = 5\ \mu$m. The last step is the deposition of a Ti/Al-based metal stack to fabricate the ohmic contacts. A more detailed description of the GET-SBD process is reported in [51], [6]. A simplified schematic of the device structure with the main dimensions and cap layer thicknesses is shown in Figure 4.34.

4.3.3 Results and discussion

General device characteristics

Table 4.3 summarizes the principal DC and pulse characteristics of the GET-SBDs with different capping layers. The turn-on (V_{TON}) and forward (V_F) voltages were obtained at a current density of 1 mA/mm and 100 mA/mm, respectively, while the leakage current is extracted at $V_{ac} = -99$ V. R_{ON} is extracted from the maximum slope of the *I-V* characteristic. The 2DEG sheet resistance (R_{sheet}) and the contact resistance (R_C) were measured on a Van der Pauw (VDP) and on a TLM structure, respectively, by using the 4-probe measurement technique. The R_{ON}-dispersion

TABLE 4.3: Device DC and pulse parameters with different cap layers

Cap layers	V_{TON} (V)	V_F (V)	R_{ON} $(ohm.mm)$	$I_{leakage}$ (nA/mm)	R_{sheet} (ohm/sq)	R_C $(ohm.mm)$	$R_{ON}-dispersion$ $@RT(\%)$	$R_{ON}-dispersion$ $@150°C(\%)$
Si_3N_4	0.71	1.27	2.10	58.81	334	0.29	9.15	9.5
GaN	0.59	1.14	2.33	24.96	359	0.29	14.42	14.0

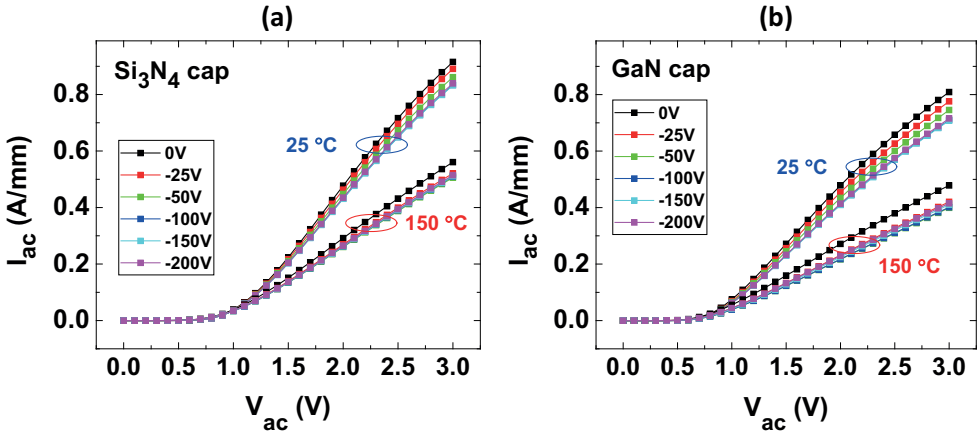

FIGURE 4.35: Dispersion measurements in devices with (a) Si_3N_4 and (b) GaN cap layer at room and elevated temperature. A slight reduction in R_{ON}-dispersion is observed in Si_3N_4 cap devices.

values at 25 °C and 150 °C were obtained from pulsed IV-measurements by switching the device from OFF- to ON-state for different OFF-state biases ranging from 0 to -200 V, as shown in Figure 4.35 and reported in Table 4.3.

This initial characterization shows similar values for most of the parameters for both structures. Nevertheless, the slightly higher R_{sheet} for the GaN cap wafer could be correlated with the decrease of the 2DEG density due to the introduction of negative polarization charge at the GaN cap/AlGaN barrier upper interface [173]. Additionally, the R_{ON}-dispersion also increases for this structure and could be explained by a higher density of traps at the oxide/GaN interface [171], [174]. Moreover, GaN cap devices have a larger dielectric constant in the access region compared to Si_3N_4 cap devices by considering both the passivation and the capping layer, which could also cause the higher dispersion due to an increase of the fringe capacitance as reported elsewhere [152].

Breakdown characteristics

For the breakdown voltage (V_{BD}) extraction, a reverse sweep was performed at different temperatures with the bias applied at the cathode while the substrate and the anode were grounded. At low negative bias, the voltage drops mainly in the AlGaN barrier until the 2DEG channel is completely depleted. With higher negative bias, the anode-cathode resistance increases and any additional voltage then drops within the access region with a weak dependence of the leakage current on the reverse bias, as depicted in Figure 4.36 (a) and (b) [164]. Finally, the V_{BD} is reached when a sudden

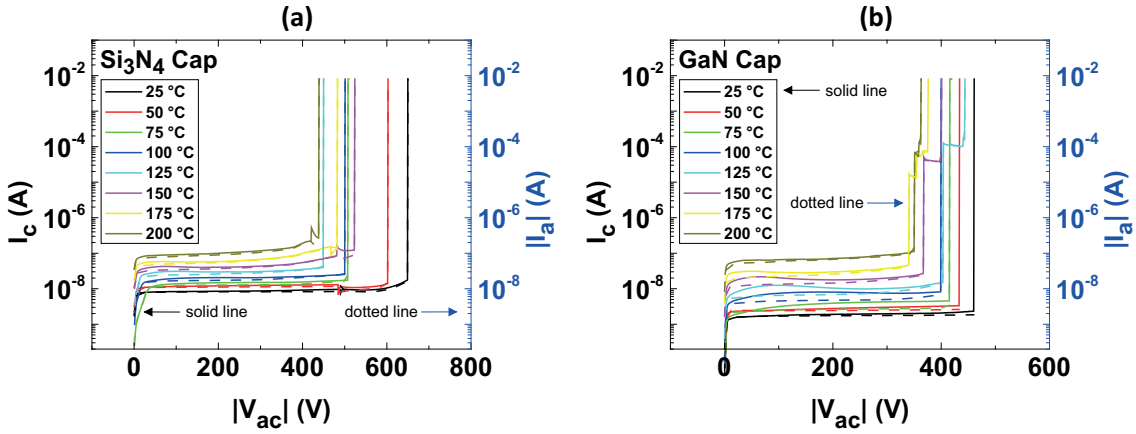

FIGURE 4.36: DC reverse sweep at different temperatures in (a) Si_3N_4 and (b) GaN cap devices with the substrate grounded and floating.

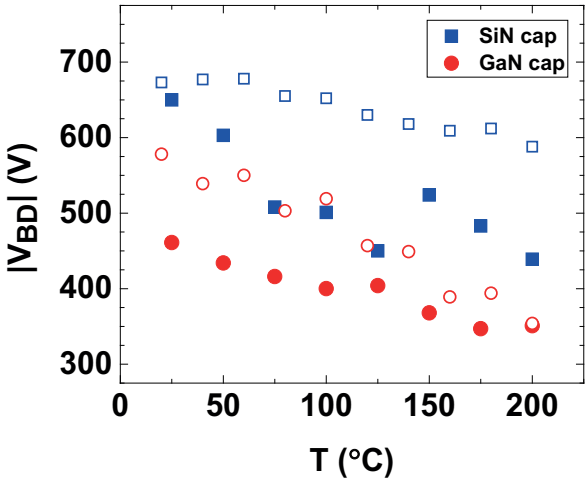

FIGURE 4.37: The extracted V_{BD} in both devices shows a negative temperature coefficient. Closed symbols: substrate grounded. Open symbols: substrate floating.

increase in the current is detected. The extracted V_{BD} results are used later as reference stress voltages in the *accelerated TDDB measurements* subsection. By considering that the anode current is a measure of the diode leakage and the cathode current is the sum of the diode leakage current collected at the anode and the vertical substrate leakage, one can assume negligible substrate leakage due to the almost overlapping of these currents in Figure 4.36.

Furthermore, Figure 4.37 illustrates a negative temperature coefficient of the V_{BD}, which suggests a breakdown mechanism other than impact ionization in both types of devices [175]. It is worth noting that the V_{BD} is higher when the substrate is floating. This is more visible at high temperature in Si_3N_4 cap devices and at low temperature in GaN cap ones. It is inferred that stronger vertical electric fields due to the grounded substrate result in a lower V_{BD}. Especially, it should be noted that GaN cap devices exhibit even lower values compared with Si_3N_4 cap devices.

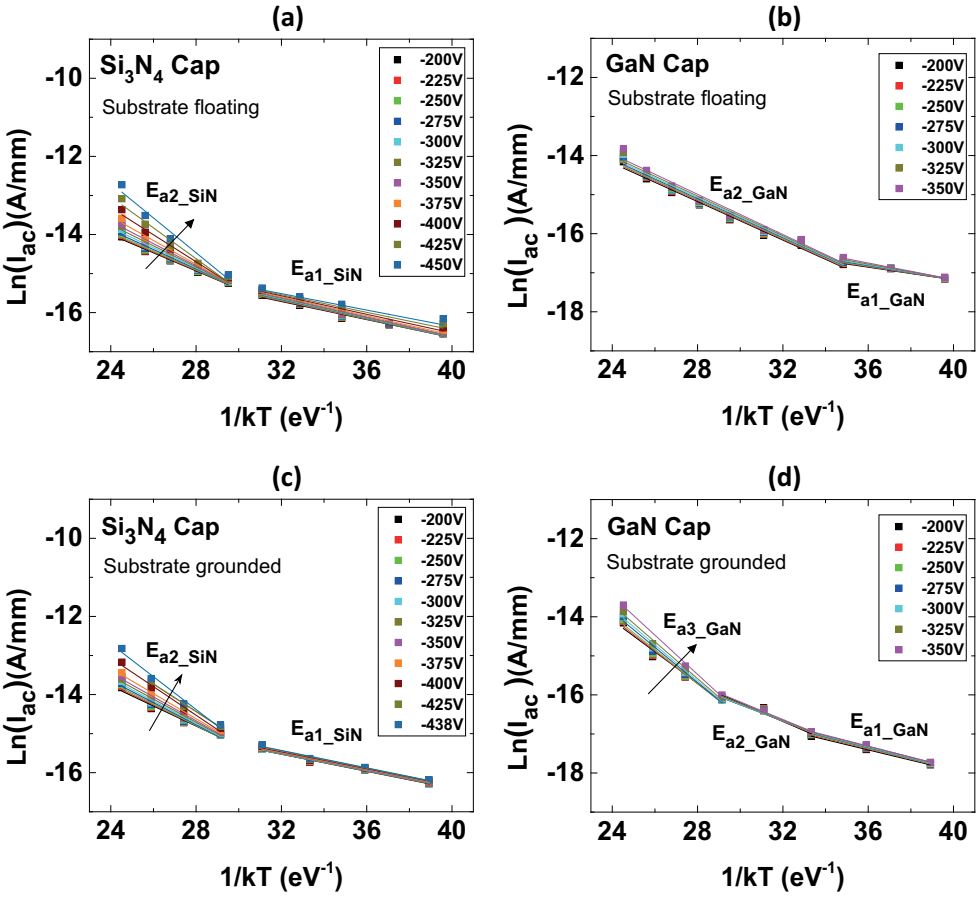

FIGURE 4.38: Activation energy plot of the leakage current of AlGaN/GaN SBDs with (a), (c) Si_3N_4 and (b), (d) GaN as cap layer with the substrate grounded and floating, respectively.

Temperature dependence of the leakage current

To investigate the thermally activated energy levels, we used the I_{ac}–$|V_{ac}|$ characteristics of the GET-SBDs at different measurement temperatures (from room temperature to 200 °C) as shown in Figure 4.36 (a) and (b). For voltages lower than -200 V (operating voltage) and in steps of 25 V, the leakage current is extracted and subsequently depicted in the Arrhenius plots of Figure 4.38. The slopes of the fitting lines are the activation energies according to the following expression:

$$I_{ac} = A\,exp\left(\frac{E_a}{kT}\right) \tag{4.16}$$

where A, E_a, k and T are the pre-exponential factor, the activation energy, the Boltzmann constant , and the temperature, respectively.

Two activation energies are well distinguished in the case of Si_3N_4 cap devices (see Figure 4.38 (a) and (c)). The first one $E_{a1_{SiN}} \approx 0.11$ eV is voltage independent and dominates at the low-temperature range, while the second one E_{a2_SiN} is voltage dependent and appears at elevated temperatures. On the other hand, GaN cap devices exhibit two voltage independent activation energies for the low and medium temperature range, E_{a1_GaN} and E_{a2_GaN}, with values around 0.13 eV and 0.22 eV, respectively. A third activation energy E_{a3_GaN} dominates at high temperature (see

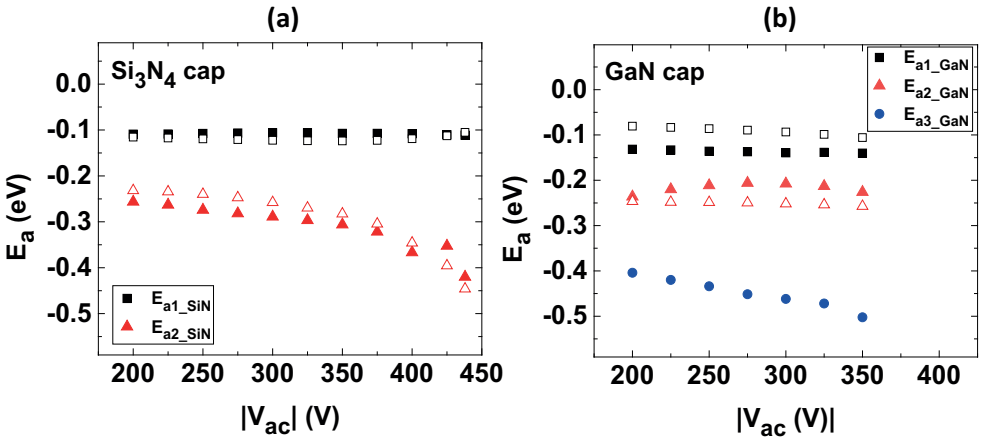

FIGURE 4.39: Evolution of the activation energy with the reversed voltage in (a) Si_3N_4 and (b) GaN cap devices when the substrate was connected to ground (close symbols) and kept floating (open symbols).

Figure 4.38 (d)). It is important to mention that this latter activation energy appears only when the substrate is grounded and is not present when the substrate is kept floating (see Figure 4.38 (b)). Thus, E_{a3_GaN} seems to be related to an intensification of the vertical electric field component.

The behavior of the extracted activation energies as a function of the voltage for both structures is shown in Figure 4.39. Similar low values of E_{a1} have been attributed to surface-based hopping conduction in the literature [176]. However, the value of this activation energy is very similar for both cap layers, thus indicating a minor sensitivity to the surface preparation. Therefore, field-emission transport is more plausible [177], since negligible variations with the applied voltage and weak temperature dependence were observed. The slight increase in E_{a2} compared to E_{a1} for both wafers indicates that the temperature starts to play a role in the conduction mechanism. Additionally, the small variation with the applied bias, for the specific case of E_{a2_SiN} up to 350 V (see Figure 4.39 (a)), suggests a thermionic field emission transport as responsible of the leakage for the medium to the high-temperature range [175]. Above this voltage, E_{a2_SiN} increases to reach values as high as the ones of E_{a3_GaN}.

In order to understand the origin of this activation energy increment and since it appears when the substrate is grounded in the GaN cap wafer as mentioned above, the leakage current through the buffer for both devices was measured in a different structure with only a top anode electrode, as depicted in Figure 4.40 (a). The overlapping of the *I-V* curves indicates that the capping layer does not modify the leakage within the buffer and thus, similar substrate leakages are observed in both devices (see Figure 4.36). An ohmic conduction mechanism characterized by a $I \propto V^m$ behavior with $m \approx 1$ in the low voltage range is observed, while a space charge limited current (SCLC) with $m > 1$ seems to dominate at high voltages [178]. For elevated temperatures, the extracted activation energy is around 0.57 eV for both substrates (see Figure 4.40 (b)). Consequently, a conduction mechanism through the buffer could be responsible for the increase of the activation energy above 350 V in E_{a2_SiN}. The presence of E_{a3_GaN} even at low voltages (200 V) suggests the presence of a higher electric field in the GaN cap devices in the high-temperature range, for which more details will be discussed in the next subsection.

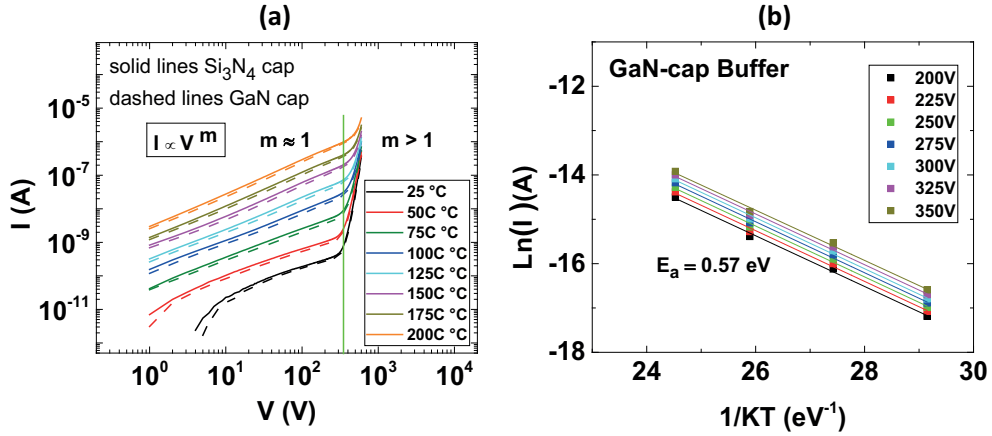

FIGURE 4.40: (a) *I-V* characteristics in log-log scale of the vertical leakage current as a function of temperature in a buffer with Si_3N_4 cap (solid lines) and GaN cap (dashed lines). (b) Activation energy extracted in the high temperature range in GaN cap buffer for different applied bias. A similar value was extracted in the Si_3N_4 cap buffer (not shown).

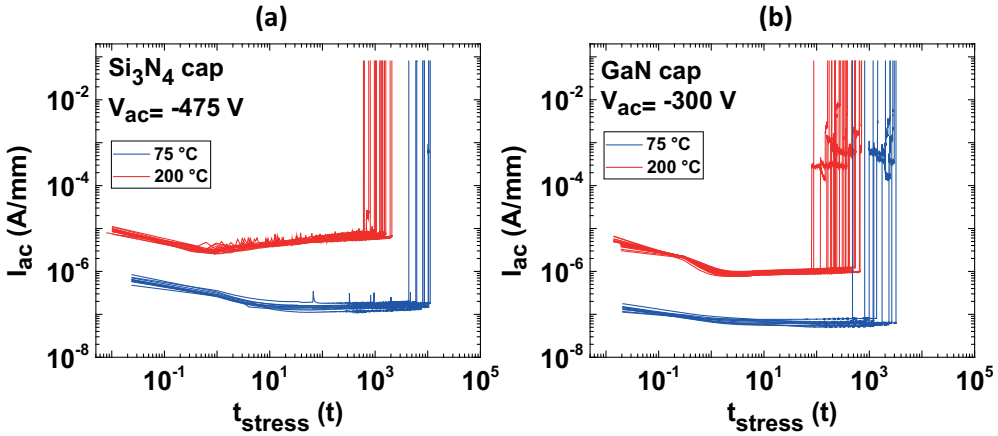

FIGURE 4.41: Results of CVS experiments for one stress condition at two different temperatures in (a) Si_3N_4 and (b) GaN cap devices. The devices-under-test (DUT) have a width of 100 μm.

Accelerated TDDB measurements

Since the leakage degradation has been demonstrated to follow a time-dependent voltage acceleration phenomenon similar to the behavior observed in gate oxide layers [179], TDDB measurements were performed by using a constant voltage stress (CVS) approach and maintaining the substrate floating to capture the diode intrinsic breakdown and reduce the possible impact of the buffer. The time to breakdown is determined when the leakage current variation (ΔI_{ac}) is equal or greater than 1 μA and a wide range of temperatures from 50 °C to 200 °C were used to cause the breakdown in a reasonable amount of time. Figure 4.41 (a) and (b) show the CVS results for one stress condition at medium and elevated temperatures for Si_3N_4 cap and GaN cap devices, respectively. At the beginning of the stress test, the leakage current decreases due to the capture of charges from the anode into the AlGaN barrier [155]. Later, the current increases, possibly because of defect generation at the Schottky edges where high electric field crowding is present or because of donor-defect creation in the GaN buffer [157]. A more visible increase in the leakage current is

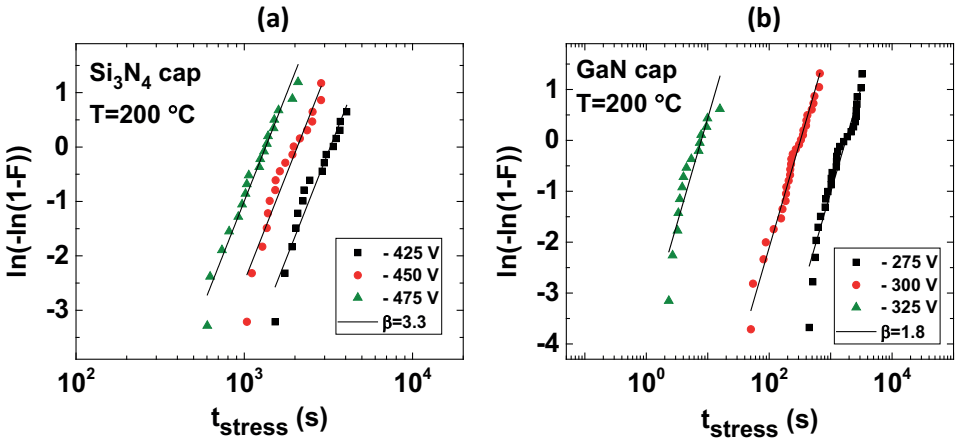

FIGURE 4.42: Weibull plot of the t_{BD}-distribution for different stress conditions at elevated temperature in (a) Si_3N_4 and (b) GaN cap SBDs.

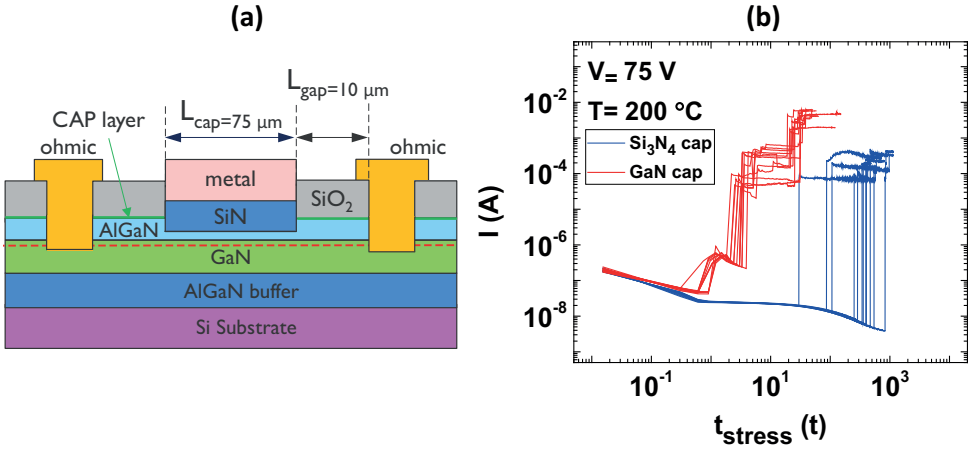

FIGURE 4.43: (a) Simplified schematic of the AlGaN/GaN capacitors. Results of CVS experiments under the same condition in (b) Si_3N_4 and (b) GaN cap capacitors.

observed in Si_3N_4 cap devices, which have been stressed at higher voltages than the GaN cap devices: this is not surprising since more damage is expected under higher voltage-stress conditions.

The time to failure follows a Weibull distribution described by Eq. 4.15. As observed in Figure 4.42, Si_3N_4 cap devices exhibit a higher shape parameter ($\beta = 3.3$), which indicates a narrower t_{BD}-distribution and smaller variability in the intrinsic breakdown behavior than GaN cap devices ($\beta = 1.8$).

For a better understanding of the breakdown at lower voltages, while simultaneously avoiding the influence of the buffer in the measurements and discarding any damage at the Schottky region (which has been reported as a critical zone [164]), TDDB tests at much lower stress voltages of ~75 V were performed in ring capacitors with a schematic structure as shown in Figure 4.43 (a). The results reveal that under the same conditions the field-related breakdown of the dielectric occurs about three orders of magnitude faster in the capacitors with GaN cap compared to Si_3N_4 cap, as depicted in Figure 4.43 (b). Therefore, the cap layer seems to modify the

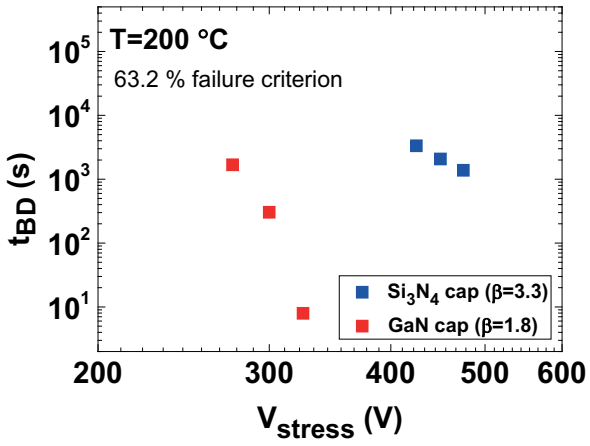

FIGURE 4.44: Time to breakdown 63.2% of the population as function of the stress voltage at elevated temperature (worst case scenario).

electric field within the PEALD-Si_3N_4 dielectric, which ultimately accelerates the breakdown process in GaN cap SBDs even at low voltages.

By plotting the time corresponding to 63.2% failures in the device population (η) as a function of the stress voltage in both devices as shown in Figure 4.44, we observe that the degradation process is clearly field dependent. Si_3N_4 cap devices show a power law dependence even under higher stress conditions, while GaN cap devices exhibit a stronger voltage dependence, but with a turn-over point at a relatively low voltage of 300 V. A turn-over point normally indicates that the breakdown mechanism under stress conditions cannot be related to the breakdown mechanism at operating conditions (overstress) and thus, these conditions cannot be considered for lifetime prediction.

In order to verify the influence of the capping layer on the electric field distribution, additional 2D-TCAD simulations of the diode structure at the normal operating voltage were carried out. Figure 4.45 (a) shows the two cut-lines where the electric field profiles were extracted. As can be seen from Figure 4.45 (b) and (c), higher electric field peaks appear within the SiO_2 passivation layer under the field plate and within the PEALD-Si_3N_4 dielectric at the GET corner. This is the case especially for GaN cap devices, for which the electric field peak inside the GET is simulated to become even higher than at the Schottky contact edge. Therefore, this intensified electric field seems to accelerate the random generation of traps within the dielectric in the MIS structure formed at the edge termination, which creates a percolation path [127], [180]. This ultimately can transform the MIS into a metal/semiconductor (MS) diode structure increasing the leakage current or under high-stress conditions directly causing the device breakdown (hard breakdown) [148].

Apart from the intensified electric field in the GET dielectric, we cannot discard the possibility that the difference in the breakdown between the structures is also influenced by the properties of the cap materials themselves [181]. In this respect, MOCVD-Si_3N_4 has demonstrated an excellent bulk film quality and a breakdown strength around 9.2 MV/cm [148], [166], while MOCVD-GaN is normally reported to have a breakdown strength around 3.5 MV/cm. Since high electric fields appear

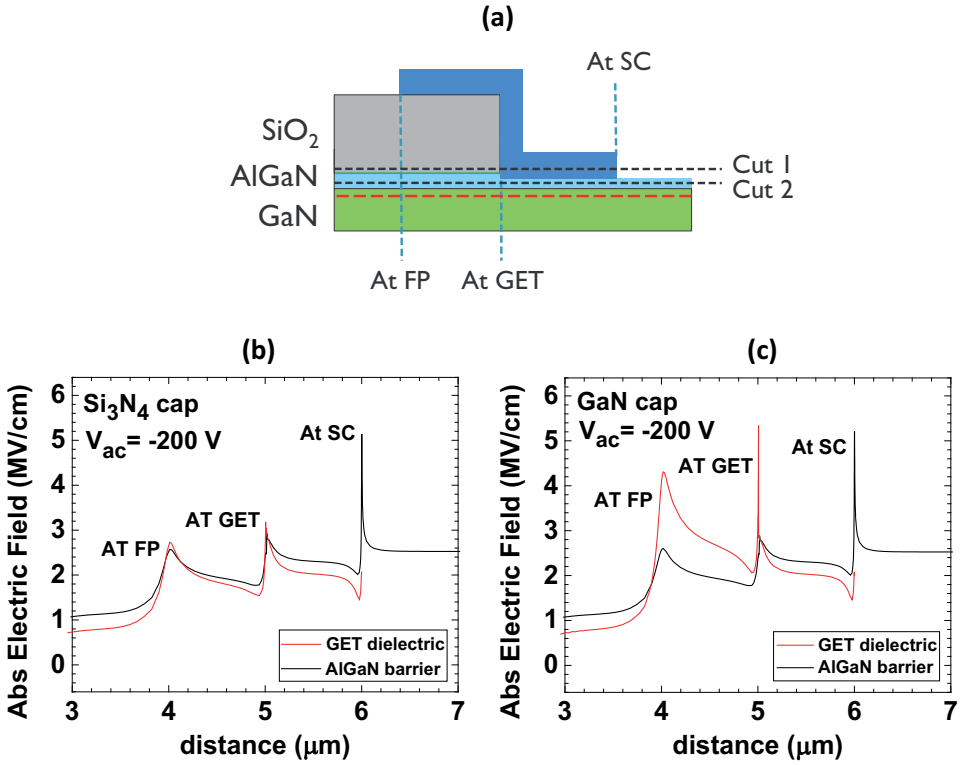

FIGURE 4.45: (a) Schematic of the locations where the electric field is monitored (2 nm and 10 nm above the bottom of the AlGaN barrier and the GET dielectric, respectively). Absolute electric field profile within the GET dielectric (cut 1) and AlGaN barrier (cut 2) at the operating voltage in (b) Si_3N_4 and (c) GaN cap SBDs.

especially at the corner of the GET termination, the GaN cap can also be submitted to these electric fields causing degradation in the GaN material or at its interfaces with other materials such as the SiO_2 passivation layer or the Si_3N_4 GET dielectric. Once the material reaches the maximum dielectric strength, an electrically conductive path and a disruptive discharge can occur through the material.

TDDB measurements at different temperatures (not shown) have the same Weibull slope for both type of devices, indicating that the breakdown mechanisms observed at high and medium temperature range are similar. The activation energy of the time to breakdown is obtained by taking the slopes of the linear fit on a log-lin Arrhenius plot of the data illustrated in Figure 4.46 for two temperature ranges. In fact, the extracted activation energies are in good agreement with the temperature dependence of the leakage current (Figure 4.38 (a) and (b)) described in the previous subsection. The higher the voltage and the temperature, the stronger the influence of the vertical conduction mechanism, while thermionic and field emission mechanisms dominate at medium/low temperatures. Thus, these mechanisms also seem to be responsible for the time-dependent breakdown, but further investigation is still needed to clarify this correlation.

4.3.4 Conclusions

In this section, the influence of the Si_3N_4 and GaN cap layer on the general characteristics and reliability of GET-SBDs has been analyzed and the following results

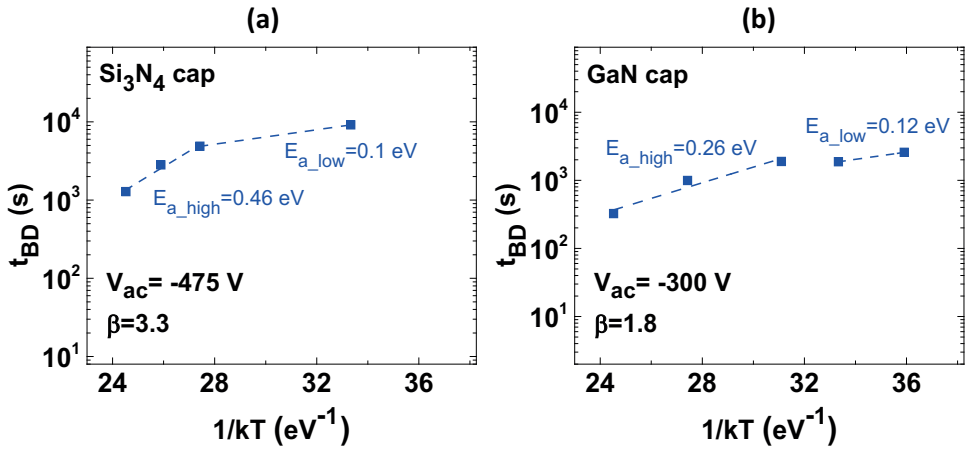

FIGURE 4.46: Arrhenius plot of the t_BD of 63.2% of the population (η) in (a) Si_3N_4 and (c) GaN cap devices.

were obtained. First, higher R_{ON}-dispersion is found in devices with GaN as a cap layer, which is possibly related to trapping at the SiO_2/GaN interface or/and the increase of the fringe capacitance in the access region. Second, the leakage current exhibits activation energies around 0.1 eV and 0.2 eV, which suggests field emission and thermionic-field emission as conduction mechanisms at low/medium temperature range. At high temperature and voltage, additional voltage-dependent activation energy is visible, apparently related to conduction mechanisms within the buffer. Third, TDDB measurements show a narrower t_{BD}-distribution in Si_3N_4 cap ($\beta = 3.3$) compared to GaN cap SBDs ($\beta = 1.8$). Fourth, measurements in ring capacitors and 2D-TCAD simulations confirm higher electric fields within the GET dielectric, especially for GaN cap devices, which ultimately impacts the reliability of these devices already at lower voltages. Finally, the observation of higher V_{BD}, lower R_{ON}-dispersion, longer lifetime and lower t_{BD} variability in the Si_3N_4 cap compared to GaN cap GET-SBD devices, make the former ones more suitable for high-power and high-temperature applications.

4.4 Summary of the chapter

In this chapter, firstly, the methodology to explore time-dependent dielectric breakdown (TDDB) phenomenon has been reviewed. A general background of this degradation mechanism including a description of the percolation model, which better explains the experimental results, and a summary of the proposed theories for the generation of traps have been presented. Moreover, the stress-experiment procedure and the required data analysis to study the TDDB degradation have also been discussed by explaining in detail the t_{BD} extraction, the Weibull plot and its fitting parameters β and η, and the different models to predict the device lifetime. This analysis was then applied to the specific study of GET-SBDs in order to optimize their performance and reliability.

Secondly, the impact of the GET structure, the passivation layer thickness, and a preclean process (sulfuric acid and hydrogen peroxide mixture + ammonia and hydrogen peroxide mixture) before the GET layer deposition on the t_{BD} has been

analyzed by means of the aforementioned methodology. Initially, a reference structure with a single-GET structure, a thick passivation layer and excellent performance under DC, and pulse characterization is submitted to stress. The results show that the time to failure follows a Weibull distribution with high shape parameter values ($\beta \sim 3$ and/or $\beta \sim 5$) related to intrinsic failure mechanisms. The exponential dependence of t_{BD} on the stress voltage suggests a degradation driven by the electric field, while lower thermal activation energies indicate that temperature acts as a weak acceleration factor. A more uniform distribution of the electric field by adding an additional peak (double-GET structure) or with more equilibrated peaks (thin passivation structure) and a more aggressive preclean process before the GET layer deposition improves the breakdown voltage and prolongs the device lifetime.

Finally, the influence of two different cap layers (Si_3N_4 and GaN) on the performance of AlGaN/GaN GET-SBDs has been studied by comparing their general characteristics, breakdown behavior, leakage-current dependency on temperature and t_{BD} under accelerated TDDB measurements. Although, both devices depict similar features in the standard characterization, a higher R_{ON}-dispersion has been observed in GaN cap devices possibly due to charge trapping at the SiO_2/GaN interface or fringe-capacitance increase in the access region. Furthermore, field emission and thermionic-field emission mechanisms seem to be responsible for the conduction at the low/medium temperature range, while conduction mechanisms within the buffer are enhanced under harsh conditions (high temperature and voltage). TDDB measurements in GET-SBDs and capacitors in conjunction with TCAD simulations have demonstrated that the GaN capping layer reduces the t_{BD} even at low-stress voltages, increases the shape parameter (β) of the Weibull plot, and impacts the electric field distribution inside the PEALD-Si_3N_4 GET layer showing increased values which accelerates the degradation process leading to the device breakdown. Consequently, GET-SBDs with a thin Si_3N_4 cap layer are preferable for power applications.

Chapter 5

Conclusion and outlook

GaN-based devices grown on a silicon substrate have been demonstrated as promising candidates for next-generation high-efficiency power switching applications because of their remarkable material properties and the formation of a 2DEG channel at the AlGaN/GaN interface. The presented study has allowed a better understanding of device instabilities caused by high positive gate bias and high reverse voltage in MOSFETs and diodes, respectively. The findings outlined in this dissertation are also helpful in understanding reliability issues related to the insertion of a dielectric layer under the gate/anode area, which will ultimately benefit the future improvement of the robustness of GaN power devices and contribute to the adoption of this technology in a wide range of power electronic applications. This final chapter, thus, briefly summarizes the Ph.D. work by highlighting the key contributions and giving an outlook on the future development of GaN technology.

5.1 Conclusions

Chapter 1 presented an introduction to modern power electronics and its wide range of applications including the role of switching-mode semiconductor devices in power conversion systems. The increasing demand for highly efficient converters and its consequent need for more reliable, robust, and low-cost devices has also been discussed as a preamble for this dissertation. The general properties of different emerging materials in the power market have been compared, and GaN has demonstrated remarkably superior characteristics, which make it a promising candidate. Nevertheless, its spread adoption is still limited by reliability issues that shorten the device lifetime.

In Chapter 2, the GaN properties have been discussed in more detail since the crystal structure and its growth on different substrates are determining in the operation of devices based on this technology. Moreover, it has been explained how the intrinsic spontaneous and piezoelectric polarizations of this material are responsible for the natural formation of a 2DEG channel at the AlGaN/GaN heterojunction allowing high mobility conduction without external dopants as in the case of its Si counterpart. Additionally, the normally-ON characteristic (Depletion mode) of GaN-based devices has been pointed out as a drawback for safe operation of converters. Therefore, some of the approaches to fabricate true normally-OFF (enhanced mode) were described. In particular, the insertion of a dielectric in the gate stack to form a MOS or MIS structure has resulted in a gate leakage reduction, drain current increase and a large gate bias swing. Additionally, in combination with an etching process of the AlGaN layer, it is possible to reduce the barrier thickness below a

critical thickness to deplete the channel, which not only eases the normally-OFF operation but also increases the threshold voltage (V_{th}). The main degradation issues observed in GaN-based devices are also explained with an emphasis on the reliability dependence on the operating state conditions.

Chapter 3 is dedicated to the reliability study of AlGaN/GaN MOS-HEMTs under a high positive gate voltage, which induces a threshold voltage shift known as PBTI. In the first part of this chapter, devices with a gate stack based on SiO_2 are analyzed by using DC characterization and several harsh stress conditions (high voltages and high temperatures). The results showed a slow trapping-process in the oxide and at the SiO_2/GaN interface with a universal decreasing behavior of the trapping rate parameter possibly associated with a relation between the probability of charging traps and the number of available empty traps or due to a charge feedback effect on the oxide field. The recovery has been well described by the superimposition of two exponential functions related to two sets of oxide traps. The slower one was found to be dominant with an average activation energy of 0.93 eV, while the average activation energy of the faster trap was spread in the interval between 0.45 eV and 0.82 eV. In the second part, a single layer of Al_2O_3 and a bilayer formed by AlN/Al_2O_3 have been adopted in the gate stack resulting in a rapid charge trapping. Therefore, pulse measurements characterization has been implemented to characterize the PBTI degradation. The pronounced ΔV_{th} has been attributed to charge trapping in the pre-existing defects with a negligible interface state generation, which follows a saturating log-time model. On the other hand, the recovery data were well adjusted by the empirical universal relaxation model. By combining stress and recovery results, the insertion of an AlN layer has shown to degrade the device reliability since a larger trap density, faster trapping, wider trap energy distribution, and slower charge release have been observed.

Finally, in Chapter 4, a background about the TDDB mechanism has been described by taking into account, the principal purposed models, the test set up and the corresponding data processing. Subsequently, this methodology has been applied to the reliability study of GET-SBDs under high-temperature reverse voltages. Firstly, the influence of the GET architecture (single vs. double), the passivation layer thickness, and the preclean process before the GET layer deposition have been analyzed. In all the cases, the t_{BD} exponentially depends on the stress voltage suggesting that the electric field leads the degradation, while the temperature has a minor impact. A prolonged device lifetime has been observed in double-GET structures, and in devices with a thin passivation layer and a more aggressive preclean treatment based on SPM+APM. TCAD simulations have indicated that this improvement is due to a more uniform distribution of the electric field in critical areas such as the GET corner and beneath the anode field plate. Moreover, it has been demonstrated that the extrinsic failure signature in double-GET devices is related to buffer limitations and once a more robust substrate is used, the Weibull distribution exhibit a slope greater than 1, which indicates intrinsic failures. The influence of the capping layer in GET-SBDs has also been discussed by comparing structures with Si_3N_4 and GaN as capping layers. Although the general characteristics were quite similar, a slightly higher R_{ON}-dispersion in GaN cap devices was observed possibly due to charge trapping at the SiO_2/GaN interface or fringe-capacitance increase in the access region. The low activation energies extracted from leakage current measurements at different temperatures suggest field emission and thermionic-field emission as conduction mechanisms at the low/medium temperature range. On the other hand, additional

voltage-dependent activation energy at high voltage and temperature was found to be intensified when the substrate is grounded even from relatively low voltages (200 V) in GaN cap diodes suggesting the presence of higher electric fields. In order to understand this behavior, TDDB measurements have been performed not only in diodes but also in ring capacitors by using low-stress voltages to discard any impact from the substrate. The data analysis showed a narrower t_{BD}-distribution in Si_3N_4 cap devices compared to GaN cap SBDs. The overall results in combination with TCAD simulations have demonstrated that the GaN cap layer increases the electric field within the GET dielectric, in special, in the GET corner causing the degradation that leads the device breakdown. Therefore, the reliability analysis described in this chapter can be used as a baseline to increase the GET-SBD lifetime by combining the advantages of the double-GET structure, the thin passivation layer, the more aggressive preclean process based on SPM+APM and the *in situ* Si_3N_4 cap layer to further expand the use of GaN-based diodes in high-power and high-temperature applications.

5.2 Outlook

Regarding the PBTI phenomenon analyzed in this thesis, several aspects can still be investigated to deepen the understanding of devices instabilities in GaN MOS/MIS-HEMTs. Among others, these are the most important ones:

- The electrical characterization under high positive gate bias could be extended to advanced gate dielectrics such as HfO_2 or the bilayer gate stack (SiO_x IL + HfO_2) since they have demonstrated PBTI improvements in advanced logic devices due to a decrease of the interface states density and gate dielectric defects.
- It is also important to identify the nature of the defects that cause degradation. Even though the dynamics of the stress and relaxation process have been described, the trap formation process still requires an advanced study. Some approaches used in Si MOSFETs can be adopted in GaN-based transistors such as magnetic resonance techniques or time-dependent defect spectroscopy (TDDS) to better examine the physical and chemical nature of BTI related defects [111].
- Since the pulsed measurement characterization presented in chapter 3 allows accurately capturing fast V_{th} dynamics, it can be used to study the influence of the temperature in the trapping and de-trapping process involved in PBTI. Additionally, this methodology can also be used to perform a statistical study, which has not been included in this thesis due to the lack of sufficient devices with similar physical characteristics and dimensions.
- As future work, it is also very important to purpose specific lifetime models for GaN MOS/MIS-HEMTs by taking into account different degradation phenomena such as BTI, hot carrier injection (HCI), TDDB, among others. Since the conventional Power law and Exponential models, which were adopted from Si-based technology, are still under debate, the development of physical models that describes the aforementioned degradation mechanisms is required to properly estimate the device lifetime and ensure a correct performance over the years.

Starting from the contributions of this Ph.D. work, the recommendations for future research on GaN diodes reliability are the following:

- In previous works [6], [51] and in this dissertation, the implementation of an edge termination in conjunction with the AlGaN barrier recess have demonstrated to effectively improve the diode performance under DC and pulsed characterization. However, a dedicated study about the impact of the barrier recess on the diode reliability under ON- and OFF-state has not been performed yet. By considering that the atomic layer etching (ALE) process can generate defects at the AlGaN surface and cause statistical variation of the barrier thickness in the wafer, long-term stability should be investigated by considering this parameter and its direct implications such as device variability, and instabilities of the barrier height and on-resistance.

- It could be interesting to perform a statistical analysis of the diode degradation under ON-state stress with the improved diodes presented in this work. Although some studies have been already performed on this topic in GET-SBDs [70], none of them have involved a representative number of devices and considered variations of the GET architecture (single vs. double). This analysis can be useful to discard any possible trade-off between the observed improvements under ON- and OFF-state conditions.

- Reverse bias TDDB at different temperatures have also been presented in chapter 4 with relatively low activation energies suggesting that the degradation mechanism is slightly influenced by temperature. However, the linkages between the different device degradation modes are still unclear. Therefore, a deeper analysis of temperature as an accelerator factor is needed not only to clarify the similarities that were founded in activation energies extracted from TDDB measurements and from the temperature-dependent analysis of the leakage current (Subsection 4.3.3) but also to appropriately estimate the device lifetime.

- The exploration of different materials with better bulk properties (poly-AlN, HfO_2, etc.) compared to Si_3N_4 is also recommended for the GET-structure fabrication because reduced defects in this layer can decrease the leakage in presence of high electric fields, and postpone the percolation path formation.

In summary, all the future work suggested in this chapter will be greatly useful to further understand the degradation mechanisms in GaN-based transistors and diodes under all the operation modes (ON-state, SEMI-ON, and OFF-state). The long-term reliability, as well as excellent device performance, are the challenges towards the integration of SBDs with AlGaN/GaN HEMTs. Once this will have achieved, GaN-based devices can easily be adopted in the power market world and research toward real applications will receive more attention.

Scientific Contributions and Awards

Honors and awards

- Best Electron Device paper, Third Ecuador Technical Chapters Meeting, IEEE ETCM, Cuenca 2018.

Journal Articles

- E. Acurio, F. Crupi, N. Ronchi, B. De Jaeger, B. Bakeroot, S. Decoutere, and L. Trojman, "Influence of GaN- and Si_3N_4- passivation layers on the performance of AlGaN/GaN diodes with a gated edge termination", IEEE Trans. Electron Devices, vol. 66, no. 2, pp. 883–889, Feb. 2019.

- E. Acurio, F. Crupi, N. Ronchi, B. De Jaeger, B. Bakeroot, S. Decoutere, and L. Trojman, "Reliability Improvements in AlGaN/GaN Schottky Barrier Diodes With a Gated Edge Termination", IEEE Transactions on Electron Devices, no. 5, pp. 1765–1770, 2018.

- E. Acurio, F. Crupi, P. Magnone, L. Trojman, and F. Iucolano, "Impact of AlN layer sandwiched between the GaN and the Al_2O_3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs", Microelectronic Engineering, pp. 42–47,2017.

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Conference Papers

- E. Acurio, F. Crupi, P. Magnone, L. Trojman, and F. Iucolano, "Impact of AlN layer sandwiched between the GaN and the Al_2O_3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs", 20th Conference on Insulating Films on Semiconductors, INFOS, Postdam 2017.

- E. Acurio, L. Trojman, F. Crupi, and F. Iucolano, N. Ronchi, B. De Jaeger, B. Bakeroot, S. Decoutere, "Reliability in GaN-based devices for power applications". Third Ecuador Technical Chapters Meeting, IEEE ETCM, Cuenca 2018.

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