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# SiGe BiCMOS Building Blocks for 5G Applications

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# Abstract

SiGe BiCMOS semiconductor technology has been increasing its application domain especially for the development of complex microwave monolithically integrated circuits (MMIC) required for modern telecommunication systems. This thesis presents a set of building blocks developed in different SiGe BiCMOS technologies for reconfigurable antenna applications. The developed blocks are oriented to the implementation of electronically scanned phased arrays or of switched beam antenna systems. The red thread that links the different topics is the next generation mobile communication systems, namely 5G systems. However, 5G networks instead of providing specific requirements for each block are employed as an application context that is adopted to provide a real employment scenario for each device proposed in this work.

The thesis is organized as follows. In the first chapter, an overview about development opportunities of 5G technology is illustrated. In the second chapter, a brief introduction in the world of MMIC and SiGe technology has been provided. In the third chapter, beam-forming networks are dealt introducing the design of an 8x8 Butler matrix and a Wilkinson combiner/divider in SiGe BiCMOS technology. In the fourth chapter, a quarter wavelength resonant filter phase shifter is presented. An innovative technique to realize a phase shifter using the peculiarity of the pass-band filters. In the fifth chapter, it is presented a study on metamaterial structures based on Split Ring Resonators integrated with on-chip Coplanar Wave guides. In the last chapter, a FDD technique is illustrated along with the design of a Duplexer in K/Ka-band with High/Low pass filter.

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# 1. Technical characteristics for 5G mobile communications systems

A 7-fold increase of the worldwide mobile traffic is expected between 2016 and 2021. This rate will soon go beyond the capacity of currently available mobile communication networks thus demanding a new high-capacity system which is referred to as 5G [1]. Researchers around the world are exploring possible ideas and technologies for the fifth-generation mobile networks (5G). Many cases of use have been summarized in various white papers and reveal demanding requirements. The possible technologies and ideas under discussion to meet these requirements are very different. There is no doubt that there is a need to improve the understanding of any new air interface at frequencies above existing cellular network technologies, from 6 GHz up to 100 GHz, as well as advanced antenna technologies such as massive MIMO and beam forming.

The current fourth generation for mobile communications already use advanced technology, such as orthogonal frequency division multiplexing (OFDM) or multiple input multiple output (MIMO), in order to achieve spectral efficiency close to theoretical limits in terms of bits per second per Hertz per cell [2]. One possibility to increase capacity per geographic area is to deploy many smaller cells such a femtocells and heterogeneous networks. However, because capacity can only scale linearly with the number of cells, small cells alone will not be able to meet capacity required to accommodate orders of magnitude increases in mobile data traffic. As the mobile data demand grows, the sub-3GHz spectrum is becoming crowded. On the other hand, a vast amount of spectrum in the 3-300GHz range remains underutilized. This portion of spectrum is called millimeter-wave band. Millimeter-wave communications system that can achieve

multi-gigabit data rates at a distance of up to a few kilometers already exist for point-to point communications. However, the electronics component used in this field are too big in size and consume too much power to be applied in mobile communications. In order to ensure good coverage MMB (millimeter-wave mobile broadband) base stations need to be deployed with higher density than macro-cellular base stations. The transmission and reception in an MMB system are based on narrow beams, which suppress the interference from neighboring MMB base stations and extend the range of an MMB link. This allows significant overlap of coverage among neighboring base stations. Unlike cellular systems that partition the geographic area into cells with each cell served by one or a few base stations, the MMB base stations form a grid with a large number of nodes to which an MMB mobile station can attach. For example, with a site-to-site distance of 500m and a range of 1 km for an MMB link, an MMB mobile station can access up to 14MMB base stations on the grid, as shown in Figure 1-1.

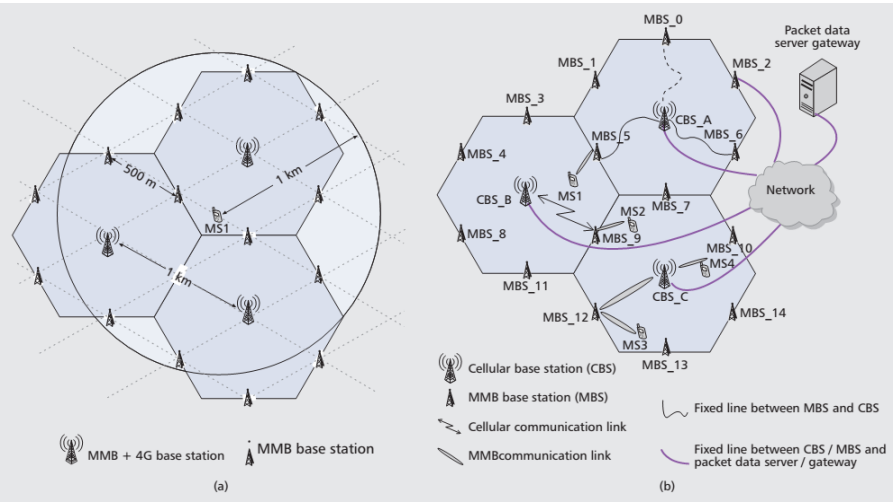



*Figure 1-1 Possible solutions for MMB architecture.*

This possible solution has the advantage to eliminate the problem of poor link quality at the cell edge that is inherent in cellular system and enables high-quality equal grade of service. However, the main disadvantages are related to the cost of

wired network necessary to connect every MMB base station. To avoid the problems related to costs the more attractive solution could be the utilization of some MMB base stations to connect to the backhaul via other MMB base stations.

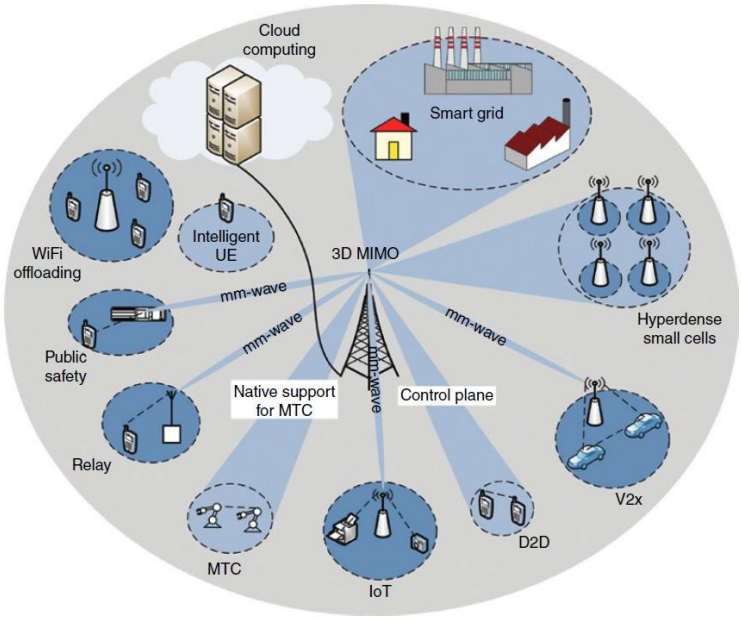



*Figure 1-2 5G system architecture*

As illustrated by Figure 1-2, 5G will be a truly converged system supporting a wide range of applications from mobile voice and multi-Giga-bit-per-second mobile Internet to D2D and V2X (Vehicle-to-X; X stands for either Vehicle (V2V) or Infrastructure (V2I)) communications, as well as native support for MTC and public safety applications [1].

## 1.1 *Fundamentals on 5G*

The 5G is really on the horizon and clearly has a major role in global research and pre-development. Constant demand for higher data rates and faster connections from users require much more wireless network capabilities, especially in high-density areas. The industry expects a 100 times higher data rate per user and a capacity greater than 1000 times, and has defined these goals for the fifth generation mobile network (5G). An example is sports events or concerts, where

many viewers want to share their experience instantly through sharing images or videos. The event itself could also offer additional services to viewers, such as basic information about playing music or replaying to the slower sports sequences.

In addition to the infinite demands for a larger offer, faster data rates at rush hours, greater capacity, better cost efficiency, especially the new Internet Things of Things (IOT), proposes new challenges to face. It is expected that millions of devices will "talk" to each other, including machine-to-machine (M2M), vehicle-to-vehicle (V2V), or general-use x-2-y.

This will require different requirements than those currently faced by 4G systems, which have been optimized to provide access to mobile broadband data. However, not just the number of devices is crucial: high reliability, long battery life (years instead of days) and very short response times (latency) require a further "G" in the future. Reducing energy consumption in cellular networks is another important requirement. This is particularly difficult since peak capacity and speed data must be increased at the same time.

The ongoing research is revealing a series of technological components aimed at achieving ambitious goals, including:

- Millimeter waves: Exploring the higher frequency ranges would allow the use of higher bandwidths, which would lead to higher peak data rates and system capabilities.
- New air interfaces: The LTE based air interface based on OFDM will not be adequate for some cases of use and therefore a certain number of new air interface candidates is being discussed.
- Massive MIMO / Beam forming, active antennas: particularly at higher frequencies, the significant increase in leakage in the propagation path

should be compensated by higher antenna gains. In addition, adaptive beam training algorithms, even on a per-user basis, are needed and can be implemented using active antenna technology.

- Device-to-Device Communications (D2D): An already existing use case to meet public security needs through LTE. Implementing D2D communications could also allow low latency for specific scenarios.
- Network Virtualization (Cloud Based Network): The goal is to run the current dedicated hardware such as virtualized software functionality on general-purpose hardware in the central network. This is extended to the radio network by separating base stations into radio units and baseband units (i.e. fiber-connected) and gathering baseband units to handle a large number of radio units.
- Control of division and user plane and / or decoupling downlink and uplink: the goal is to use heterogeneous networks, making it possible to control all user devices on a macro level, while user data is provided independently by a small cell.
- Light MAC and RRM strategies optimized: Considering the high number of potentially very small cells, radio resource management needs to be optimized. Planning strategies would potentially require stack of slower protocols, which could also be used in uncoordinated scenarios.

It is significant that the European Research Program 5G is called Horizon 2020. It gives an idea of the timeline foreseen for the dissemination of this new technology[3].

# 2. MMIC and SiGe BiCMOS technology

As the frequency of operation of electronic circuits increases, the parasitic impedance plays a major role in the circuit performance. In circuit simulation, these factors are generally neglected. Soldering of the components, leads etc. also contributes to the parasitic effect. Other than performance degradation, circuit repeatability is also lost, as the effect of soldering will not be exactly same for each iteration. To get rid of these effects and to enable higher integration densities, MMIC circuits are used at high frequency.

## 2.1 *Monolithic Microwave Integrated Circuit*

“Monolithic Microwave Integrated Circuit” (MMIC) are integrated circuits (IC) operating at microwave frequencies (300 MHz to 300 GHz) with active and passive components fabricated on one semiconductor substrate. The term monolithic comes from the possibility to realize passive and active structures not in a planar way, but MMICs offer to the designers several metallization layers as it is shown in Figure 2-1.

In this technology, all the elements are grown on a common wafer. The circuit size is small resulting in negligible parasitic. As no soldering is involved, repeatability of circuit is also achieved.

Therefore, MMIC results in low mass-size, less parasitic and repeatable circuits.

Other than active devices, capacitor, inductors and transmission lines are the components mostly involved in any high frequency circuit.

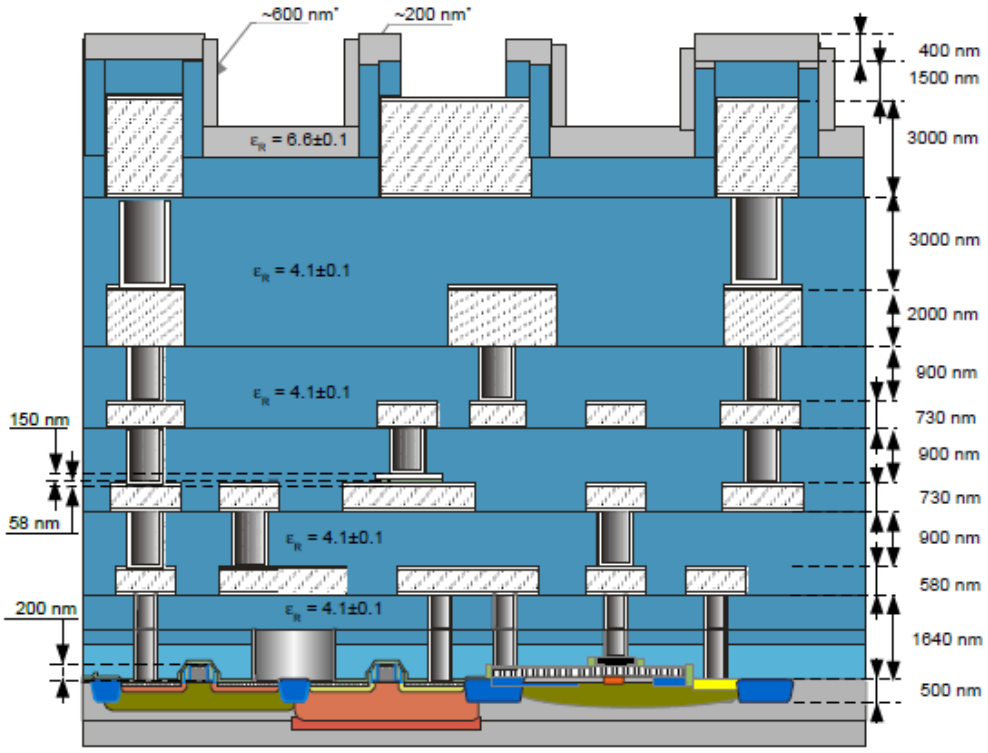



*Figure 2-1 IHP SiGe BiCMOS SG25H3 stack-up with upper part for passive and the bottom part for active device.*

The manufacturing process of the wafers entails forming micrometric or even nanometric features on their surface. Because of this reason, the fabrication process is costly and time consuming. MMIC technology provides the core components for many applications of microwave and telecommunication. There are some advantages of applying MMIC technology that listed below [4]:

- Cheap in large quantities;
- Good reproducibility;
- Small;
- Light;
- Less parasitic;
- Larger bandwidth.

MMICs were originally fabricated using gallium arsenide (GaAs), a III-V compound semiconductor. It has two fundamental advantages over silicon (Si),

the traditional material for IC realization: device (transistor) speed and a semi-insulating substrate. Both factors help with the design of high-frequency circuit functions. However, the speed of Si-based technologies has gradually increased as transistor feature sizes have reduced, and MMICs can now be fabricated in Si technology. The primary advantage of Si technology is its lower fabrication cost compared with GaAs. Silicon wafer diameters are larger (typically 8" or 12" compared with 4" or 6" for GaAs) and the wafer costs are lower, contributing to a less expensive IC.

The advances in silicon transistor performance from 1998 to 2004, for both the MOSFET and the Silicon Germanium (SiGe) HBT processes, coupled with the high integration density of five to seven metal layers, have allowed high performance MMICs to be developed at microwave and even millimeter-wave (mm-wave) frequencies. For the SiGe technology, the transistor maximum (unity gain) frequency $f_T$ in standard commercial runs increased from 40 to50 GHz in 1998 to >200 GHz in 2004. The last ST BICMOS55 has been released with a $f_T$ > 300 GHz.

In order to design MMICs, it is necessary to have precise characterization/ modeling of elements (mainly FETs) and impedance analysis based upon it, circuit design suitable to monolithic integration, and element and device fabrication technology appropriate to microwave frequencies and above.

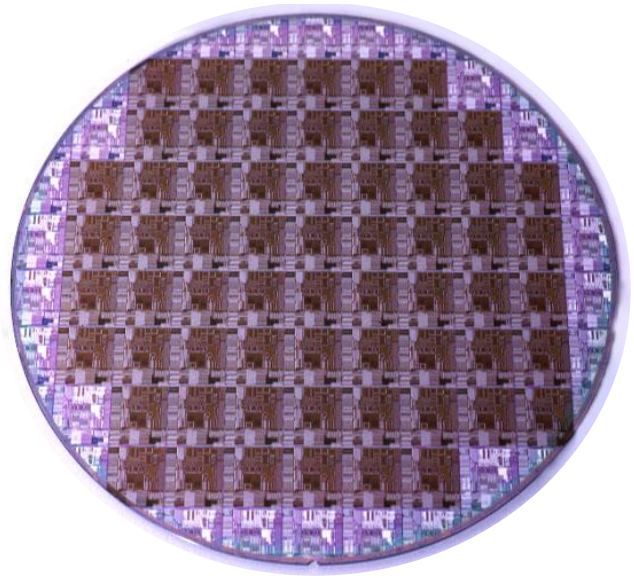


*Figure 2-2 SiGe wafer*

## 2.2 *BiCMOS technology*

BiCMOS is a technology for the production of integrated electronic components. The acronym stands for Bipolar Metal Oxide Semiconductor Semi-conductor and indicates the technology that integrates CMOS and BJT on the same semiconductor chip. The advantage of this process is feasible in the various different technologies. The main advantages are derived directly from the advantages of the two families of devices: if on the one hand the MOS has low power consumption and wide noise margins, on the other the bipolar has a greater ability to drive high loads and high gain. Normally, a CMOS circuit, to obtain a suitable fan-out (ability to drive a load), make use of coupling circuits (buffers). Another important advantage is that the overall capacity of a BiCMOS port is almost equal to one of BJT only, so it is very low. This allows a significant increase in the frequency performance of the BiCMOS when used as a broadband amplifier, or in the same way, a significant increase in the switching frequency when used in logic circuits. For example, by incorporating NMOS, PMOS and NPN BJT devices on the same integrated circuit, BiCMOS process technology

offers the promise of hybrid SRAM solutions that combine the low power and high capacity characteristics of CMOS with the fast access and cycle times of bipolar memories. Another important advantage is the possibility of combining in the same integrated analog and digital electronics, which is useful in realizing system-on-a-chip.

# 3. Antenna array beam forming networks

Nowadays, wireless communication systems are required to process extremely increasing data with high performance, maximize throughput, and small cell etc. Typically, beam forming can be implemented following two main approaches [5].

- **phased array systems** Figure 3-1(a)
- **switched array systems** Figure 3-1(b).

Phased array systems are implemented by placing an attenuator and phase shifter in front of each antenna element [6]. This approach allows to fully control the array pattern, but it results in a complex and costly architecture. On the other hand, in the switched array approach the phase of each radiating element can vary only within a given number of states which can be generated by a Rotman lens such as in [7] or [8], a Blass matrix [9] or a Butler matrix [10].

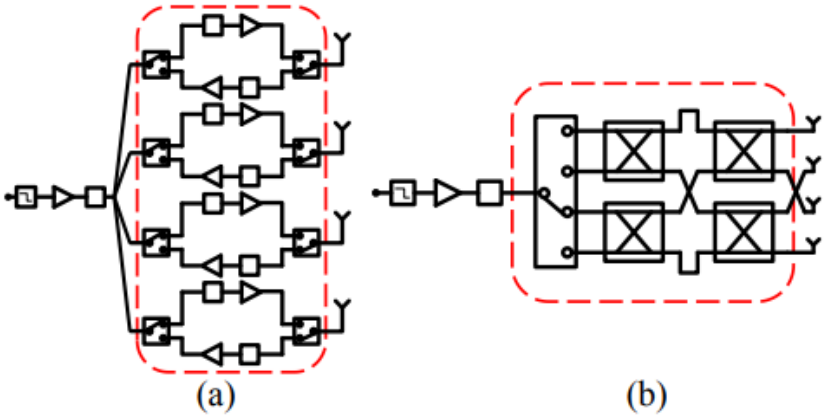



*Figure 3-1 (a) Analog phased array system, (b) switched array system*

Beam formation networks combine signals from multiple antennas into an array that is more directional than each antenna taken individually. These networks are used both in radars and in mobile communications. An example of radar system that uses a linear array of antennas is the one currently used in automotive environments and capable of generating four azimuth beams or, in remote sensing applications, arrays are used by a satellite to route its beam to the Earth.

Beam-forming networks (BFNs) are the signal distribution systems to the different antenna of an array system. Their main function, therefore, is to distribute the signal according to specific amplitude and phase distribution criteria. Depending on their typology, BFNs can generate a single beam or different radiation pattern configurations [11].

Beam forming networks do offer various advantages over phased arrays the main one being related to the use of passive components which reduce losses while providing a great simplification of the architecture which does not require a phase or amplitude control for each element. As a result, also the power consumption is greatly reduced being limited only to the switching and control elements.

## 3.1 *Butler Matrix and a switched array system*

The Butler matrix is configured as a multiport system with N inputs and N outputs. The outputs are the input ports of the antennas while the inputs represent different possible configurations of the radiation pattern of the N radiant elements. Depending on which of the N inputs it activates, the antenna beam is guided in a specific direction in a plane; Butler matrices can be combined on two levels and are used to facilitate 3D scanning.

The first approach with this matrix was described in an article [10] published by the people who named this passive component Jesse Butler and Ralph Lowe in 1961.

The main features of Butler's matrix are:

- N inputs and N outputs, with N usually varying between 4, 8 or 16.
- Inputs are isolated from each other.
- The N outputs are linear with respect to the position, so the output beam is deviated from the main axis.

- None of the inputs provides a very wide beam.
- Increasing the phases between outputs depends on which input is used

By the way, this is a reciprocal passive network, so it works in the same way both when it transmits energy and when it receives it.

Figure 3-2 shows a block diagram of a typical 4x4 Butler matrix. It usually consists of $2^n$ inputs and $2^n$ outputs. Therefore, $\frac{N}{2}\log_2 N$ hybrid couplers are needed, where $N = 2^n$ is the number of input/output. The number of delay lines can vary; in the case of the 4x4 matrix there are 2 phase delays that will provide a shift of 45° of signal. Phase delay of 22.5 ° (x2), 45 ° (x4) and 67.5 ° (x2) are required for an 8x8 matrix.

Outputs are the Fourier transform of inputs and the circuit diagram of a Butler matrix is the same as the FFT (Fast Fourier Transform).

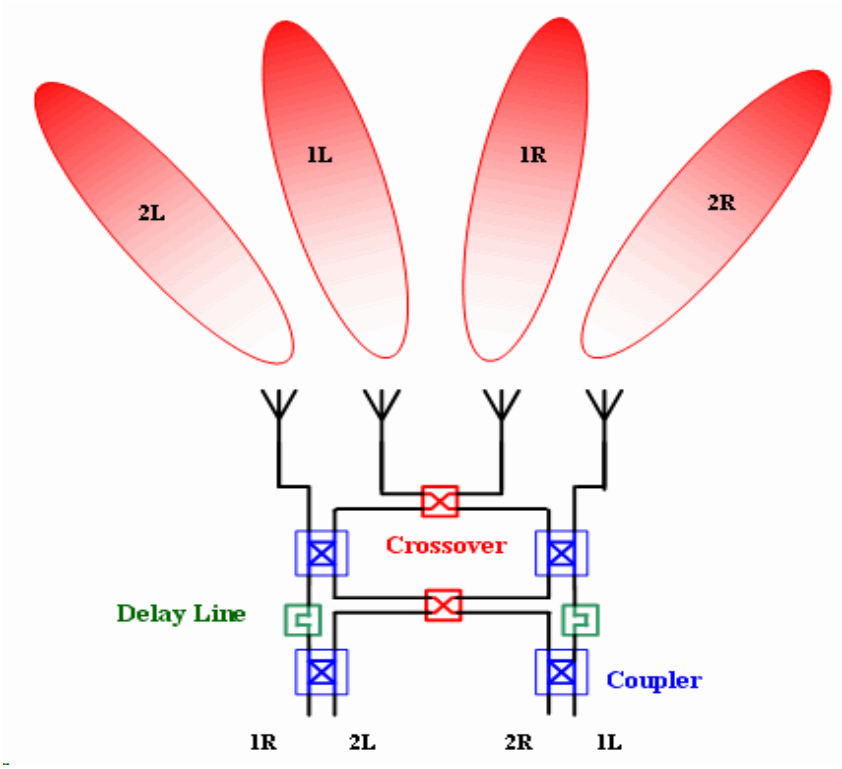



*Figure 3-2 Block diagram of a 4x4 Butler matrix*

If the Butler matrix is connected to an array of antennas, the array will perform its purpose as a beam former and the array will have a uniform distribution of amplitude and a constant phase difference between adjacent elements:

$$\exp(-j\ k\ n\ d_x\ u_i)$$

with $u_i = \left(\frac{\lambda}{N}\ d_x\right) * i$ where $i = \pm\left(\frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \ldots\right)$ if N is even and $i = \pm(1,2,3, \ldots)$ if N is odd.

The generated radiation patterns are N different beams having different angular directions and covering an angular field of 180 °, see Figure 3-3. The direction of the beams depends on which input is used to introduce the signal while the scanning range depends also on the spacing between the array elements. The phase difference between the radiating elements for a Butler matrix with N elements is given by:

$$\Psi_n = \frac{2\ \pi\ d}{\lambda}\cos\alpha = \pm\frac{2\ p-1}{N}\ x\ 180°$$

where the phase difference, $\Psi_n$, it's plus or minus depending on whether the beam is to the right or left respectively relative to the frontal direction. Since the equation depends on $\lambda$ the beam angles $u$ vary with frequency. The Butler matrix, therefore, forms beams whose width depends on frequency. The series of beams generated will be tight at high frequencies and wider at low frequencies [12]

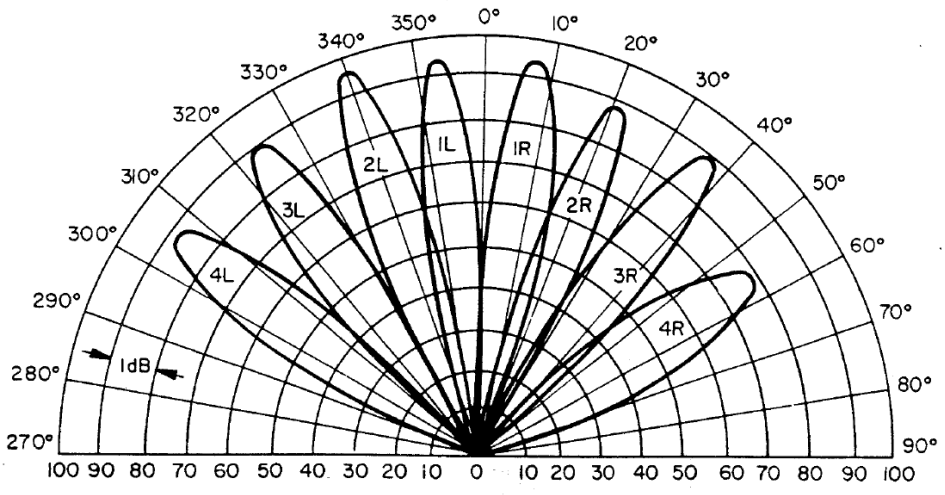



*Figure 3-3 Simultaneous radiation patterns of phased array connected to an 8x8 Butler matrix.*

## 3.2 *Butler Matrix: state of the art*

In the literature, there are several techniques of realization of Butler matrices. Among the various types of designs and realizations in this paragraph will be some sample examples of Butler made on-chip.

In [13] a 24-GHz 4-way Butler Matrix MMIC in 0.18-µm CMOS technology is presented. The multi-layer structure of CMOS process is utilized to monolithically realize the bulky Butler matrix on silicon substrate (Figure 3-4). Particularly, the multi-layer bifilar transformer is introduced to miniaturize the circuit and reduce the signal loss. The implemented CMOS Butler matrix MMIC only occupies a chip area of 0.41 $mm^2$ (excluding I/O pads). The experimental results show that insertion losses are 2.2±0.6 dB from 23 to 25 GHz and the phase errors are within 6°. Therefore, by connecting this Butler matrix to a linear array antenna, four orthogonal beams, pointing to -49°, -15°, 15°, and 49°, respectively, are generated within 0.3° error.

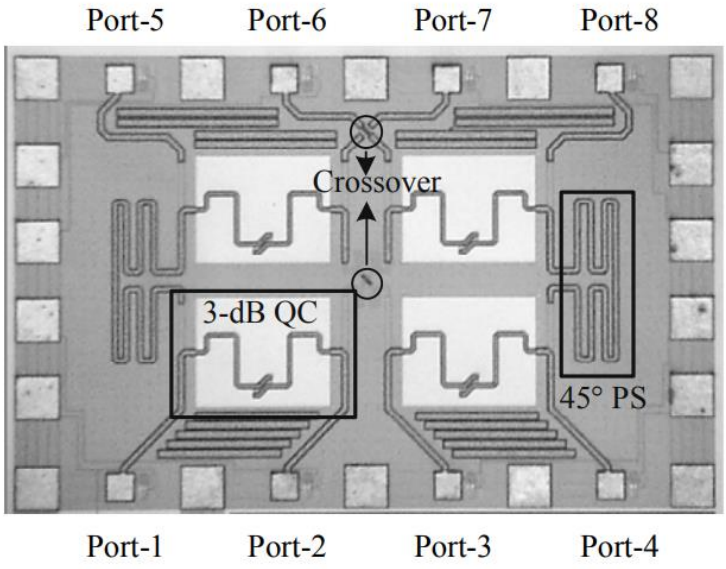



*Figure 3-4 Die photograph of the 4-way CMOS Butler matrix [13]*

In [7] and [14] A compact V-band 4x4 Butler matrix, using 0.35 µm SiGe bipolar process, is proposed. This design exhibits an average insertion loss of 3 dB with amplitude variation less than 1.5 dB and an average phase imbalance of less than 10° from 55 GHz to 65 GHz. The chip area is only 0.5x0.9 $mm^2$ including all pads. The SiGe Butler matrix is an excellent candidate for MIMO systems and applied in high data-rate communications.

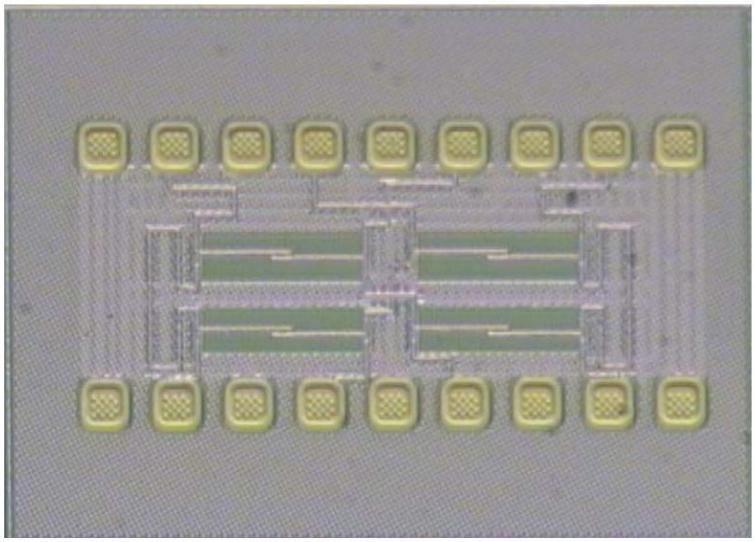


*Figure 3-5 Microphotograph of the proposed Butler matrix in [14]*

In [15] a novel design of monolithic 2.5-GHz 4 4 Butler matrix in 0.18- m CMOS technology in proposed. To achieve a full integration of smart antenna system monolithically, the proposed Butler matrix is designed with the phase-compensated transformer-based quadrature couplers and reflection-type phase shifters. The measurements show an accurate phase distribution of $45 \pm 3°, 135 \pm 4°, -45 \pm 3°$ *and* $-135 \pm 4°$ with amplitude imbalance less than 1.5 dB. The antenna beamforming capability is also demonstrated by integrating the Butler matrix with a 1x4 monopole antenna array. The generated beams point towards -45°, -15°, 15°, and 45°, respectively, with less than 1 error, which agree very well with the predictions. This Butler matrix consumes no dc power and occupies the chip area of 1.36x1.47 $mm^2$.

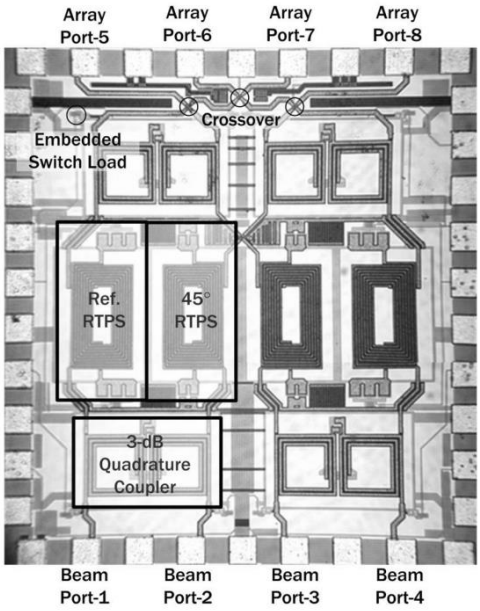



*Figure 3-6 Die photograph of the 4x4 CMOS Butler matrix presented in [15]*

In [16] and [17] are presented a two miniature 11-13GHz and 5–6-GHz 8x8 Butler matrix in a 0.13- m CMOS implementation. The 8x8 design results in an insertion loss of 3.5 dB at 5.5 GHz and no power consumption. The chip areas are respectively 0.95x0.65 $mm^2$ and 2.5x1.9 $mm^2$ including all pads. The 8x8 matrix presented in [17] is mounted on a Teflon board with eight antennas, and the

measured patterns agree well with theory and show an isolation of 12 dB at 5–6 GHz.

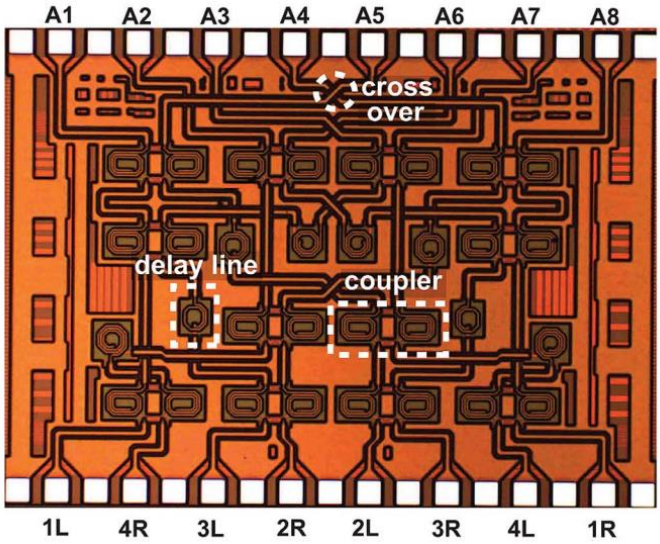



*Figure 3-7 Microphotograph of the 8x8 Butler matrix [13]*

## 3.3 *Design of an 8x8 BiCMOS Butler Matrix*

The ideal block diagram of the designed Butler matrix is shown in Figure 3-8.

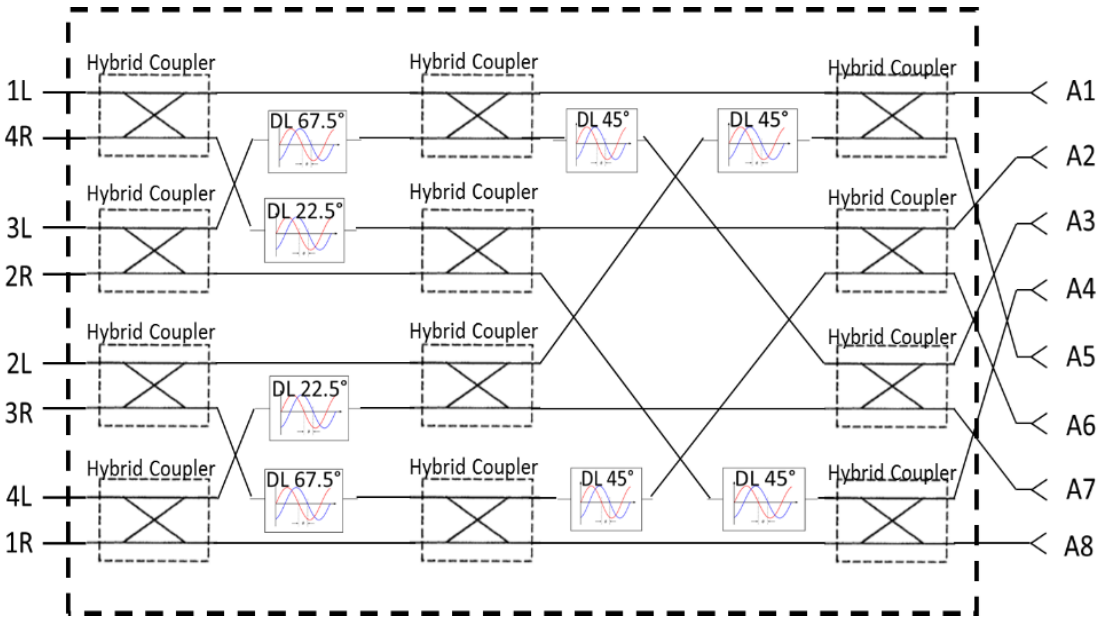



*Figure 3-8 Block diagram of a 8x8 Butler matrix*

The designed Butler matrix is a 16-port component, where 8 ports are used to feed an array of 8 antennas. Depending on the port being fed, the array is excited with different phase distributions and depending on how phases are deployed,

the direction of the main beam varies between -61 and +61 degrees. A summary of the output phase distribution and the associated beam directions are given in Table 3-1.

| | *Beam Ports* | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ***Ant. Port*** | **1L** | **4R** | **3L** | **2R** | **2L** | **3R** | **4L** | **1R** |
| **A1** | 90 | -180 | 157.5 | -112.5 | 135 | -135 | 157.5 | -112.5 |
| **A2** | 112.5 | 22.5 | -90 | -180 | -157.5 | 112.5 | -45 | -135 |
| **A3** | 135 | -135 | 22.5 | 112.5 | -90 | 0 | 112.5 | -157.5 |
| **A4** | 157.5 | 67.5 | 135 | 45 | -22.5 | -112.5 | -90 | -180 |
| **A5** | -180 | -90 | -112.5 | -22.5 | 45 | 135 | 67.5 | 157.5 |
| **A6** | -157.5 | 112.5 | 0 | -90 | 112.5 | 22.5 | -135 | 135 |
| **A7** | -135 | -45 | 112.5 | -157.5 | -180 | -90 | 22.5 | 112.5 |
| **A8** | -112.5 | 157.5 | -135 | 135 | -112.5 | 157.5 | -180 | 90 |
| **ΔΦ** | 22.5 | -157.5 | 112.5 | -67.5 | 67.5 | -112.5 | 157.5 | -22.5 |
| **Beam Angle** | -7 | +61 | -39 | +22 | -22 | +39 | -61 | +7 |

*All in degrees

*Table 3-1 Phase distribution of an 8x8 Butler matrix*

In this research study, an innovative design of an on-chip 8x8 Butler matrix implemented using a BiCMOS process.

### 3.3.1 Hybrid coupler: theory and different topologies evaluation

The most important component of a Butler matrix is the quadrature hybrid coupler. Hybrids are 3dB directional couplers with a phase difference of 90° to the outputs of through and coupled branches. This component is the one that takes up more area on the chip. For this reason, specific attention was devoted to the reduction of the size occupied by this sub-block.

An ideal transformer contains 3 main components and Figure 3-9 shown the ideal circuit that represent it.

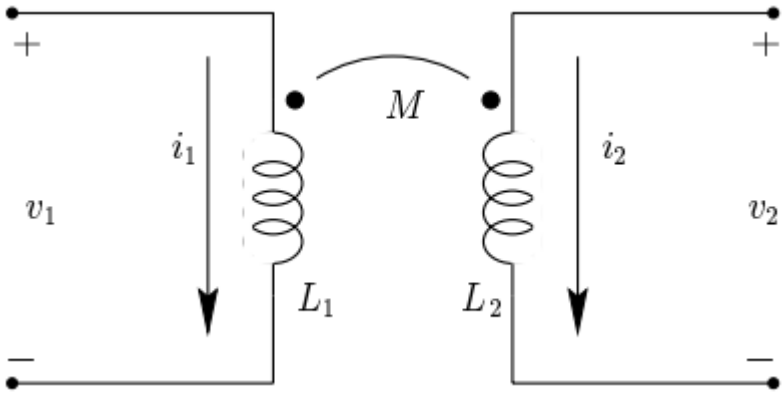



*Figure 3-9 Ideal transformer*

$L_1$ and $L_2$ represents the self-inductance of the primary and secondary coil while M represents the mutual inductance in between. The terminal voltages and currents of an ideal transformer are specified by the following equations [18].

$$v_1 = L_1 \frac{\partial i_1}{\partial t} + M \frac{\partial i_2}{\partial t}$$

$$v_2 = L_2 \frac{\partial i_2}{\partial t} + M \frac{\partial i_1}{\partial t}$$

The mutual inductance, M, is related to the self-inductances, $L_1$ and $L_2$, by the mutual coupling coefficient, *k:*

$$k = \frac{M}{\sqrt{L_1 L_2}}$$

As the transformer is a passive device the value of $k$ is $\leq 1$. k = 1 means ideal transformer but typical value of on-chip transformers exhibit $k$ values between 0.3-0-9.

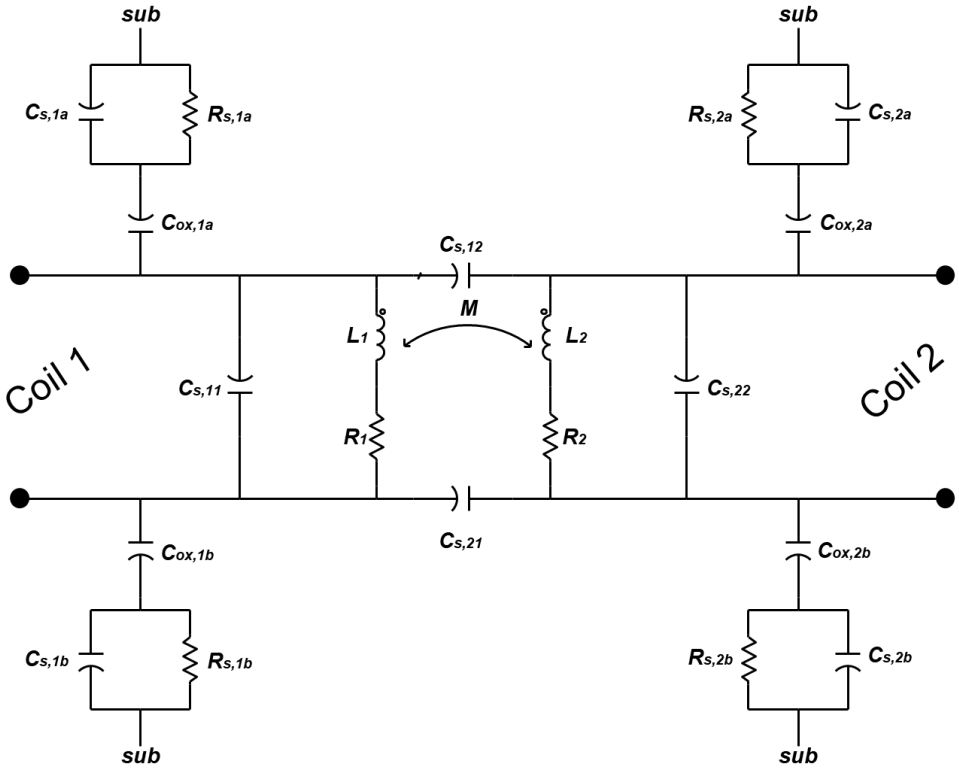



*Figure 3-10 Non-ideal transformer: physical model*

In Figure 3-10, parasitic resistances and capacitances present in the non-ideal transformer are shown. Resistance $R_1$ and $R_2$ model the series resistance of the two coils. The spiral-to-substrate oxide capacitances ($C_{ox,1a}$ etc.) and the terminal-to-terminal oxide capacitances ($C_{s,ij}$ with $i,j$ = 1..2) and the resistive and capacitive losses to the substrate ($R_{si}$ and $C_{si}$). The self/mutual inductance and series resistance are independent of the configuration of the transformer.

In literature, mainly 3 types of monolithic transformers can be found:

1. Tapped Transformers;
2. Stacked Transformers;
3. Interleaved Transformers.

The first one is depicted in Figure 3-11 is the best suited for three-terminal applications due to the asymmetry it permits a variety of tapping ratios to be realized.

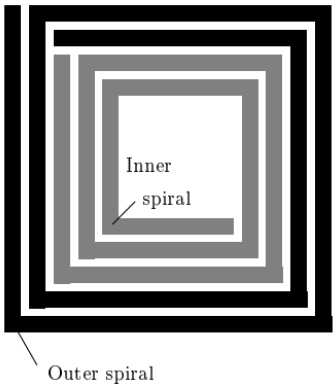



*Figure 3-11 Tapped transformers*

The stacked transformer (Figure 3-12) uses multiple layers and thanks to the vertical and lateral coupling provide the best area efficiency, the highest self-inductance and highest coupling (k is typical around 0.9). The main disadvantage of this transformer is the high terminal-to-terminal capacitance that cause a low self-resonance.

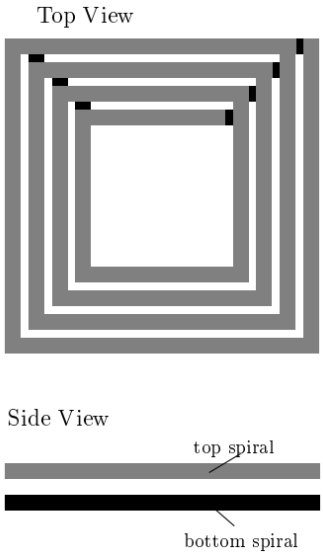



*Figure 3-12 Stacked transformer*

The interleaved transformer is suitable for four-terminal application that demand symmetry. The interleaving of the two inductances permit moderate coupling ($k$=0.7) to be achieved at the cost of reduced self-inductance. This coupling may be increased at the cost of higher series resistance by reducing the turn width and spacing.

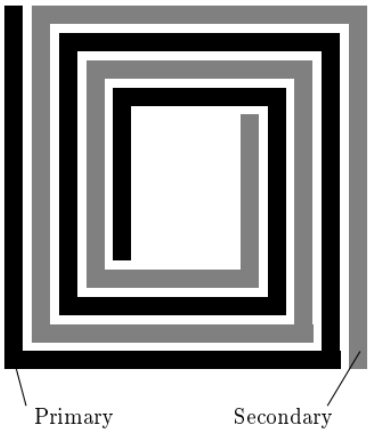



*Figure 3-13 Interleaved transformer*

Different layouts are available in the state of art and the aim is to maximize the coupling between coils. The solution introduced in this work is based on the latter type of transformer because although the staked transformer allows higher coupling factors, but coils have different electrical parameters because they are built with different metal layers. Interleaved structures provide full symmetry between two coils but in the other side poor magnetic coupling. In a first design approach, it is implemented using the lumped element equivalent network shown in Figure 3-14(a). This simplified model fits well with the interleaved transformer.

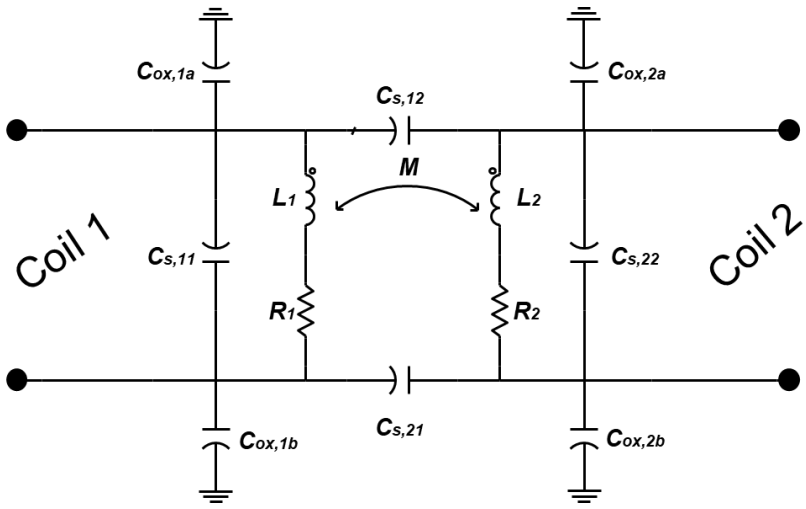



*Figure 3-14 Quadrature coupler equivalent circuit*

The following equations are used to model the transformer, and this is how geometrical parameters are related with the model:

$$L = \frac{\mu\, n^2\, d_{avg}}{2}\ \left[ln\left(\frac{2.46}{\rho}\right) + 0.2\,\rho\right]$$

L is the inductance value of the two coils that are identical where $\rho = \frac{(D_{out}-D_{in})}{(D_{in}+D_{out})}$ is the fill factor and $d_{avg} = 0.5\,(D_{out} - D_{in})$ is the average diameter.

$$R_{1,2} = R_{DC_{1,2}} + \left(1 + 0.1\sqrt{f} + 0.002\,f^2\right)$$

$R_{DC_{1,2}}$ and $R_{1,2}$ are the dc and ac series resistances of the coils ($R_1$ and $R_2$ respectively) and f is the frequency expressed in GHz.

$$C_{OX} = A\,\frac{\varepsilon_{OX}}{t_{OX}} + P\,C_s$$

The value of $C_{ox}$ (that actually takes into account the substrate effect) arises from both area and perimeter effects so $A$ is the area of the inductor, $P$ is the perimeter and Cs is the unit-length specific capacitance. $C_s$, can be calculated with the same formula where $t_{ox}$ and $C_{SP}$ are the thickness and capacitance-per-unit-length between the two coils, between spirals and underpass.

$$k = x_0\ n^{x_1}\ W^{x_2}\ D_{out}^{x_3}$$

In the equivalent circuit, that has been used to model the transformer, each branch of the coils is magnetically coupled through the coefficient $k$. The dependency of $k$ with geometrical parameters are reported in the equation above. In particularm $x_0, x_1, x_2$ and $x_3$ are coefficients determined by measured data. Their values were set to 0.46, 0.006, 0.003 and 0.1 respectively [19].

### 3.3.2 Hybrid coupler design

For the case at hand, the port impedance, $Z_0$, is equal to 50 Ohm, the center band frequency, $f$, is 24-GHz. As it can be observed looking at the equivalent circuit model, the key feature in this schematic is that, due to its symmetry, each port of the four available may be used as an input port.

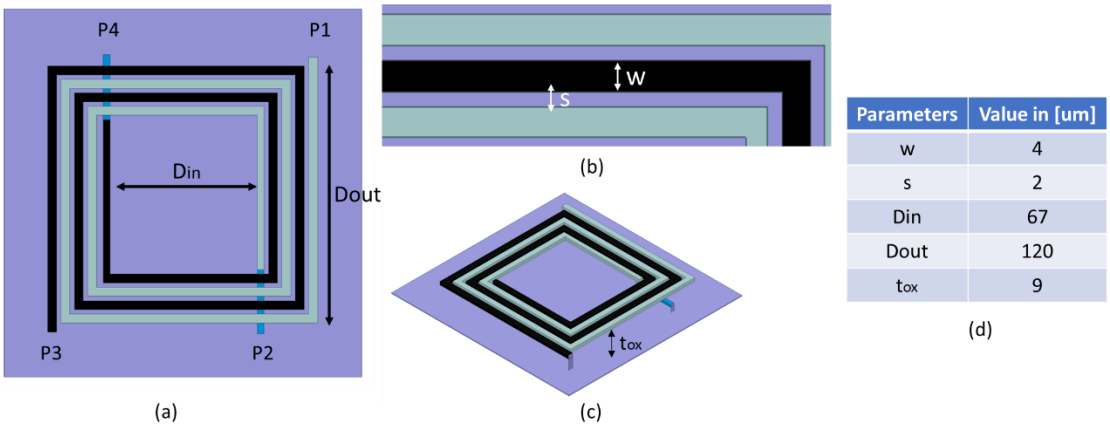
In the case at the hand, it has been decided to start with a simple model and put more effort in the optimization in the layout level.

The technology used in this design is ST BiCMOS 9MW technology. This technology is a 0.13 um process with $f_T = 230\ GHz$ and $f_{max} = 250\ GHz$. The BiCMOS9MW process includes 6 metallization layers. The lower metal layers are identified as M1-M3 which are 0.26-0.35um thick. The topmost metal layers are 3um thick and they are referred to as M5 and M6. In Figure 3-15 the BEOL (back and of line) of the process is shown. This technology, thanks to the 6 metallization layers, results suitable for designing the Butler matrix that, as has been already discussed in previous paragraph, requires several interconnections lines, capacitors and inductors.


*Figure 3-15 ST BiCMOS9MW BEOL Stack-up*

The layout of the quadrature hybrid was implemented using an innovative approach based on a monolithic transformer shown in Figure 3-16. The coupler consists of two rectangular inductors intertwined one inside the other placed on metal level metal M6. The thickest metal layer has been chosen for three main reason.

1) The thick metal layer M6 provides lower electrical resistance thus producing less losses.
2) This layer provides a good side-coupling between the coils (corresponding to the capacitor $C_{s,21}$ in Figure 3-14) due to the thickness of the layer.
3) The capacitors $C_{ox}$ in Figure 3-14 are one of the key parameters that govern the frequency response of the quadrature hybrid. As much as we increase the distance between the coil and the ground place (M1) we reduce these capacitances. It thus results that the capacitance that has been generated between the coil and the ground plane allows setting the width of the coils and the inner diameter very close to the minimum granted to the technology. In other words: a more compact design has been obtained using the top-most metal layer.




| Parameters | Value in [um] |
|---|---|
| w | 4 |
| s | 2 |
| Din | 67 |
| Dout | 120 |
| tox | 9 |

*Figure 3-16 Designed interleaved transformer: (a) Top view (b) Top view (zoom) (c) side view (d) table with the values geometrical parameters.*

M1 has been used as ground layer. The benefit of this choice is that having a metal ground in M1 reduce the losses of the substrate. The main disadvantage is that as the capacitors mentioned in the circuit model as $C_{ox}$ increase, it reduces the self-resonance of the inductor (that directly affect the self-resonance of the coupler). The disadvantage by the way is negligible as the working frequency of the circuit is far from the self-resonance. Better results in terms of Q-factor could be

achieved if a Pattern Ground Shield (PGS) would have been used instead of a flat metal ground (it has been inserted in the list of the possible future works).

This hybrid is based on an inductive coupling effect like conventional directional hybrids implemented using coupled lines. It consists of a pair of coupled transmission lines of electrical length equal to θ having characteristic impedances in the configuration even-and-odd respectively equal to $Z_{0e}$ and $Z_{oo}$ [20]. If the impedances of the odd and even mode are designed satisfying

$$Z_0 = \sqrt{(Z_{0e} \cdot Z_{0o})}$$

then all the impedances of the device ports would be matched to $Z_0$ at the design frequency provided the electrical length is an odd multiple of a quarter of a wavelength.

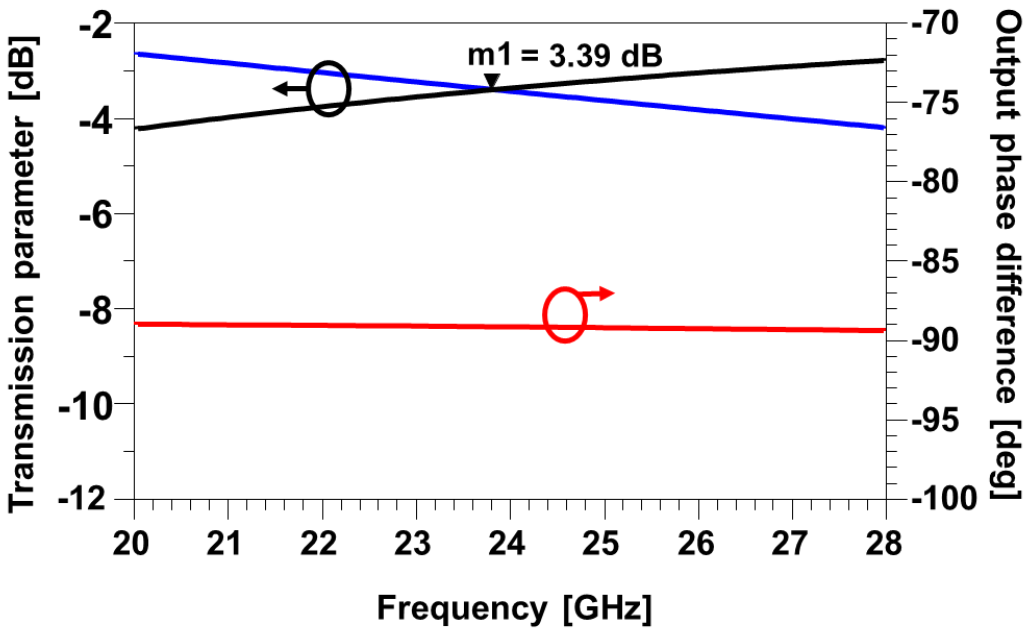



*Figure 3-17 Simulated transmission parameter and output phase deviation of the quadrature hybrid*

The results of the S-Parameter plotted versus frequency in Figure 3-17 are obtained with a full wave simulation performed using a commercial finite element method solver for electromagnetic structures (HFSS, ANSYS). This plot show good results in terms of both transmission parameter and output phase difference

at central frequency and for a wide bandwidth. In particular, it can be noticed that the circuit has been designed to operate at the frequency of 24 GHz not in the classical "U-shape" but in the range where the direct and coupled ports have a positive and negative slope respectively (see the cross in the Figure 3-17). The main advantages of this approach are that it introduces less losses (only 0.39 dB) than the classical solution (sacrificing a bit the bandwidth) and in the same time we obtain an almost flat 90° output phase difference for an ultra-wide frequency range. In order to reduce the chip area occupied by the quadrature coupler, the layout topology was optimized by increasing the circuit density and by evaluating mutual coupling effects through a full-wave [21] simulation of the whole structure. The chip area occupied by the quadrature hybrid is equal to 120x120 $\mu m^2$.

### 3.3.3 Phase delay line

As it is shown in the block diagram of Figure 3-8, three different phase delay blocks are required for the implementation of the 8x8 Butler matrix. In particular, 22.5°, 45° and 67.5° fixed delay lines need to be laid out in the circuit. In this work, phase delay lines were implemented using a transmission line π-model implemented through lumped elements.

| Delay line | Inductor [pH] | Capacitor [fF] | Size [$um^2$] |
|---|---|---|---|
| 22.5 ° | 135 | 20.73 | 45 |
| 45° | 230 | 50.5 | 50 |
| 67.5° | 300 | 85 | 56 |

*Table 3-2 Inductance and capacitance needed for phase delay*

The π-network consists of two parallel capacitors and a series inductor. The inductor was designed using a rectangular geometry placed on the M6 level.

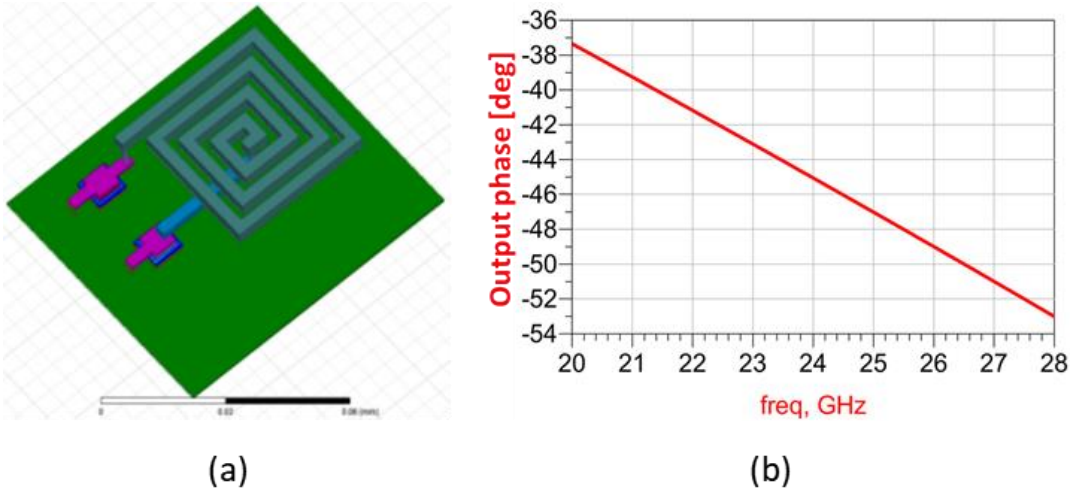



*Figure 3-18 45° Delay line: (a) layout (b) Output phase.*

Table 3-2 shows both inductance and capacitor values required to implement the circuit where it is shown also the overall size of each delay line. An example of the delay line model is shown in Figure 3-18a along with the simulated phase of the transmitted signal Figure 3-18b.

### 3.3.4 Crossover

Crossovers have been implemented taking advantage of the multilayer stack-up of the BiCMOS technology at hand. In particular, the two crossing lines were located on M6 and M4 metal layers while M1 layer also in this case act as a ground plane. The simulated isolation of the two crossing lines, shown in Figure 3-19, shows an isolation greater than 40 dB over the whole band.

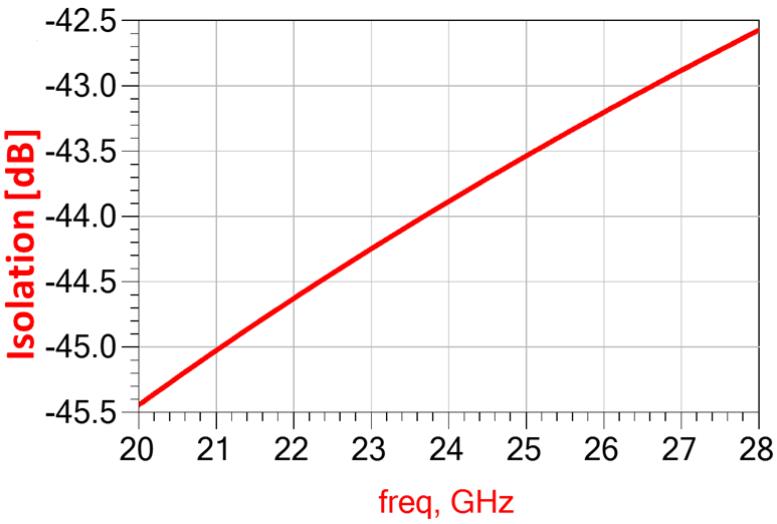



*Figure 3-19 Crossover isolation*

### 3.3.5 Simulation results

The entire layout, with the exclusion of the measuring pads, is equal to 714 um x 650 um. As it can be observed in Figure 3-20 and Figure 3-21, the configuration proposed in this work shows an excellent input matching bandwidth for all ports. Indeed, the reflection coefficient remains below 20 dB in the whole simulation range. Furthermore, the insertion losses from the input to all the output ports remain within the 3 dB range for a 10% bandwidth.

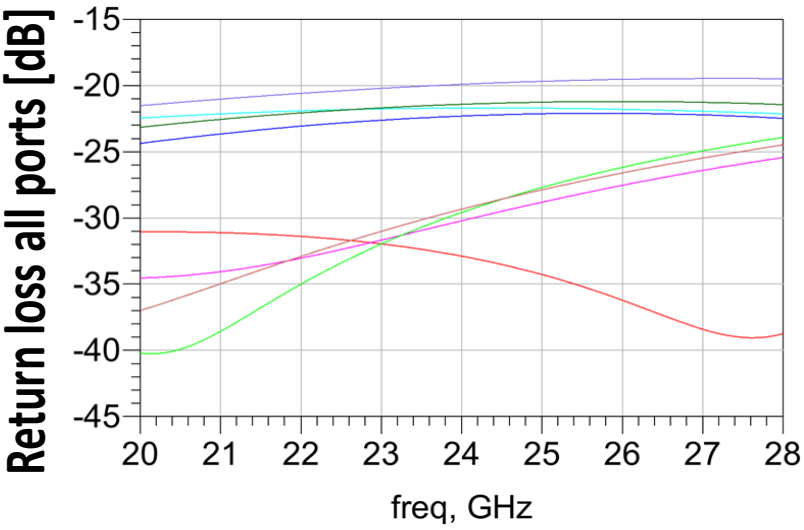



*Figure 3-20 Simulated input return loss of Butler matrix*

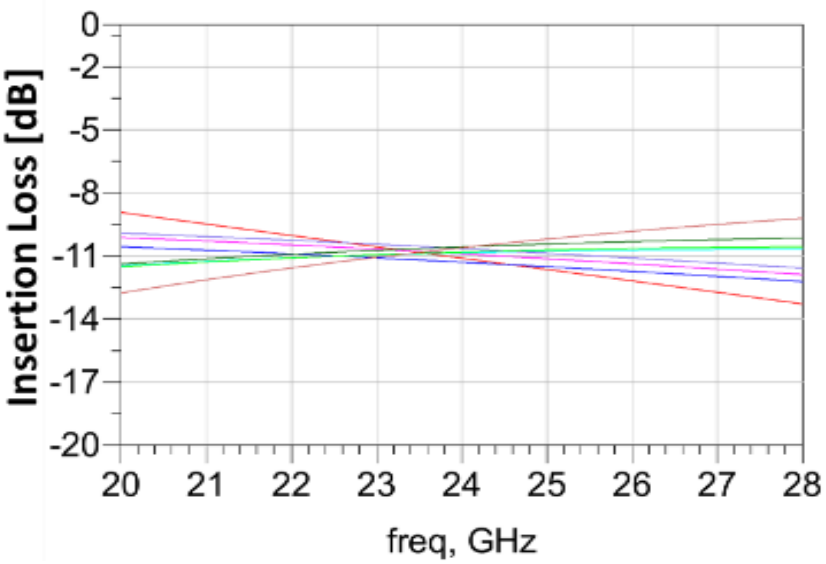



*Figure 3-21 Simulated input insertion loss of Butler matrix*

The output phases are in line with the ideal values and they were evaluated by analyzing the array factors obtained for different configurations of the Butler matrix. As it can be observed in Figure 3-23b, the simulated Butler matrix of Figure 3-22 generates 8 beams in the range from -60° to 60° as expected thanks to the output transmission phase shown in Figure 3-23(a).

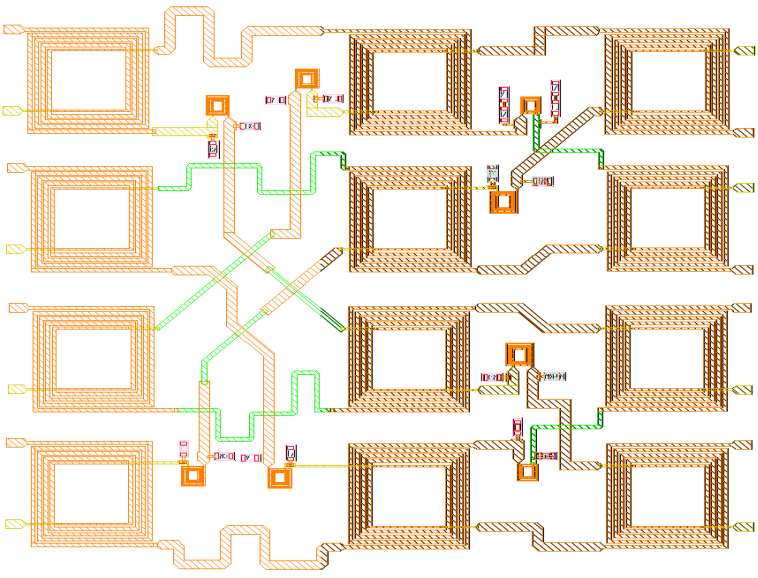


*Figure 3-22 Final layout of the 8x8 Butler matrix*

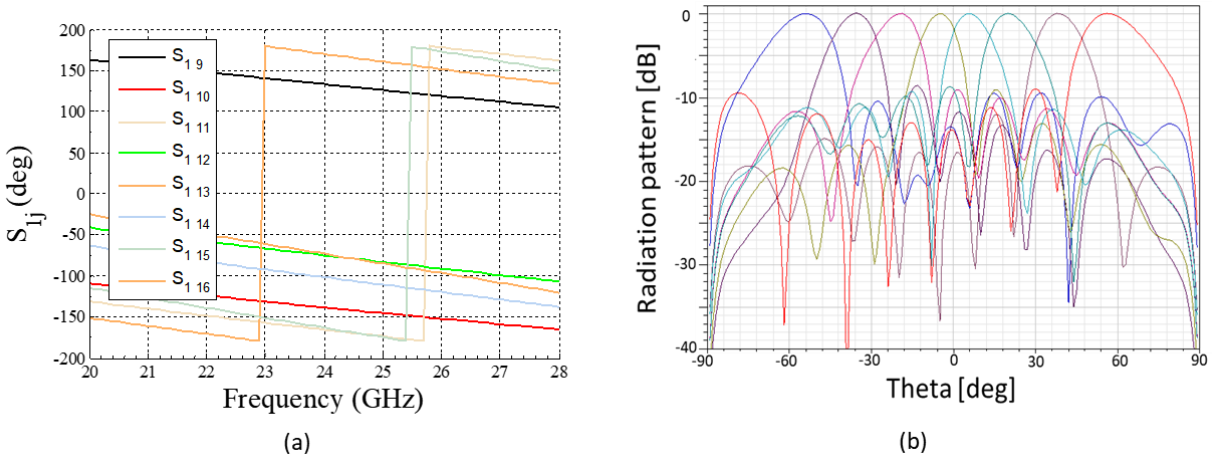



*Figure 3-23 Transmission Phase (a) Simulated radiation pattern using all input ports (b)*

### 3.3.6 Measurement setup and final results

In order to measure the Butler matrix, a PCB test board was designed and prototyped. It is not so easy to design a test board for this small chip, which includes 16 RF ports. The configuration of the input and output ports is shown in Figure 3-24.

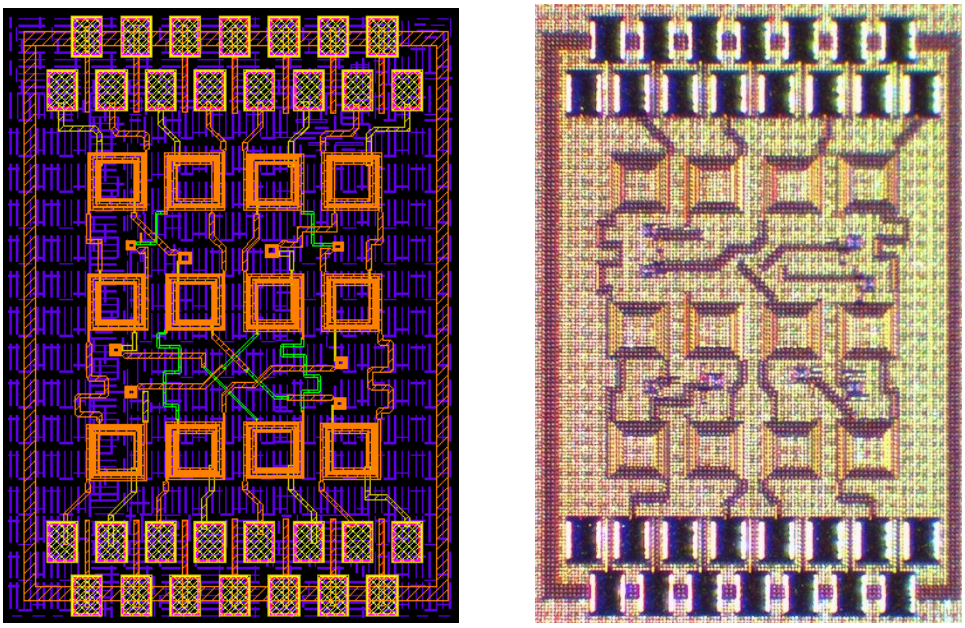


*Figure 3-24 Submitted (left) and manufactured (right) layout of the 8x8 BiCMOS Butler matrix*

As it can be observed, the input and output ports, located in position N-S in the chip, required a high-density arrangement which was necessary in order to

reduce the overall chip area. In order to bond this chip on the test board, shown in Figure 3-25, it was necessary to etch, within the PCB, a cavity in the way that the chip top surface was aligned to the PCB top layer. This solution was required to reduce as much as possible the length of the bonding length. As it can be observed in Figure 3-27, the bonding between the Butler matrix die and the PCB test board required a complex and highly dense net of transmission lines. The maximum length of the bonding path is equal to 700um while the distance between the die and the PCB microstrip line is equal to 100um.

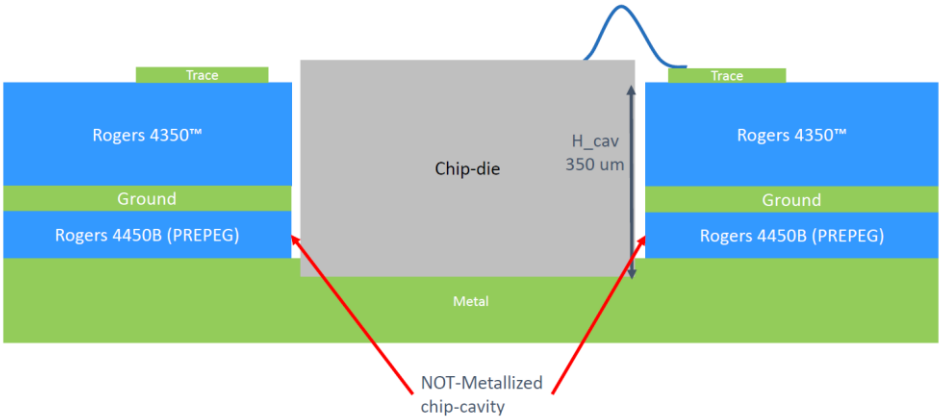



*Figure 3-25 PCB test board section.*

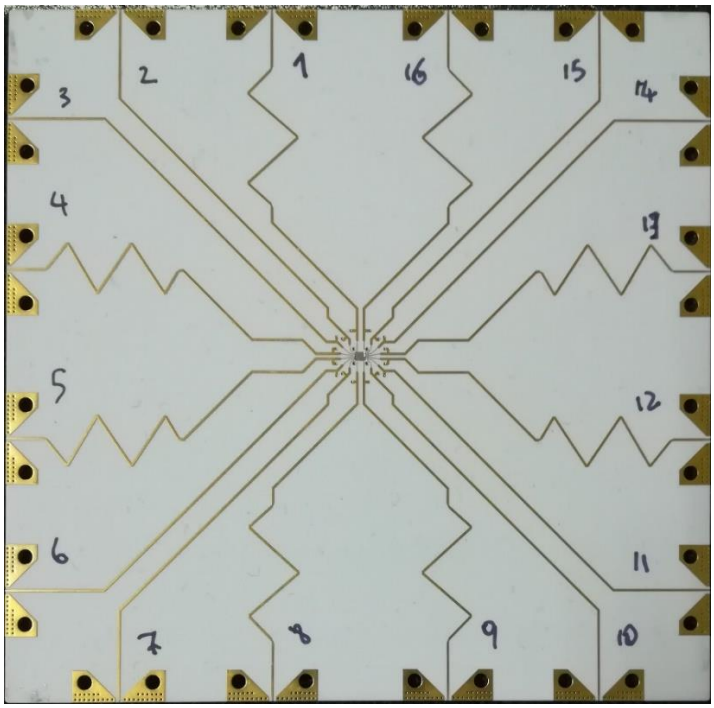



*Figure 3-26 Butler matrix integrated in a PCB board by wire bonding*

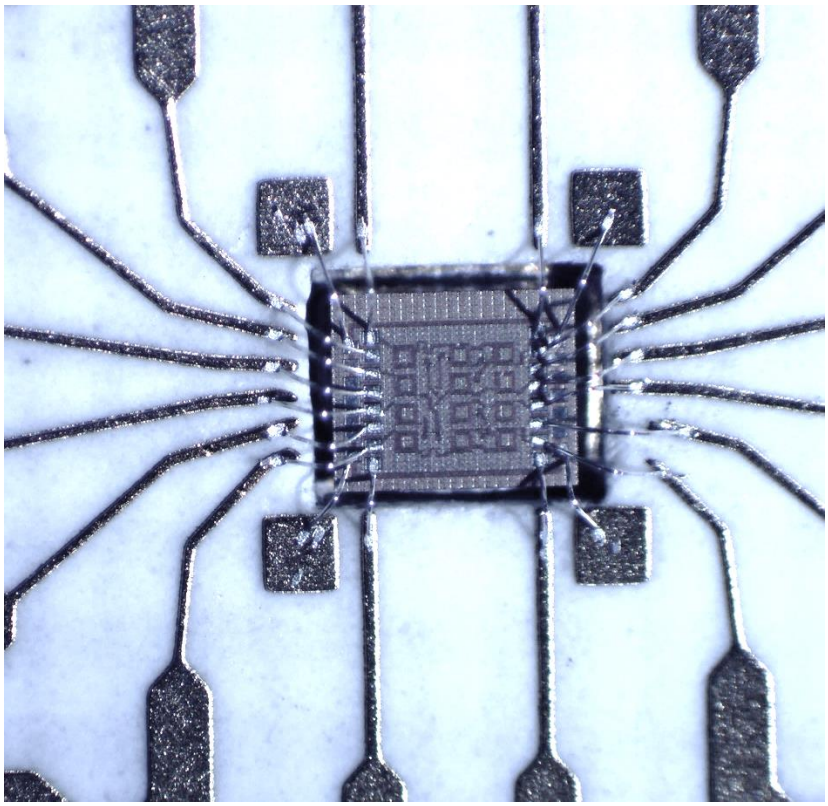


*Figure 3-27 Butler matrix integrated in a PCB board, zoom to the chip area and wire bonding*

As can be clearly presumed from the Figure 3-26 and Figure 3-27, the integration of Butler's matrix on PCBs has been very intricate. The difficulty was in designing a board with cavities in order to reach the chip from the board with very short wire bonding. Wire bonding matching network has been realized with a short-circuited stub on the PCB side. Although de-embedding circuits for all the lines and connectors have been created (they are shown in Figure 3-28) the de-embedded procedure doesn't include the eventual coupling between the wire bonding (that can be only predicted by EM simulation). It has been designed de-embedding circuit for the connector and for each branch of the BM and Hybrid Coupler.

Due to the variations of the production process and a minimum mutual coupling between the wire bonding, the output phases of the measured Butler matrix, even if respecting the frequency linearity, during phase de-embedding has been compensated adding a phase offsets to some output branches.

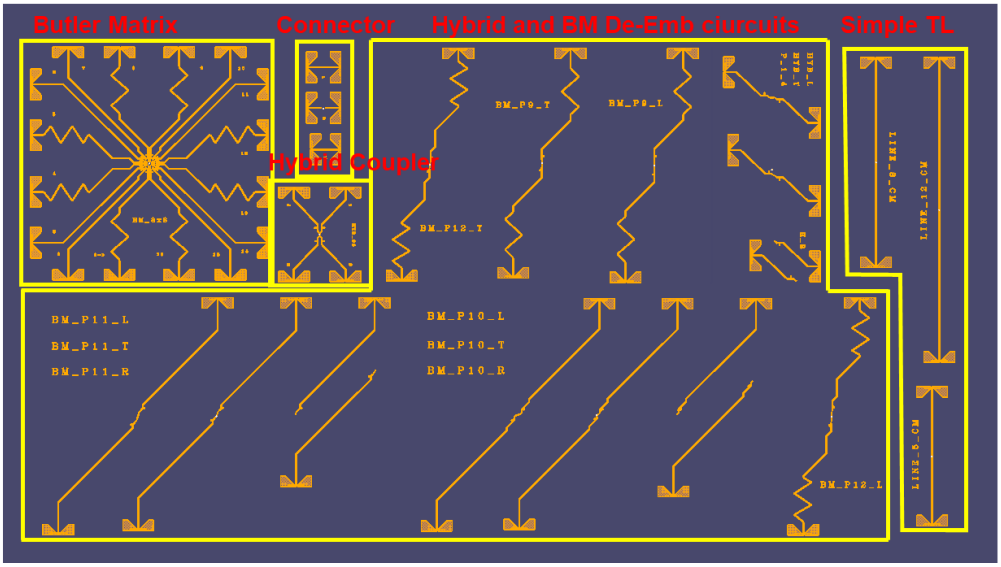



*Figure 3-28 PCB designed test boards of Butler Matrix and Hybrid Coupler. It has been designed de-embedding circuit for the connector and for each branch of the BM and Hybrid Coupler*

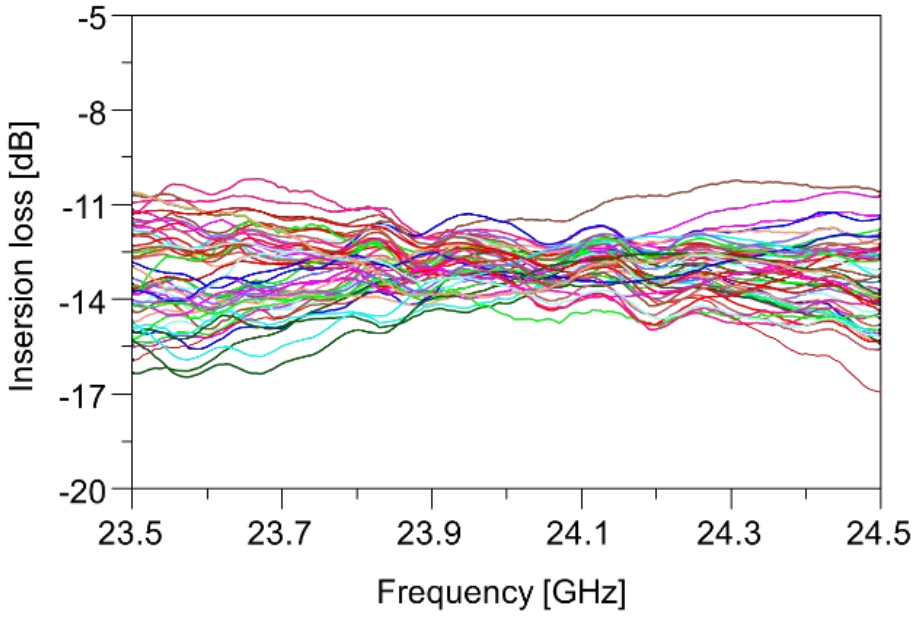



*Figure 3-29 De-embedded measurement of Insertion Loss from all input ports trough all output of the Butler matrix*

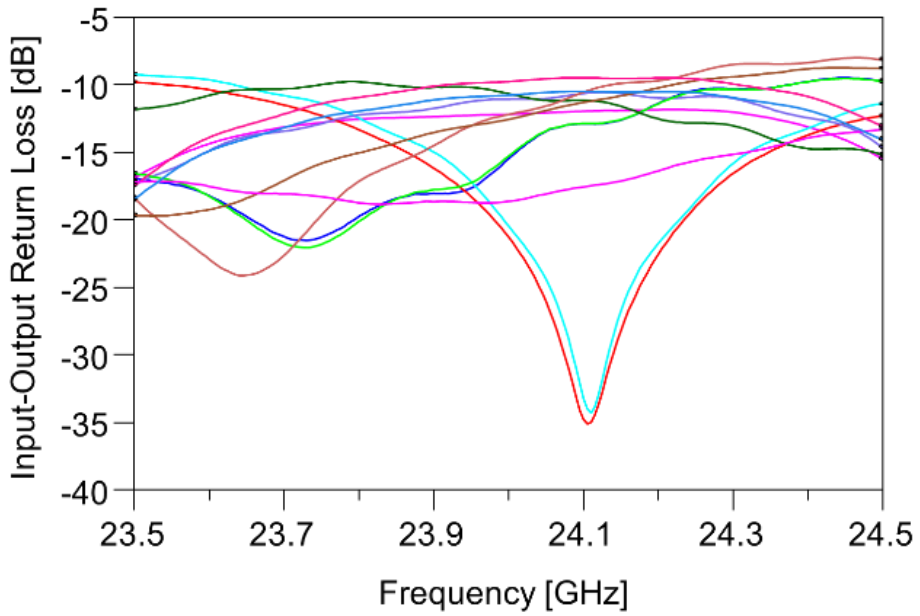



*Figure 3-30 De-embedded measurement of input and output return loss of the Butler Matrix.*

Due to the very long wire bonding and transmission line of the test board, the measured bandwidth of the Butler Matrix is very narrow. As it can be visible in Figure 3-29 and Figure 3-30 Insertion Loss and Return Loss show acceptable performances in terms of amplitude but in a very narrow bandwidth [from 23.5GHz to 24.5GHz] (4% of bandwidth).

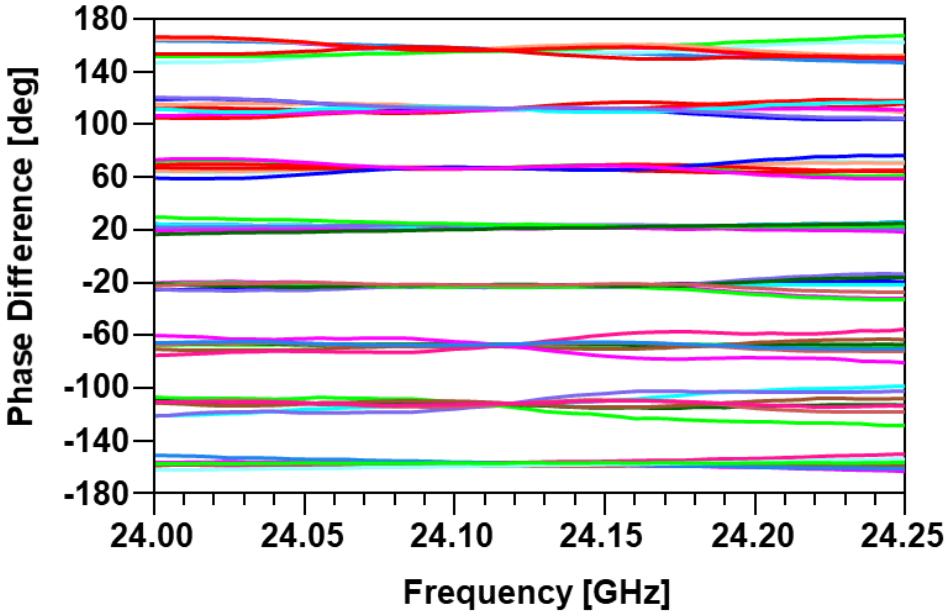



*Figure 3-31 De-Embedded measurement of output phase distribution of the Butler matrix fed though different input ports*

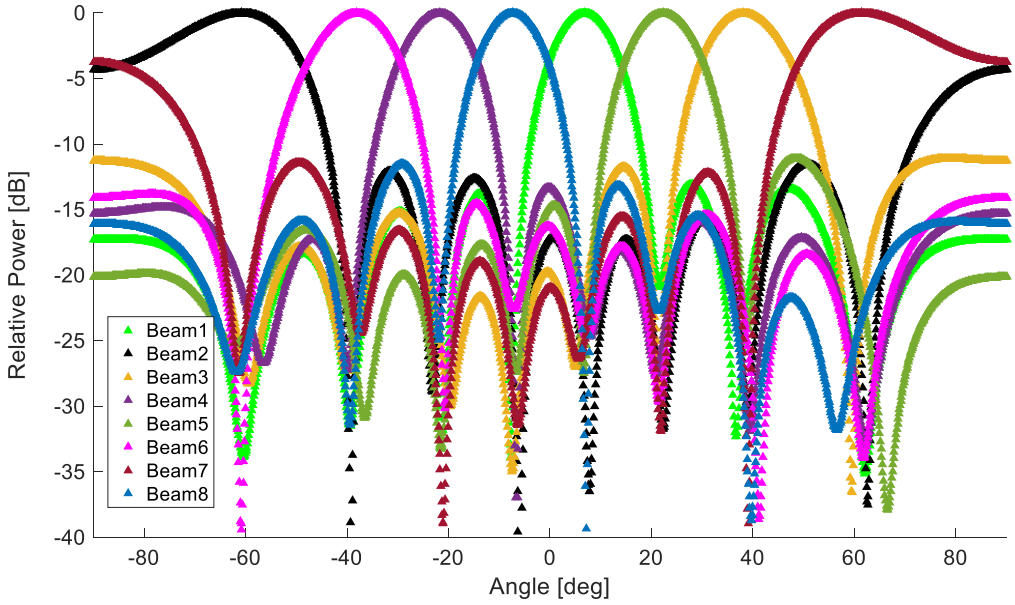



*Figure 3-32 Simulated 24 GHz array factor based on the de-embedded measurement of the Butler matrix with isotropic antenna elements*

The measured output phase distributions of the BiCMOS Butler matrix fed through different input ports is shown in Figure 3-31.

The measured S-parameters of the 8x8 Butler matrix are used to calculate the array factor of the linear antenna array [22]. Assuming ideal isotropic antennas with $\lambda/4$ inter-element spacing, the calculated array factors of the 8 beams are plotted in Figure 3-32.

### 3.3.7 Post measurements studies and future works

Although the Butler matrix measurements were satisfactory in terms of amplitude and phase response, the operating bandwidth was much narrow than the simulated one. Some hypothesis has been discussed in the previous paragraph. The main bandwidth limiting factor is clearly related to the wire bonds which have been compensated through a single frequency optimization process. The following studies have been performed and they are still in the assessment stage:

1) The variance in the length of the wire bonding. In fact, the manufactured wire bonding results in 20% - 30% longer than the desired making useless (or less preforming) the matching network realized on the test board to compensate the inductance caused by the wire bonding.
2) The coupling between wire bonding. Similar to the problem of the point 1). Even if EM simulation of the wire bonding and the chip integration have been performed, having longer wire bonding cause more coupling between them.
3) Side coupling between close lines on the board side. Due to the high density of the circuit close to the chip, the isolation between the line is poor as we design a test board with 50um of isolation between the microstrip in this area. Also in this case, the coupling can be predicted but couldn't be de-embedded.

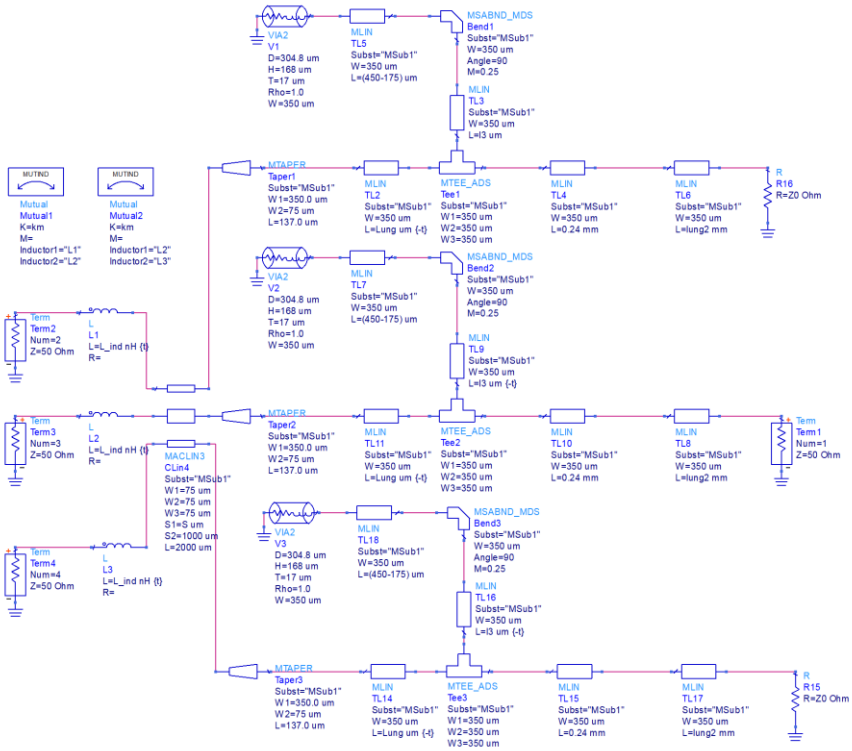



*Figure 3-33 Post measurements study on the test board: ADS representation of part of the board including coupling effect of wire bonding and microstrip*

Possible solutions and future works are:

1) Flip chip integration: the main advantage to use this solution is that wire bonding are not needed anymore (main cause of phase offset and mismatching).
2) Multi-layer test board can be designed also to reduce the coupling effect between line. Closed lines can be drawn in different layers ensuring a good isolation.
3) Instead of solderless connectors on the side of the test board, it can be interesting to think about SMD connectors in order to reduce the size of the test board and also reduce the electrical length between the lines.

   See Figure 3-34 the proposed solution.

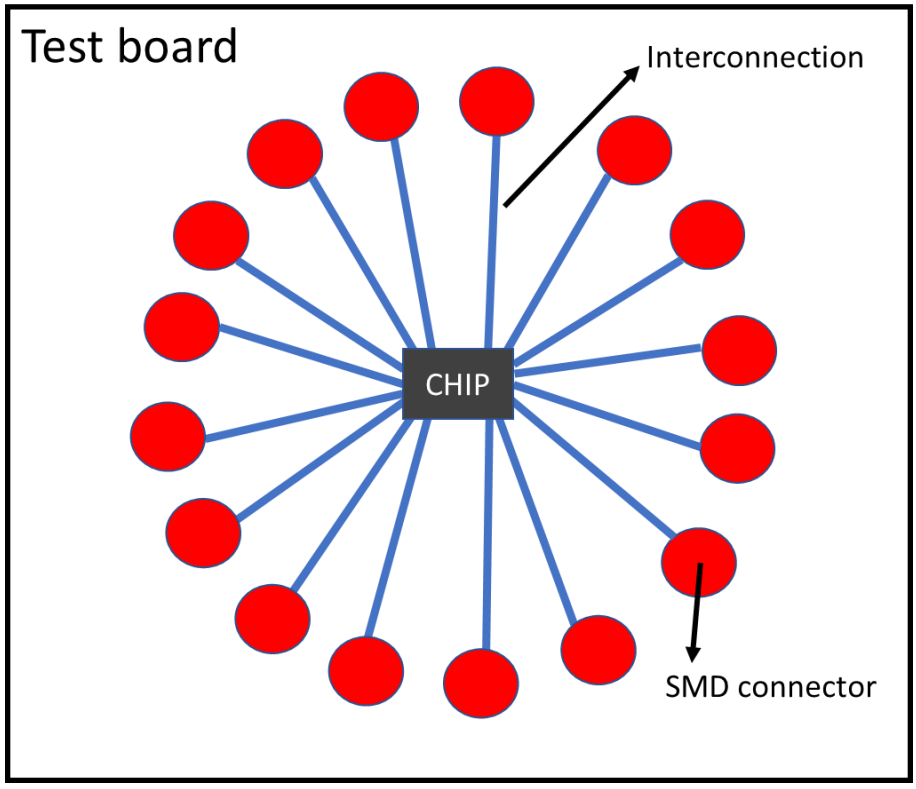



*Figure 3-34 Possible solution for a future test board design with SMD connector*

## 3.4 *Wilkinson power divider*

In microwave systems, the Wilkinson power divider is a component belonging to the family of power splitters that isolates the output ports from the other while maintaining the impedance matching to all ports. This circuit can be used to combine two signals because it consists of passive components and is therefore reciprocal. Published by Ernest J. Wilkinson in 1960 [23], this circuit finds its place in radiofrequency in multichannel systems because it is very effective in minimizing crosstalk.

At the base of the analog phased array system shown in Figure 3-35 there is the combining of the signal at the output of the phase shifter. As an example, a chip for SAT-COM on the move applications is reported on Fig. 3-35 and it shows how the signal should be combined (in RX case or split in TX case).

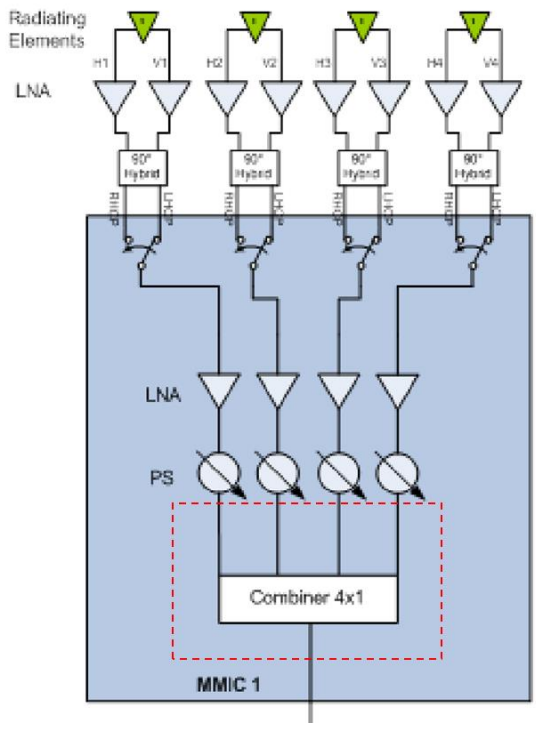



*Figure 3-35 RX chip of a SAT-COM on the move application*

Usually, when it is used as divider, the output power from ports 2 and 3 is equal to half of the incoming power, although an arbitrary power division may be

realized. It is possible to realize a multi-stage Wilkinson combiner in order to combine/split the signal in more than two parts. A Wilkinson power divider/combiner most of the time is realized with only passive component and for this reason is a reciprocal component, it means that the same circuit can be used as a divider or as a combiner. For this reason, to simplify, most of the time the term Wilkinson power divider (WPD in the follow) is used to define the reciprocal component.

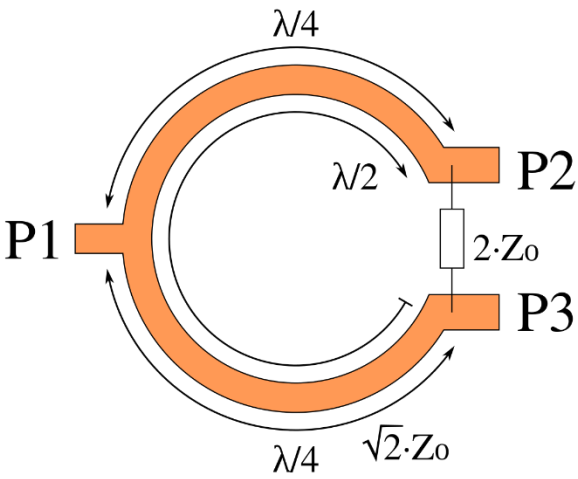



*Figure 3-36 General Wilkinson combiner*

## 3.5 *Wilkinson power divider state of art*

As literature shows, there are several topologies and methodologies to realize a WPD. Herewith are reported some on chip CMOS and BiCMOS designs that can be found in the state of art.

In [24] an integrated equal-split WPD tailored for operation in the X-band is reported. The combiner features differential input/output ports with different characteristic impedances, thus embedding an impedance transformation feature. Over the frequency range from 8 to 14 GHz it shows insertion loss of 1.4dB, return loss greater than 12 dB and isolation greater than 10 dB. The circuit

is implemented in a SiGe bipolar technology, and it occupies an area of 0.12 $mm^2$. The schematic and a microphotograph of the proposed differential WPD is represented in Figure 3-37.

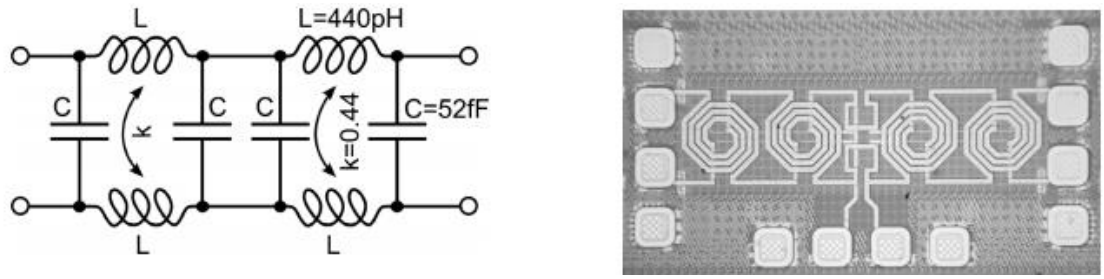



*Figure 3-37 Schematic of the lumped-element equivalent circuit of the line section (left) and Microphotograph (right) of the WPD presented in [24]*

In [25] a 24 GHz four-way miniature WPDs in a standard CMOS technology is presented. The chip area is significantly reduced using a lumped-element design, and the effective areas of four-way WPD are 0.11 $mm^2$. The four-way WPD results in an insertion loss 2.4 dB, an input/output return loss better 15.5 dB, and a port-to-port isolation 24.7 dB from 22 to 26 GHz. In Figure 3-38, the first demonstration of 24 GHz four-way WPD in a standard CMOS technology is shown.

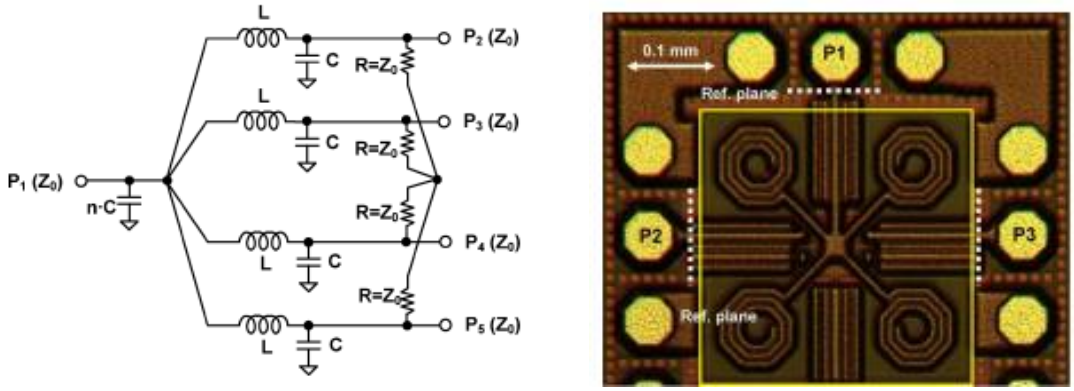



*Figure 3-38 Schematic (left) and Microphotograph (right) of the four way WPD presented in [25]*

In [26] an ultra-compact WPD incorporating synthetic transmission lines at K-band in CMOS technology is presented. An improvement on the size reduction can be achieved by increasing the slow-wave factor of synthetic transmission line.

The presented WPD design is analyzed and fabricated by using standard 0.18 $\mu m$ IP6M CMOS technology. The prototype has a chip size of 480x90 $\mu m^2$, corresponding to 0.0002 $\lambda^2$ at 21.5 GHz. The measured insertion loss and return loss are approximately 4 dB and 17.5 dB from 16 GHz to 27 GHz, respectively. In Figure 3-39 a microphotograph of the proposed WPD is depicted.

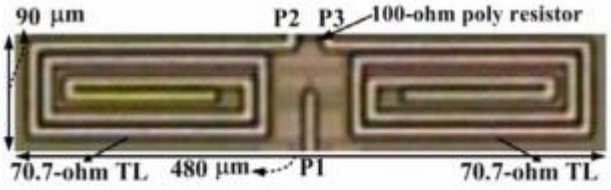



*Figure 3-39 The prototypes of the proposed CMOS WPD using synthetic transmission lines*

## 3.6 *Design of a multi Stage WPC/D*

The goal of this project is to realize a compact multi-stage WPD with a minimum of 20 dB of isolation between the output ports and good performance in terms of phase and magnitude unbalance (typical requirements of an analog phase array system).

| | **Goal** | | **Unit** |
|---|---|---|---|
| BW | 19 - 20 | 29 - 30 | GHz |
| Insertion Loss | <7.5 | <7.5 | dB |
| Input Return Loss | <7.5 | >14 | dB |
| Output Return Loss | >14 | >14 | dB |
| Phase Unbalance | < 3 | <3 | deg |
| Amplitude Unbalance | < 0.3 | <0.3 | dB |
| Insertion Loss Flatness | <0.2 | <0.2 | dBpp |
| Isolation | >20 | >20 | dB |

*Table 3-3 Specification set of WPDs designed for SAT-COM on the move application*

Although their design principle has a generic validity, in this project two multi-stage Wilkinson combiners has been designed for SAT-COM on the move applications. Therefore, the required working frequencies are 20-21 GHz for the downlink (Rx) and 29-30 GHz for the uplink (Tx). The full target set is reported in Table 3-3.

### 3.6.1 Schematic

The design flow starts with the studying of a distributed element WPD as reported in Figure 3-40. The next step has been to transform it in a lumped element WPD, as it illustrated in the Figure 3-41 with the corresponding formulas.

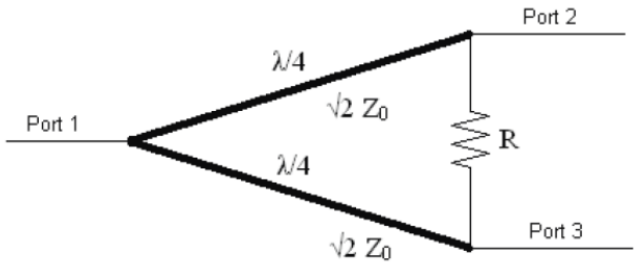



*Figure 3-40 Distributed element Wilkinson combiner/divider*

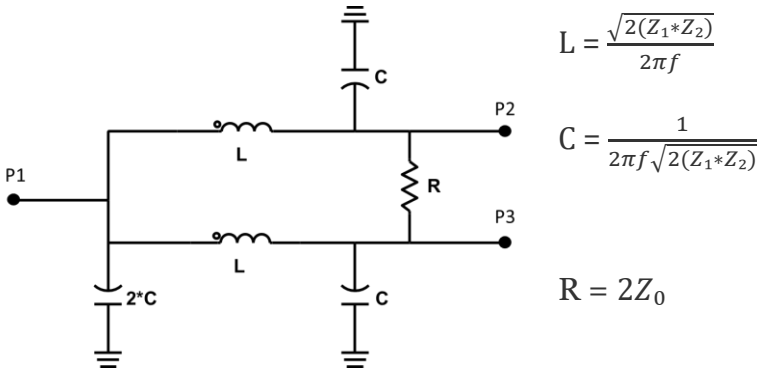



*Figure 3-41 Distributed element WPD*

The same procedure was used to design both Rx and Tx combiner/dividers. The value obtained at 20 GHz and 30 GHz are reported in the Table 3-4.

| | @20 GHz | @30 GHz |
|---|---|---|
| L [pH] | 561 | 375 |
| C [fF] | 113 | 75 |
| R [Ω] | 100 | 100 |

*Table 3-4 Lumped element values of a WPD designed at 20GHz and 30 GHZ*

Figure 3-42 shown the return loss of both Rx and Tx single stage WPD.

Both circuits are implemented following the design flow. For this reason only the description of the Tx design will be reported in the following.

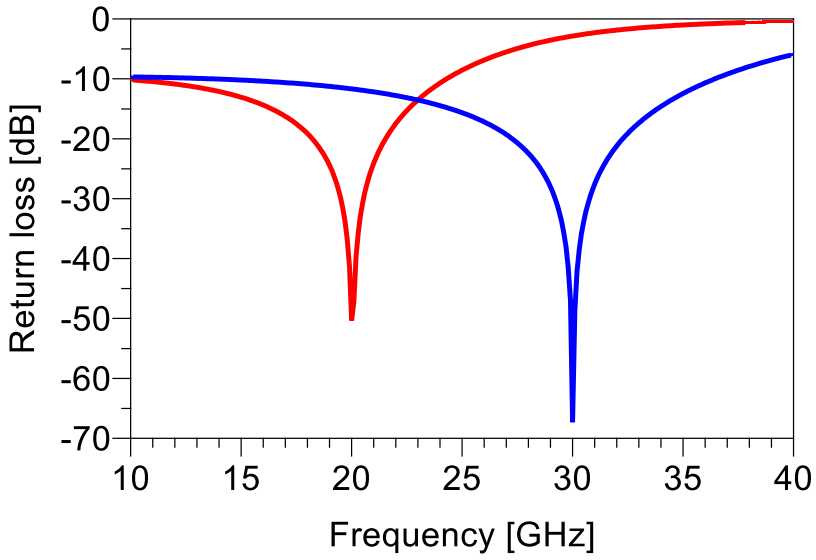



*Figure 3-42 Return loss of 20 GHz (red line) and 30 GHz (blue line) WPD*

In order to obtain a 4 ways power divider, a multi stage WPD has been designed. Once the circuits of WPD (one 50Ω input and two 50Ω outputs) has been designed, the second stage will be exactly a copy of the first stage and the inputs of the second stage has been connected directly to the two outputs of the first stage.

The final schematic is reported in Figure 3-43.

### 3.6.2 Layout

The layout of the two multi-stage WPDs has been designed in SiGe BiCMOS 0.25um technology (IHP SG25H3).

SG25H3 technology is a BiCMOS technology with a gate length of 25nm. The $f_T$ of this technology is 120GHz and the standard backend option offers 3 thin metal layers, two Top Metal layers (Top-Metal1 -2 μm thick metal layer and TopMetal2 -3 μm thick metal layer) and a MIM layer.

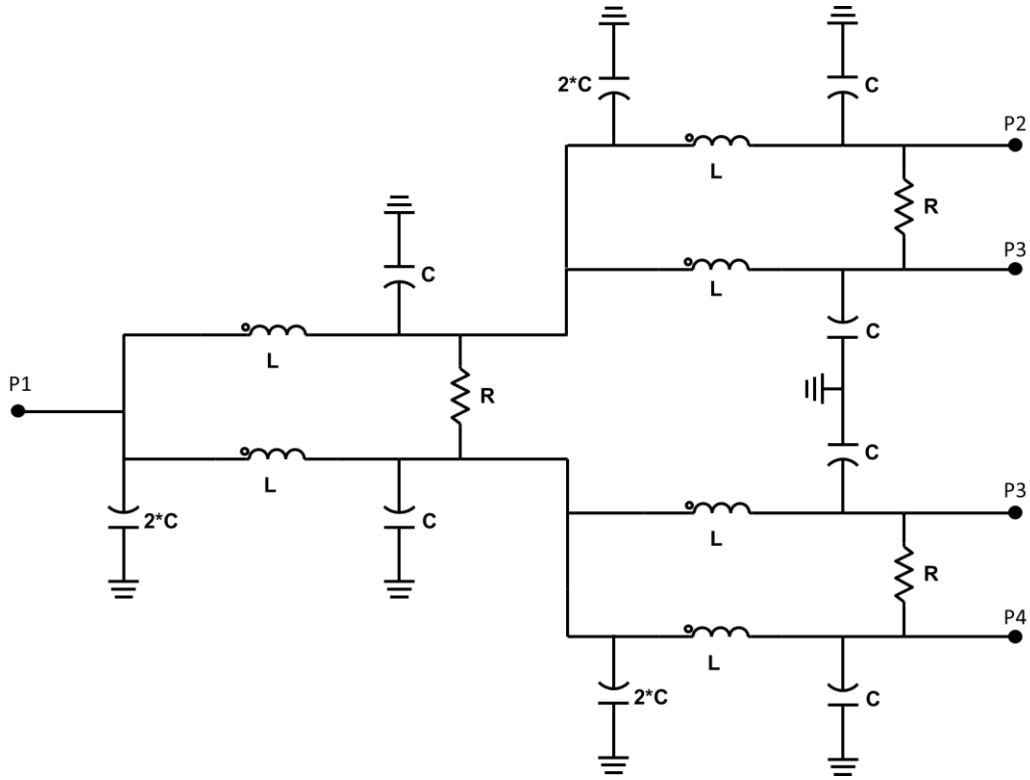



*Figure 3-43 Schematic of 2 stages WPD*

In the layout, inductors and interconnection lines are placed on the thicker TM2 metal layer while M1 act as ground. MIM capacitors and poly-resistors from the design kit has been used. The final layout has been full wave electromagnetic simulated in ANSYS HFSS. Some small tuning of the inductance and capacitance values has been performed in order to compensate the effect of the interconnection lines. The density of the circuit has been optimized to reduce to the minimum the occupied chip area taking always in account the minimum

distance between components to avoid any kind of coupling. The final layout is shown in Figure 3-45. The two outputs port has been rotated of 90° respect to the input to simplify future interconnections with other component (i.e. two different Tx channels). The overall chip size (both layouts almost occupy the same area) is 680x550 $um^2$ (230x430 $um^2$ without pads). RF pads with 100 $\mu m$ pitch are used to measure the performance of the device (S-parameters).

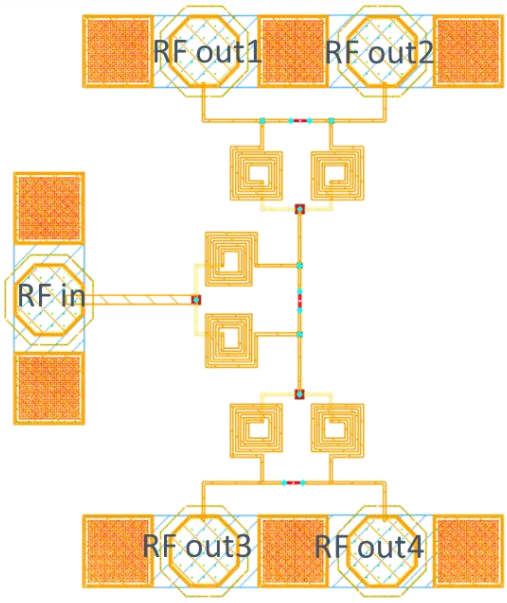



*Figure 3-44 Final layout of a 30GHz Wilkinson combiner/divider*

### 3.6.3 Comparison of measurements and simulations

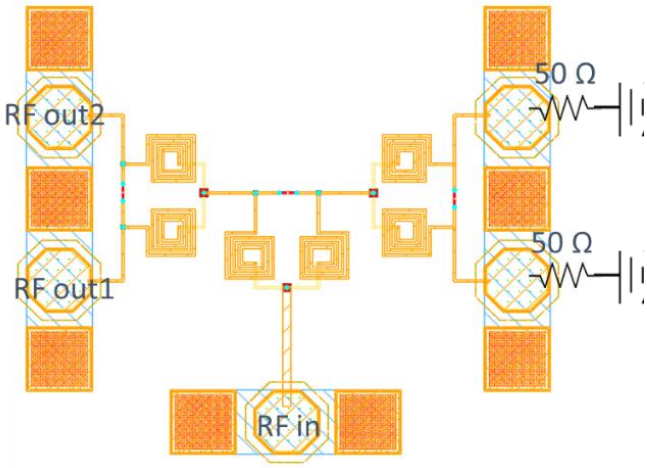



*Figure 3-45 Wilkinson combiner on chip measurement setup*

The measurement setup is shown in Figure 3-45. Since the circuit is symmetric, to simplify the measurement two output ports have been connected to a 50Ω load and GSG and GSGSG probes have been used to measure the input port and the remaining 2 output ports respectively. The de-embedding procedure used to remove from the measurements the RF-pads has been TRL (through, reflect and line). Comparison between simulation (blue lines) and measurement (red lines) results for both case Rx and Tx are shown in Figure 3-46 and Figure 3-47.

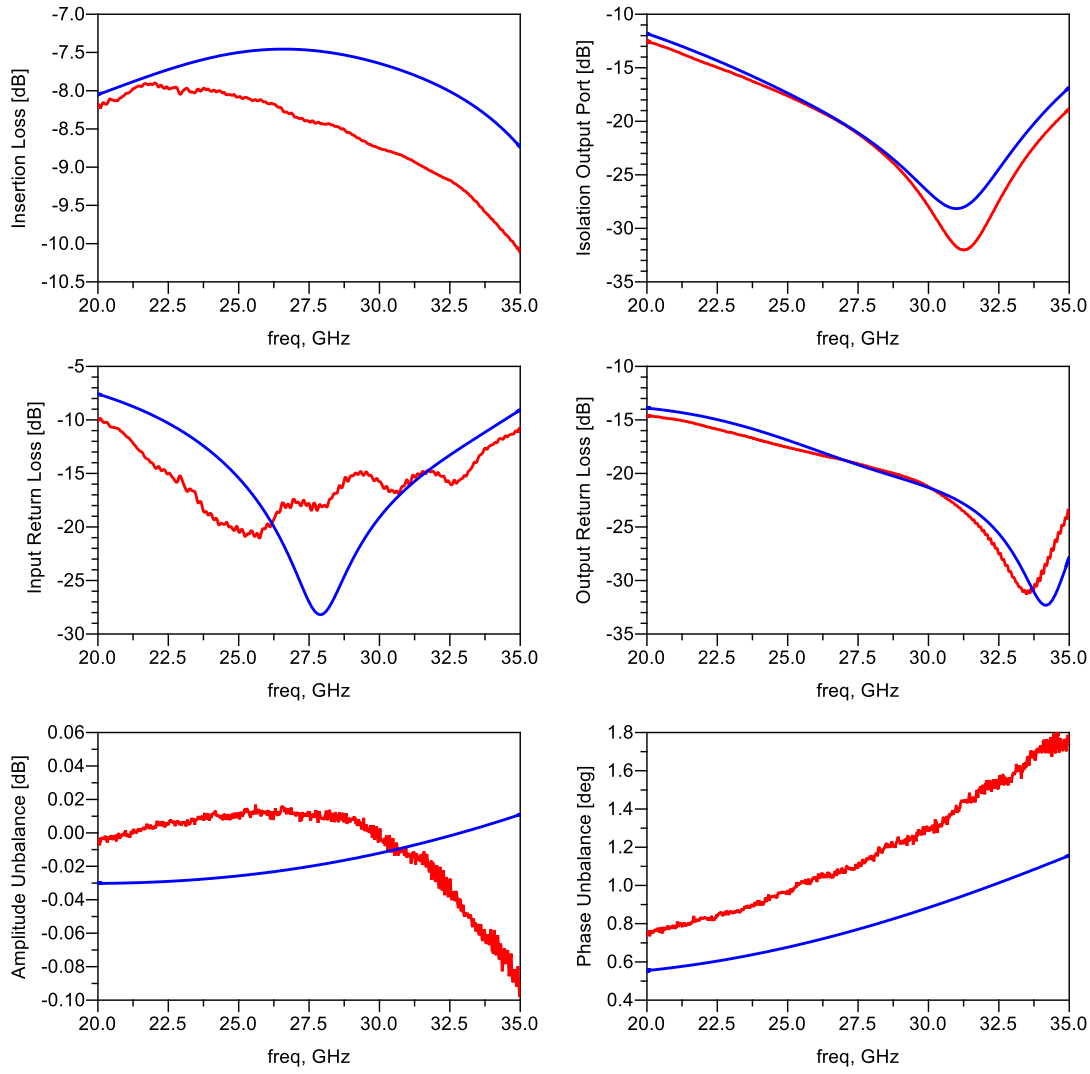



*Figure 3-46 Simulation (blue) vs measurement (red) results of Tx Wilkinson combiner*

The results show a good agreement between measurements and simulations. Furthermore, this layout presents a good compromise between reduction area

and output isolation. Phase and amplitude imbalance are limited to 1° of phase and 0.1dB of amplitude imbalance. Insertion loss is less than 2 dB (1.9 in Rx case and 1.5 in Tx case).

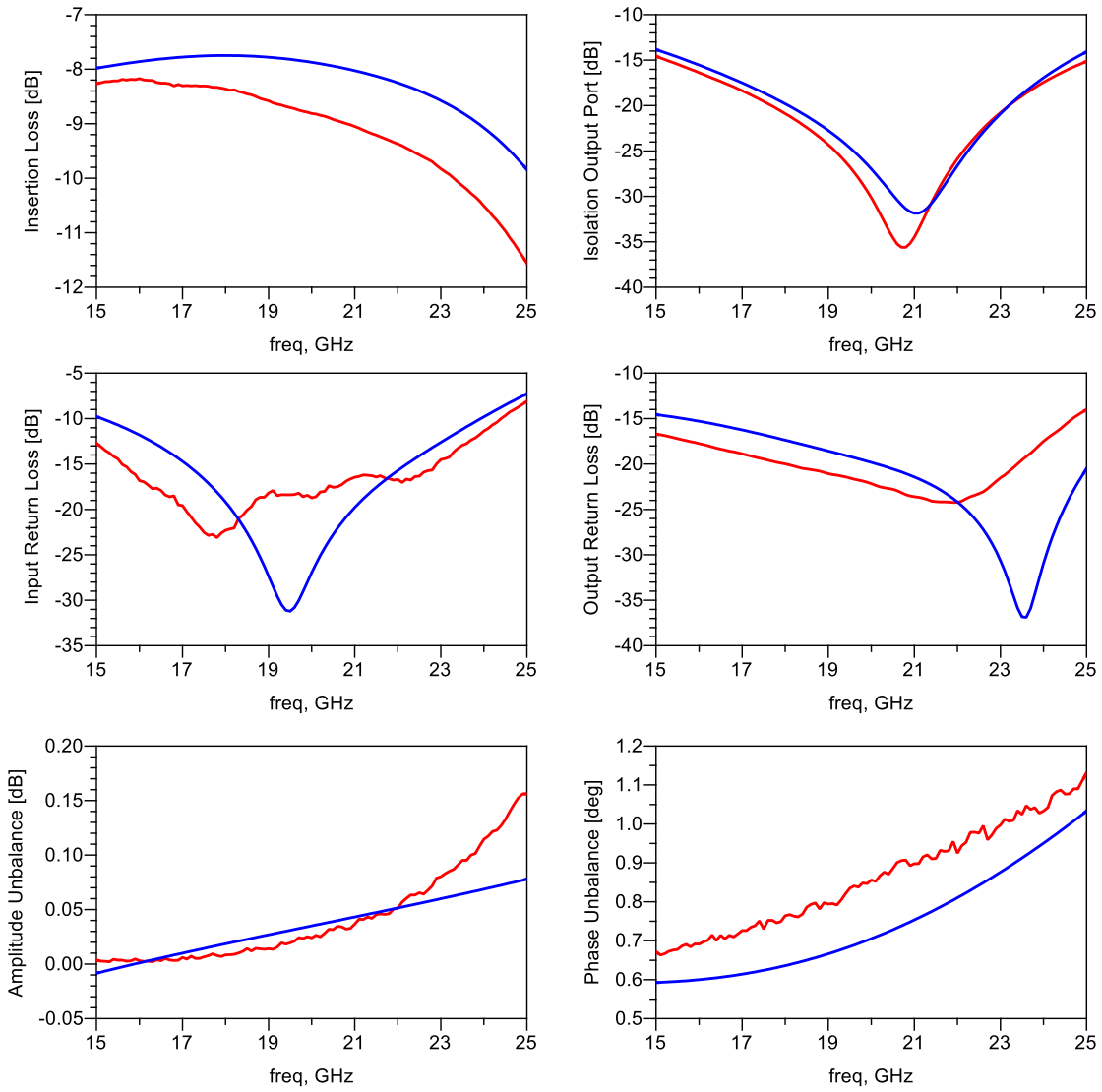



*Figure 3-47 Simulation (blue) vs measurement (blue) results of Rx Wilkinson combiner*

Table 3-5 presents a comparison between this work and the state of art. As it can be noticed, there is only another work in literature reporting a multi-stage Wilkinson power combiner/divider on chip that's why other works of single stage WPD has been included in the table. Form Table 3-5 is possible to assert that this is a most compact multi-stage WPD with the best performances in term of

bandwidth, insertion loss and isolation. The performance of this multi-stage WPD (even size and IL) can be compared with the single stage WPDs present in literature.

| *Ref.* | *[26]* | *[24]* | *[25]* | *This work (Rx)* | *This work (Tx)* |
|---|---|---|---|---|---|
| *Process* | *0.18 µm CMOS* | *0.35 µm BiCMOS* | *0.13 µm CMOS* | *0.25 µm BiCMOS* | *0.25 µm BiCMOS* |
| *# Output* | *2* | *2* | *4* | *4* | *4* |
| *Frequency and BW* | $f_0 = 21\ GHz$ *51.2%* | $f_0 = 11\ GHz$ *51.2%* | $f_0 = 24\ GHz$ *16.7%* | $f_0 = 20\ GHz$ *50%* | $f_0 = 30\ GHz$ *51%* |
| *I.L.** | *1 dB* | *1.4 dB* | *2.4 dB* | *1.9 dB* | *1.5 dB* |
| *R.L.** | *25 dB* | *12 dB* | *15.5 dB* | *30 dB* | *28 dB* |
| *Iso.** | *15 dB* | *10 dB* | *24.7 dB* | *25 dB* | *19 dB* |
| *Max mag. Imbalance* | *0.11 dB* | *0.5 dB* | *N.A.* | *0.14 dB* | *0.1 dB* |
| *Max phase difference* | *0.18°* | *1.5°* | *N.A.* | *1.1°* | *1.8°* |
| *Chip size* | *0.043* $mm^2$ *0.0002* $\lambda_0^2$ | *0.12* $mm^2$ *0.00016* $\lambda_0^2$ | *0.11* $mm^2$ *0.0007* $\lambda_0^2$ | *0.099* $mm^2$ *0.00044* $\lambda_0^2$ | *0.086* $mm^2$ *0.00072* $\lambda_0^2$ |

** Parameter extracted at $f_0$. IL is considered without the nominal losses for power splitting.*

*Table 3-5 Comparison the major characteristics of the proposed Wilkinson power combiners and other works*

With the exception of the insertion loss (Rx case), all the requirements set in Table 3-3 have been achieved. Most likely, this small discrepancy between simulation and measurement results in terms of insertion loss come from bad prediction of the substrate losses or metal sheet resistances (considering valid the de-embedding procedure).

# 4. Phase shifter

Phased array systems will play a crucial role in 5G networks. Through them it is possible to obtain radiation patterns where the direction of the main lobe can be electronically steered, acting appropriately on the phase of the signal sent to each element radiant of the array [27]. Phase shifters are one of the fundamental components of a phased antenna systems. Figure 4-1 shows the basic architecture of a typical beamforming Tx network where the phase shifter (dashed lines) are highlighted.

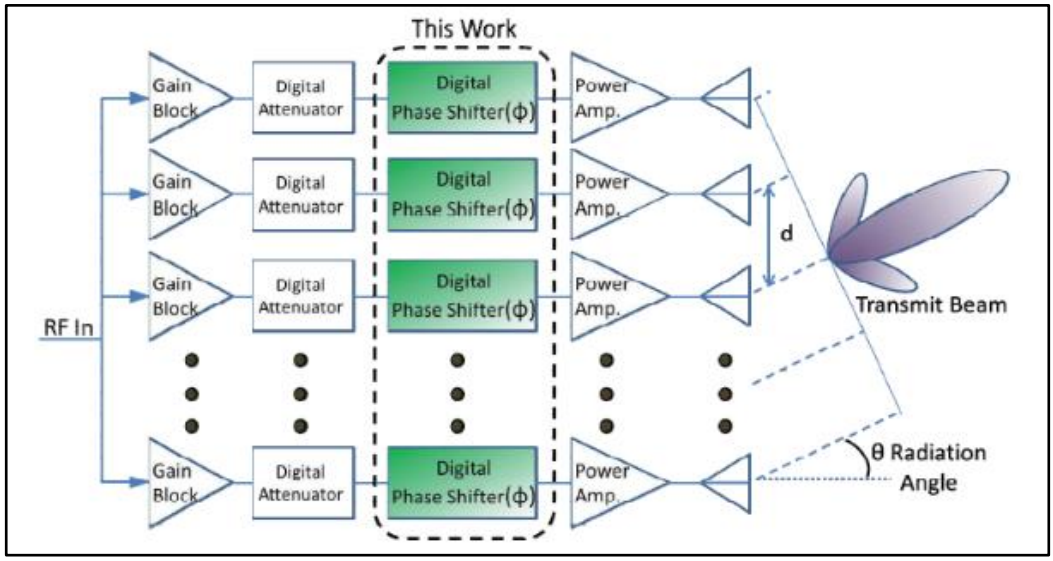



*Figure 4-1 Beam Forming network TX architecture*

## 4.1 *Phase shifter classification*

RF Phase Shifters are used to change the transmission phase angle of an input signal. The input signal is shifted in phase at the output based on the configuration of the phase shifter selected. The transfer function can be defined by the scattering matrix in the form indicated as the follow:

$$S = \begin{bmatrix} 0 & A(\omega)e^{-j\psi(\omega)} \\ A(\omega)e^{-j\psi(\omega)} & 0 \end{bmatrix}$$

where $A$ and $\psi$ represent respectively the gain and phase of the phase shifter and $\omega$ the pulsation of the signal.

A first classification of phase shifter is based on the subdivision of the latter into two large groups:

- Active
- Passive

Active phase shifters, also known as amplifier type phase shifter (ATPS), provide the shift in the required phase by suitably modifying the gain of the VGA (Variable Gain Amplifier), present inside the structure, through a voltage signal applied to the terminals of control of the transistors of the amplifiers. These devices guarantee a phase control range that typically varies from 0° to 360° and the gain of the structure is used to compensate the losses of power of the other components. The main disadvantages of this family of PS are related to the increased consumption of DC power and greater complexity of the circuit.

Passive phase shifters do not include amplification stages and, compared to the active PSs, they offer better performances in terms of phase linearity in the band of interest with lower power consumption [28]. Regarding the disadvantages, the passive PSs have higher insertion loss values and a larger area occupied on the chip that is generally directly dependent on the required phase shift.

A second distinction can be made with respect to the way in which the phase of the signal is controlled by the PS:

- Analog
- Digital

In analog PSs, the input signal phase is continuously varied in a certain interval $[\psi_{\min}, \psi_{\max}]$ by changing the capacitance and/or inductance values of elements

such as varactors and tunable active inductors (TAI) through the use of control voltages ($V_{\text{ctrl}}$). The use of a control network obviously involves an increase in the complexity of the circuit architecture of these PSs and an increase in the consumption of DC power.

In digital PSs, the signal phase can take only a limited number of values depending on the resolution of the PS, i.e. the number of bits of which the structure is characterized. The resolution of the PS affects the number of elementary PS cells connected in cascade and therefore on the occupied area by the entire circuit on the chip. The digital PSs are immune to the noise that can occur on the lines where the control signals are propagated and usually the consumption of DC power is negligible.

With the dependence on phase $\psi$ (see scattering matrix in Figure 4-1) has with the frequency $f$ of the signal, there are two categories of phase shifter:

- Constant phase
- Constant delay or TTD (true time delay)

In the phase shifter with constant phase, theoretically there is no dependence of the phase with the frequency as illustrated in Figure 4-2 therefore:

$\psi(\omega) = \psi_0$ with $\psi_0 = fixed\ phase\ \ set\ from\ the\ PS\ at\ pulsation\ \omega_0 = 2\pi f_0$.

In phase shifter with constant delay or true time delay (TTD), theoretically the phase is a linear function of the frequency as reported in Figure 4-3 Figure 4-2that is:

$\psi(\omega) = \omega * \Delta t$

When the working bandwidth of the PS is sufficiently narrow, these two types of PS can be considered equivalent since they are $\psi = \omega * \Delta t$.

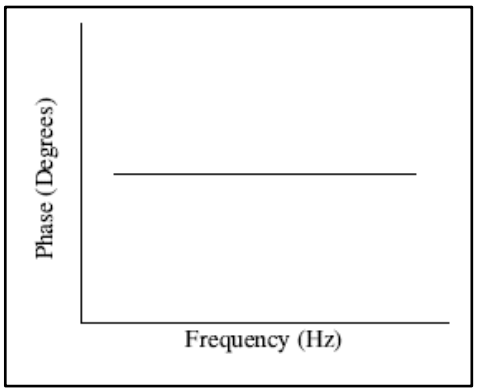



*Figure 4-2 PS with constant phase*

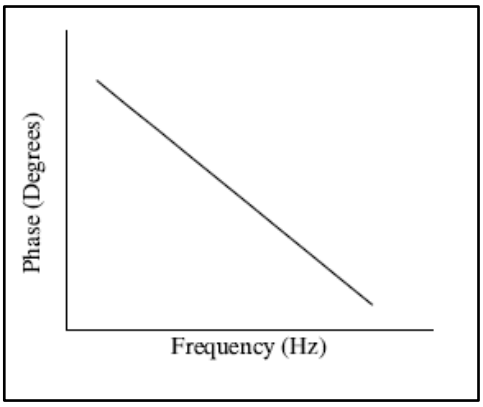



*Figure 4-3 PS with constant delay*

The main parameters that characterize the phase shifter are:

**Phase control range**: normally it is 360 °, necessary to reach the whole phase space.

**Phase resolution**: in analogical PSs, theoretically, it is equal to ∞ but in practice, it depends on the resolution of the DAC. In digital PSs, however, the resolution is limited by the number of bits.

**Insertion loss (IL)**: represents the decrease in the amplitude of the signal output from the PS. In active PSs, due to the presence of VGAs, there may also be an insertion gain.

**Variation of insertion loss versus phase**: In some applications, compensation can also be requested, using VGA, to keep the signal level constant as the phase changes.

**Bandwidth**: frequency field in which the PS can work and in which the defined design specifications must be respected such as, for example, the value of the average IL, average phase error etc.

**Power consumption**: important parameter especially in battery-powered portable devices.

**Chip size**: the size occupied by the structure must be as small as possible to try to reduce costs and increase the level of integration. This is a parameter of fundamental importance especially in phased-array systems where the number of radiating elements is very high and therefore the number of PS modules used in beamforming networks is high.

**Noise figure**: additive noise introduced by the phase shifter; this is an important parameter especially in the phased-array receivers where it is possible that the PS modules of the beamforming network are directly connected to the radiating elements.

**Phase error**: error (typically expressed in degrees) on the value of the insertion phase of the signal evaluated at the project frequency $f_0$

## 4.2 *Phase shifter state of art*

In the following paragraph, **Errore. L'origine riferimento non è stata trovata.** and Table 4-2 show a performance comparison of various analog and digital phase shifter architectures present in literature. **Errore. L'origine riferimento non è stata trovata.** also shows and summarizes very clearly the qualitative performances of the various phase shifter structures [29].

| | Phase shifter type | Tech. | Working freq [GHz] | Range phase control | IL/ripple Gain / Gain Variation | Area | Phase error | NF/FoM | Power consum. |
|---|---|---|---|---|---|---|---|---|---|
| **[30]** | VSPS | 0.18 um CMOS | 15-20 GHz | 360° | 14.2 dB | 0.58 $mm^2$ | 12.5° | NA | NA |
| **[31]** | RTPS | 0.13 um BiCMOS | 58-64 GHz | 360° | 3.7dB - 10.2 dB | 0.16 $mm^2$ | 1° | 36°/dB | NA |
| **[32]** | Distributed | 0.13 um CMOS | 5–40 GHz | 60° | 2.6dB - 3.8 dB | NA | NA | NA | NA |
| **[33]** | Distributed (lumped element) | 0.6 um GaAs | 5-6 GHz | 360° | 4 dB ± 1.7 dB | 0.8 $mm^2$ | 0 | 63 °/dB | 0 |

Table 4-1- State of art of analog phase shifter

| | PS type | Tech. | Working freq [GHz] | # bit | Range phase control | IL/ripple Gain/ Gain Variation | Area [mm^2] | Phase error | NF/FoM | Power consum. |
|---|---|---|---|---|---|---|---|---|---|---|
| [34] | Switched line | InGaAs pin diode | 46 - 49 | 4 | 360° | 6.1 dB/ <1.2dB | 2.16 | < 7.6° | NA | 51 mW |
| [35] | Switched delay | 0.13 µm SiGe BiCMOS | 65 - 85 | 5 | 360° | 20 dB / NA | NA | <3.5° | NA | NA |
| [36] | Switched delay – High/low pass | 0.15-µm GaAs pHEMT | 36 | 4 | 360° | 12.5 dB/±1.5 dB | 1.32 | 4° | NA | NA |
| [37] | Switched delay | 65 nm CMOS CMOS | 28 | 4 | 360° | 6.6 dB/ ±1 dB | 0.23 | 9° | NA | NA |
| [38] | VSPS | 90 nm CMOS | 57 – 66 | 4 | 360° | 4 dB/ < 0.52 dB | 0.31 | < 5.1° | NA | 15.6 mW |
| [39] | VSPS | 90 nm CMOS | 57 – 64 | 4 | 360° | 1.1 dB / <1.6 dB | 0.61 | 4.5°-10° | < 13 dB | 19.8 mW |
| [27] | VSPS | 28 nm FDSOI CMOS | 80 – 97 | 4 | 360° | 0.83 dB / < 2dB | 0.15 | < 11.9° | <15 dB | 21.6 mW |
| [40] | VSPS | 250 nm InP DHBT | 220-320 | 4 | 360° | 13.7dB/ <1.2 Db | 0.23 | <10.2° | NA | < 42 mW |
| [41] | Distributed PS | 130nm SiGe BiCMOS | 26-30 | 40 (Digital Code) | 190° | 9.3 dB | 0.18 | 0.6° | 20 °/dB | NA |
| [42] | Distributed PS | 32 nm CMOS SOI | 55-65 | 3 | 180° | 3.5-7.6 dB | 0.1 | 0.5°-1.2° | 24.5°/dB | NA |
| [43] | Tunable TL PS | 45nm CMOS SOI | 45 | | 75° | 3.3 dB | 0.072 | N/A | 23.9°/dB | NA |

Table 4-2 - State of art of digital phase shifter

| Type | Subtype | Comment | Phase control | Loss/ripple | BW | Size | Noise | $P_{DC}$ |
|---|---|---|---|---|---|---|---|---|
| Vector modulator | VGA | Phase offsets e.g., by filters or couplers | Large | Low (gain)/ low | Small/ Medium | Large | Low | Medium/ large |
| | Attenuators | | Large | High/low | Medium | Medium | Similar to loss | Zero |
| Distributed | TL | Varactor tuned | Large | Medium/ medium | Large | Very large | Similar to loss | Zero |
| | LP-sections | Varactor tuned | Large | Medium/ medium | Large | Large | Similar to loss | Zero |
| | | Varactor and active L tuned | Very large | Small/ medium | Very large | Large | Large | Medium/ large |
| Reflective type | Coupler based | Varactor tuned | Small | Small/small | Medium | Medium | Similar to loss | Zero |
| | | Varactor tuned, resonated with L | Medium | Medium/ large | Small | Medium | Similar to loss | Zero |
| | | Parallel LC resonances | Large | Large/ large | Small | Large | Similar to loss | Zero |
| | | Varactor and active L tuned, resonated | Large | Medium/ medium | Small | Small | Large | Medium/ large |
| | Circulator based | Z tuning | Small | Medium/ medium | Large | Small | Large | Medium |
| | | $g_m$ tuning | Medium | Small/small | Large | Small | Large | Medium/ large |
| | | $g_m$ and Z tuning | Large/ medium | Medium/ medium | Large | Small | Large | Medium/ large |
| Switched | TL | Simple "digital" control | Large, but resolution limited by number of bits | High/ medium | Medium | Very Large | Similar to loss | Zero |
| | HP/LP | | | High/ medium | Small | Large | Similar to loss | Zero |

*Table 4-3 - Typical qualitative performance of integrated phase shifter approaches. TL: transmission lines, LP: low-pass filter, HP: high-pass filter, gm: trans-conductance, Z: impedance, L: inductance [29].*

## 4.3 *Quarter Wavelength Reflect Type Phase Shifter*

In this chapter, a tunable band-pass phase shifter is proposed. A novel compact quarter-wavelength resonator filter phase shifter (QWRF-PS) using the lumped elements is designed and fabricate using a 0.25um BiCMOS technology with 5-metallization layers.

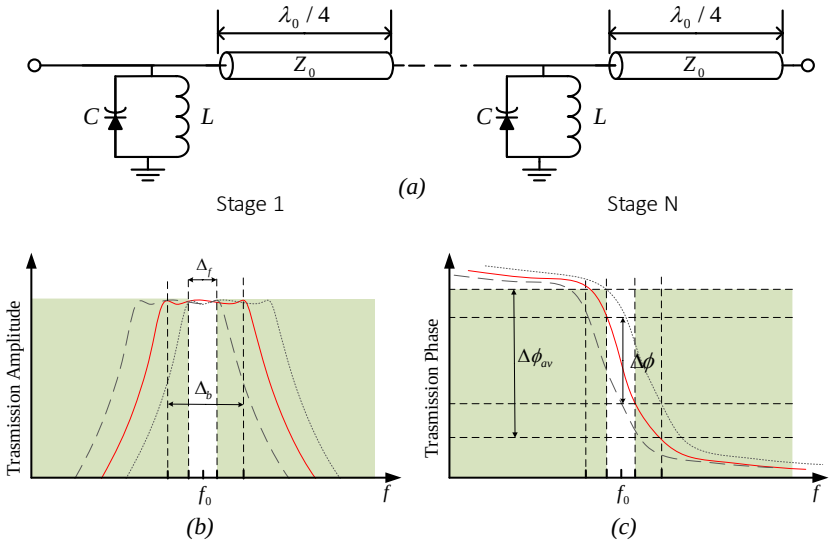



*Figure 4-4 (a) QWRF-PS simple model. (b) Amplitude and phase transmission responses of a QWRF-PS obtained with the varactor diodes biased to achieve the lowest (solid line) and highest (dashed line) capacitance values [30].*

The main idea is to realize a pass band filter that works as PS and it is designed cascading several LC resonators with quarter-wavelength transmission lines. Varying the reactance of the LC resonator results in a shift of the transmission phase (ΔΦ). Part of this shift lies in a range where transmission amplitude remains acceptable (in a certain bandwidth, Δb). This effect is more clearly illustrated in Figure 4-4 b and c. The phase shift range mainly depends on the number of cascaded stages as each stage introduces a pole in the transmission response of the filter, which in turn determines an increase of 180 of the phase range observed when the frequency is varied.

The basic cell is designed with a LC resonator connected in series with a quarter-wavelength transmission lines (Figure 4-4a). The starting point has been the

study of a single cell. It has been performed a parametric simulation of a LC resonator swiping the capacitance and keeping fixed the inductance in order to evaluate the capability in terms of phase shift at a certain frequency $f_0$. The results of this simulation are reported in Figure 4-5 and its show that with a ratio $C_{max}/C_{min}$ around 2 it's possible to achieve 40° with taking care of matching and return loss.

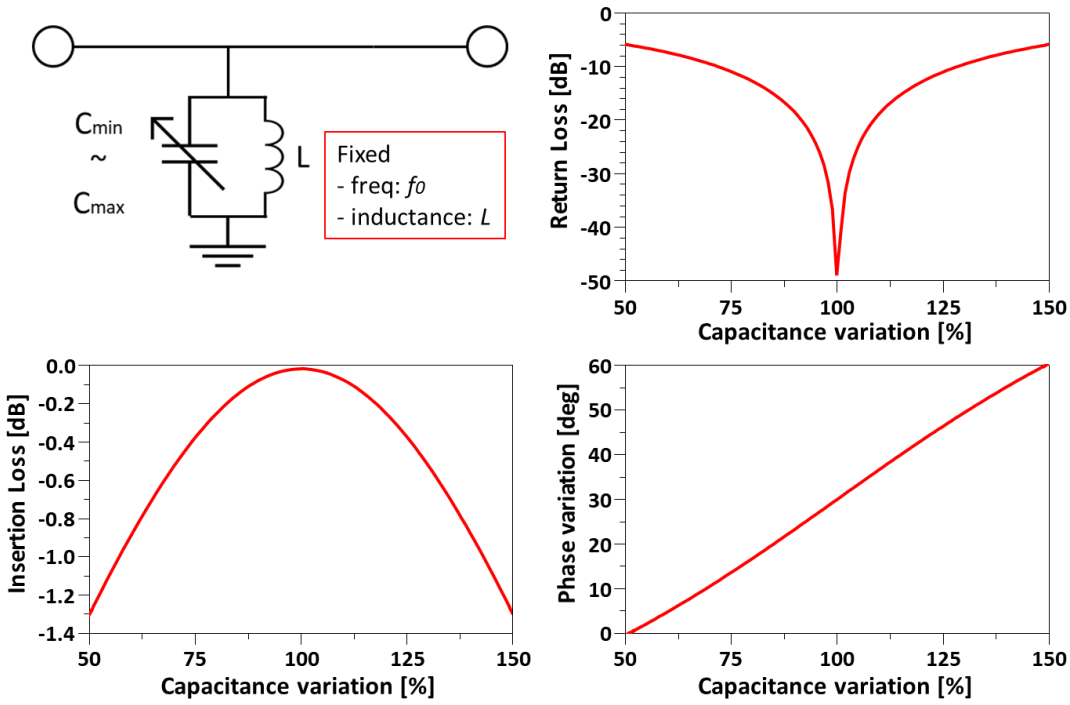



*Figure 4-5 Single cell results swiping C and keeping L fixed (@23.5 GHz)*

To increase the phase difference range, it is possible to put several single cells in series interposing a $\lambda/4$ transmission line.

As proof of concept, a QWRF-PS has been designed at $f_0 = 23.5GHz$ with a bandwidth $\Delta f = 2GHz$ and a transmission phase shift $\Delta\Phi$ of 180°. The model of the circuit is shown in Figure 4-6a. According to the study of the single cell, 5 stages have been employed in the proposed design. The block diagram of the proposed design is reported in Figure 4-6.

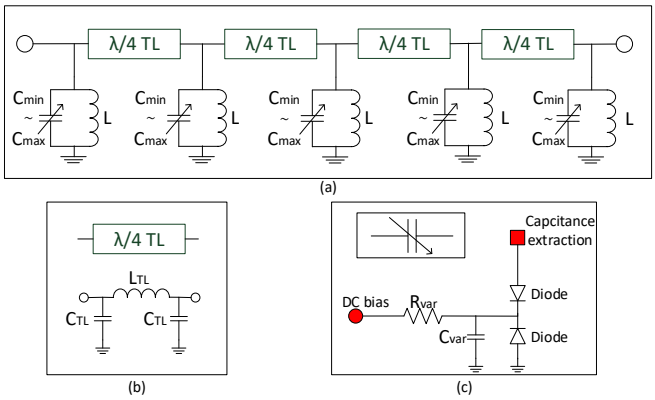
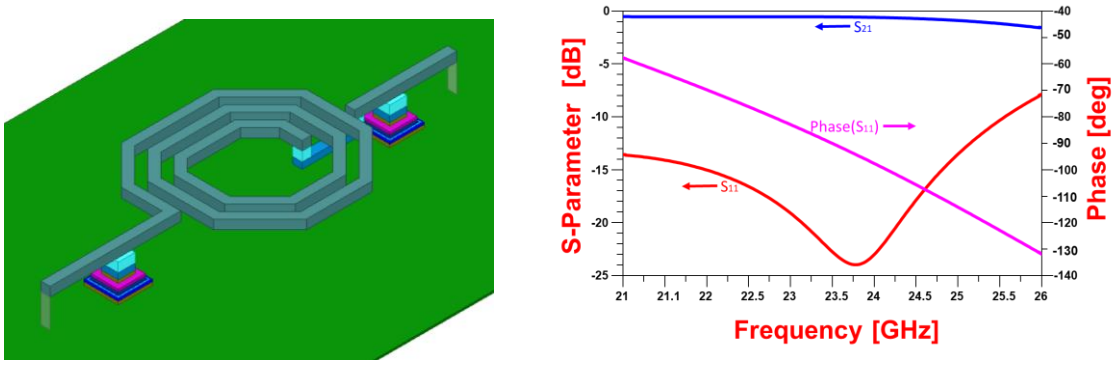



*Figure 4-6 (a) Schematic model of QWRF-PS (b) Lumped elements transmission line (c) Simplified varactor model*

### 4.3.1 Quarter-wavelength transmission lines design

In order to implement the QWCR BPF in monolithically integrated technology it is essential to reduce the size of the TL sections. For this reason, quarter-wave TL sections were implemented using their equivalent $\pi$. The series inductor was implemented using a square inductor on the top metal layer whose nominal value is $L_{TL}$ and two series metal-insulator-metal capacitors $C_{TL}$ equal to 350 pH and 132 fF respectively. The π-network consists of two parallel capacitors and a series inductor. The inductor was designed using a rectangular geometry placed on the top metal layer (Figure 4-7a). As it can be observed in Figure 4-7b this design provides a shift of 90° between the input and output port with an insertion loss of $0.7dB$ @23.5 $GHz$. These losses are mainly due to the inductor which has a quality factor of 12. The overall size occupied by this block is equal to $120 \times 60\ \mu m^2$.




(a) (b)

*Figure 4-7 (a) HFSS layout of a lumped elements λ/4 transmission lines and (b) simulation results of Phase delay and S-Parameter*

### 4.3.2 LC resonator and varactor diode design

The second block required for the implementation of the QWCR BPF is the single tunable resonator. In principle, tunable resonators can be achieved through different techniques. Examples of tunable BPF in microstrip technology are reported in [31]–[33] while an example of monolithically integrated band-stop filter is reported in [34]. In this work, a highly compact varactor-tuned LC parallel tank was employed. It is worth noticing that the filter tuning range and in turn also the PS phase range is directly related to the maximum variation of capacitance that is possible to achieve with the varactor. Unfortunately, for the semiconductor technology at hand the performance of the varactor diode in the available technology is not optimal in the selected frequency range as the ratio between the maximum and minimum available capacitance varies between 25 and 12 pF when the diode is reverse biased between 1 and 5 V. This range would not be sufficient to adequately tune the filter band pass. For this reason, a new varactor configuration was implemented by using a couple of reverse biased pin diodes in back-to-back configuration. In order to increase tuning range, 4 pin diode cells have been shunt-connected, as shown in Fig. 3. The resulting diode

capacitance, $C_{var}$, varies in the range from 210 to 95 fF when the control voltage, $V_{DC}$, varies between -0.5 and 3.5 V. Diode losses have been taken into account by the resistance $R_{var}$ whose value has been estimated to be 10 KOhm while the ground coupling effects are modelled through a capacitance, $C_g$, equal to 1pF while the PIN diode model included in the design kit was employed for modelling purposes. The simulated behaviour of the varactor and its quality factor are shown in Fig. 3-c. As it can be observed, the quality factor of the diode varies from about 27 to 57 within the bias tuning range. Although the overall performance of the PS will be affected by the varactor losses, it is important to notice that this aspect is strongly dependant on the available technology and that IL would significantly be reduced if the Q factor of the diode is increased.

The phase shift is directly related to the maximum variation of capacitance that is possible to achieve with the varactor.

$$r_C = \frac{C_{max}}{C_{min}}$$

A simplified model of the varactor is shown in Figure 4-6c.

The junction capacitance of a varactor can be changed electrically by applying a control voltage $V_r$ (thus $C = f(V_r)$). It can be classified as a passive element because it can only store reactive energy and cannot supply energy (as it happens for the amplifiers). A varactor is a nonlinear component, and while the nonlinearity of diodes is studied through the external characteristic $I - V$, the non-linearity of the varactor is evaluated starting from the characteristic $C - V$. As example, the symbol of a varactor diode is shown in Figure 4-6a with the indication of the simplified equivalent electric circuit (Figure 4-6b) and of the characteristic C-V (Figure 4-6c).

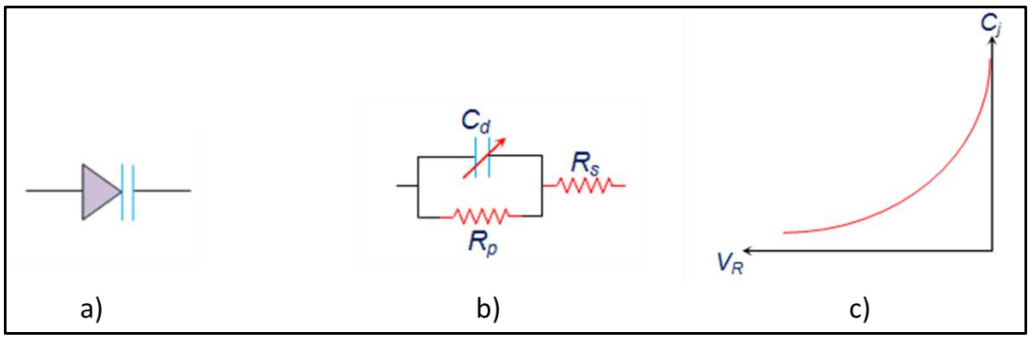



*Figure 4-8 (a) Symbol, (b) equivalent circuit and (c) C-V characteristic of a varactor diode*

Regarding the characteristic parameters of varactors, the two most important figures of merit are the quality factor $Q$ and the tuning range $r_C$, followed by other parameters such as the auto-resonance frequency $f_r$ and the parameter $ESA$ (effective silicon area).

The $Q$ parameter for the varactor is calculated as:

$$Q = \frac{Energy_{stored}}{Energy_{dissipated}} = \frac{Im\,(Z(Vr))}{Re(Z(Vr))} = \frac{X_{C_d}\,(Vr)}{R_s\,(Vr)} = \frac{1}{\omega C_d(Vr)R_s(Vr)}$$

where:

$Z(Vr) = R_s(Vr) - jX_{C_d}(Vr)$ = impedance seen from the varactor's terminals

$Vr$ = reverse bias voltage = control voltage of the varactor

$$\omega = 2\pi f$$

The quality factor equation shows that to maximize Q, it is necessary to minimize resistive losses (related to the energy dissipated by the resistive part of the component under test). In the case of negligible resistance, the maximum energy stored by a varactor can be ideally calculated as:

$$E_{cmax} = \frac{1}{2} C_p V_p^2$$

where: $C_p$ = capacity value imposed by the varactor

$V_p$ = maximum voltage

The tuning range $r_C$ is another important parameter used to evaluate the effective functionality of the component. The $r_C$ of a varactor can be defined as the ratio

between $C_{max}$ and $C_{min}$ where $C_{max}$ and $C_{min}$ respectively represent the maximum and the minimum capacity value obtained by considering two specific voltage values $V_{r_{max}}$ and $V_{r_{min}}$. The aim is to design a varactor trying to extend as much as possible the tuning range, equal to $r_C$, in the desired voltage range.

To increase the capacitance values of the varactor, it is possible to connect several diodes in parallel with the anode always connected to ground. As an example, in in Figure 4-9 it is reported the case of two back-to-back diodes compared with a single varactor. From this picture it is possible to deduce that even if the capacitance values increase with the increase in the number of identical junctions connected in parallel, the amplitude of the tuning range remains the same as in this case the value of the $r_c$ is about 2 in both cases.

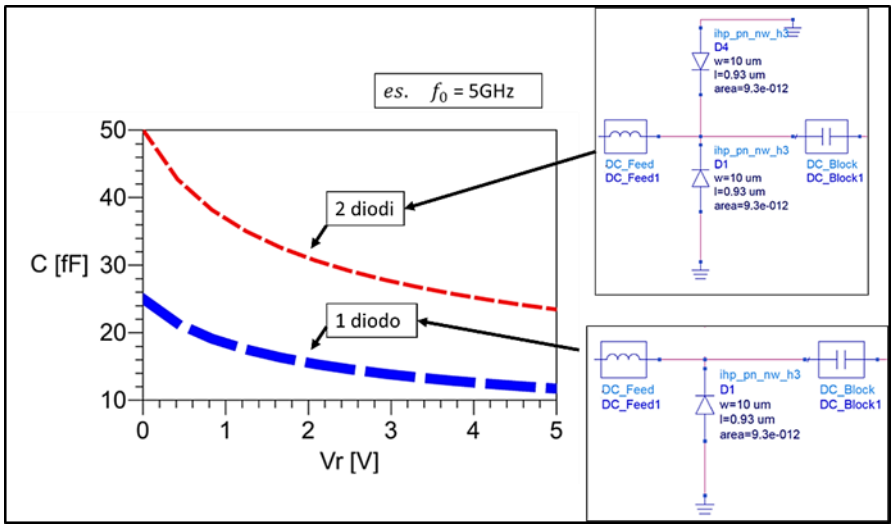



*Figure 4-9 C-V curve of a varactor done by 1 or 2 diodes*

Starting from the considerations just made, Figure 4-10 shows the complete circuit model of the PN junction varactor used in the QWRF-PS, operating at the frequency $f_0 = 23\ GHz$,.

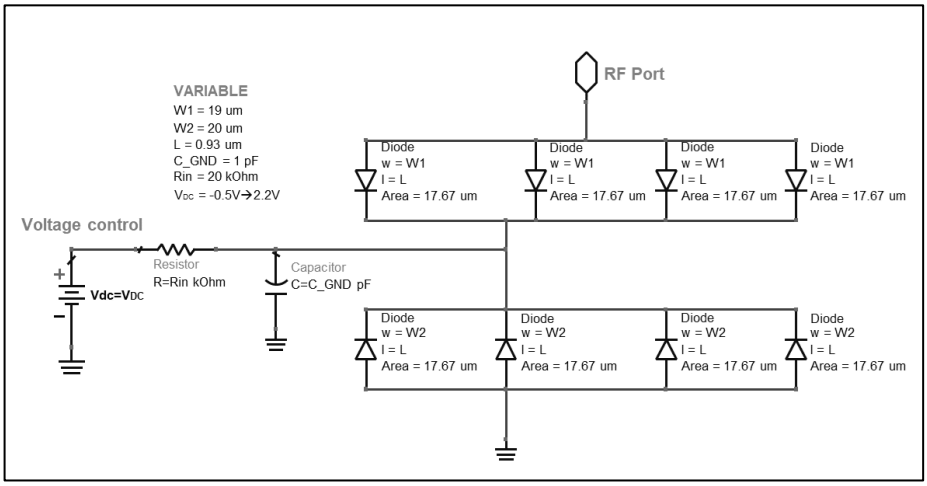



*Figure 4-10 Full schematic of a 23GHz PN junction varactor for QWRF PS*

In the schematic in Figure 4-10, there are two groups consisting of 4 PN junctions connected in parallel. The cathodes of the diodes present in these two groups are connected to a common node to which the control voltage of the varactor $V_{DC}$ is applied. Between the common node and the ground has been inserted the capacity $C_{GND}$ capacitor. This capacitor doesn't affect the ratio $\tau_c$ but increase the overall value of the capacitance that can be extracted.

The upper group of diodes has three functions:

1) acts as DC-block for the DC signal
2) act as AC-pass for the RF signal.
3) The back-to-back configuration overcomes the problem of the RF modulating the tuning voltage as the effect is cancelled out - as the RF voltage rises, the capacitance on one diode will increase and the other decrease. The back-to-back configuration also halves the capacitance of the single diode as the capacitances from the two diodes are placed in series with each other. It should also be remembered that the series resistance will be doubled, and this will affect the Q.

The resistor $R_{in}$ must be high enough to isolate the bias circuitry from the tuned circuit without lowering the Q. It must also be big enough to control the bias on

the diode against the effects of the RF passing through the diode. A value of 10-20 kΩ is often a good starting point.

The proposed configuration has been first simulated at the frequency $f_0 = 23.5GHz$ and results are reported in Figure 4-11. The curve $C - V$ was obtained considering a sweep associated to the control voltage $V_{DC}$ which varies from $-0.2\ V$ to $2.2\ V$.

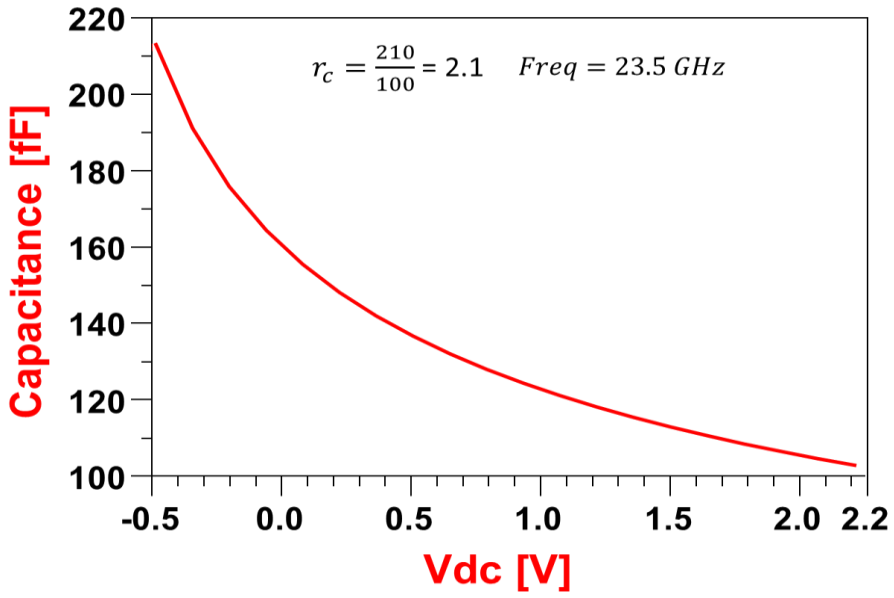



*Figure 4-11 C-V curve of the designed varactor at 23.5 GHz*

The capacitance value has been calculated from the impedance seen at the output of the varactor, $Z_L$, with the assumption of negligible losses.

$$C\ (V_{dc}) = -\frac{1}{2\ \pi\ f\ Im\{Z_L(V_{dc})\}}$$

Figure 4-12 shows the trend of the quality factor when the control voltage $V_{DC}$ changes at the design frequency $f_0 = 23.5GHz$. Increasing the voltage results in a decrease of the capacitance and in an increase of the quality factor. Therefore, the Q can be written as:

$$Q\ (V_{dc}) = \frac{1}{\omega\ C(V_{dc})\ Re\big(Z_L(V_{dc})\big)}$$

In the case at hand, the value of Q varies from a minimum of 30 to a maximum of 60.

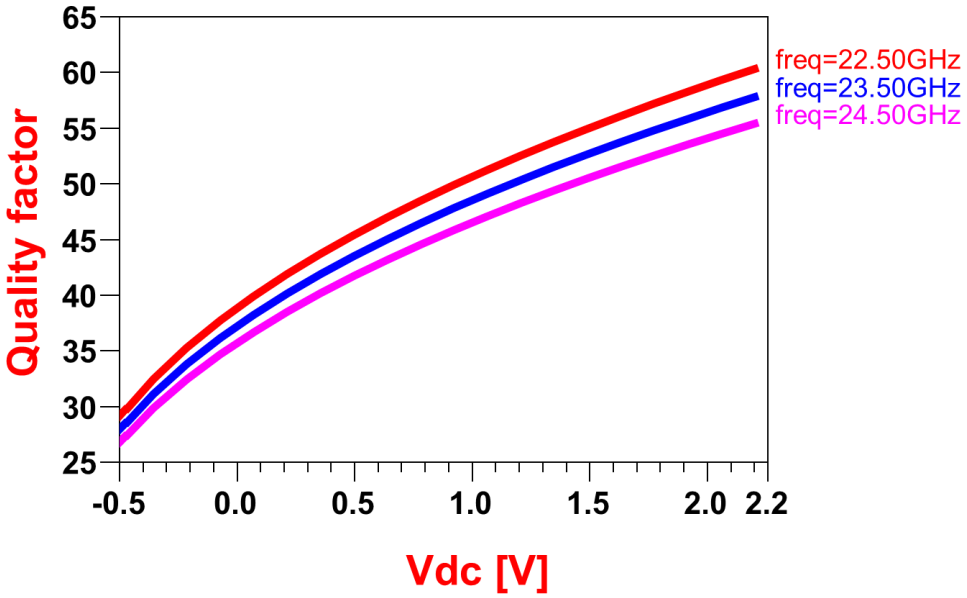



*Figure 4-12 Quality factor performance versus $V_{DC}$*

From the trend of the coefficient $S_{11}$ reported on the Smith chart (Figure 4-13) it can be observed the phase variations of the capacitance (vs. bias) and the losses introduced by the diodes.

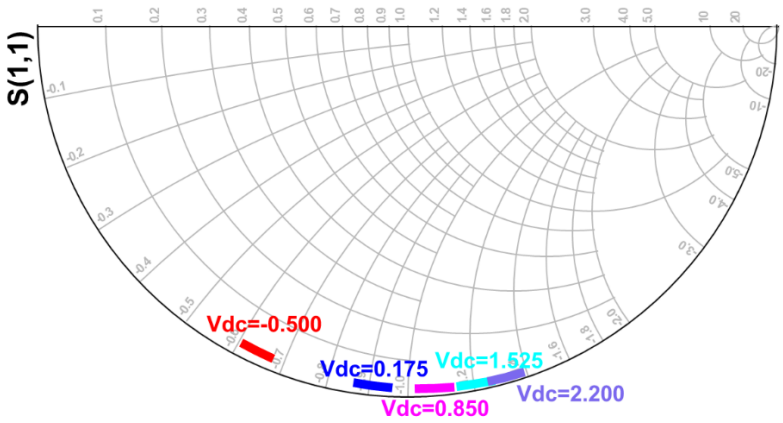



*Figure 4-13 Plot of $S_{11}$ on the Smith Chart of the proposed Varactor*

In Table 4-4 are reported the values of each component used in this design. A spiral grounded inductor of 135 pH is realized to form the LC resonator at design frequency.

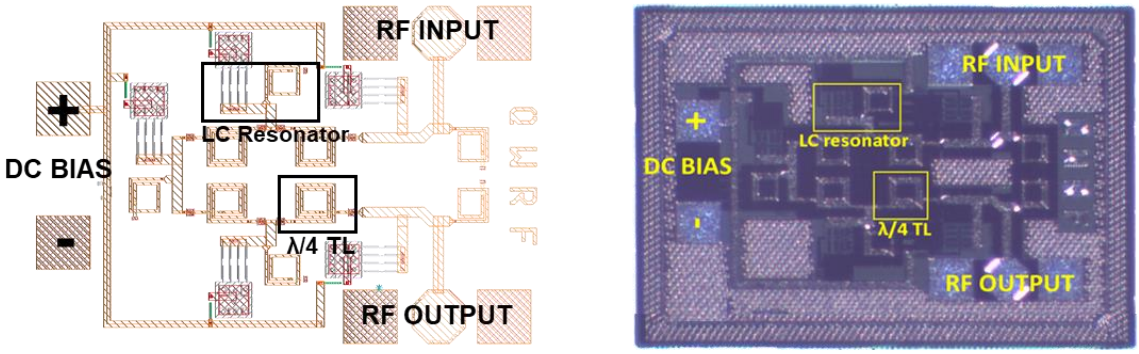
| | |
|---|---|
| $L_{TL}$ | 350 pH Q=12 |
| $C_{TL}$ | 132 fF |
| $DC_{bias}$ | From -0.5V to 2.2 V |
| $C_{var}$ | 1 pF |
| Diode size | 19um x 0.93 um |
| L | 135nH Q=12 |

*Table 4-4 Design component values of QWRF PS*

$L_{TL}$ and $C_{TL}$ are respectively the inductor and capacitance values that has been used to realize the $\lambda/4$ transmission line.

In Figure 4-14a the Cadence layout is shown while in Figure 4-14b a microphotograph picture of the QWRF-PS. The unit cells are folded to produce a more compact layout and to minimize the chip area. The overall size of the chip is:

- PADs included: 500um x 750 um
- PADs excluded: 340um x 650 um




(a) (b)

*Figure 4-14 (a) Submitted layout and a (b) microphotograph picture of the QWRF-PS*

### 4.3.3 Simulation and measurements results of QWRF PS

This phase shifter is implemented using a 0.25 $\mu m$ BiCMOS technology with 5-metallization layers. The average insertion loss at the operating frequency is about 6 dB with a variation of ± 2dB. The measured insertion loss almost follows

the trend of the simulation except in the region of negative bias voltage of the varactor where it shows more losses (Figure 4-15). This problem is due to the wrong modelling of the diodes in the design kit at high frequency.

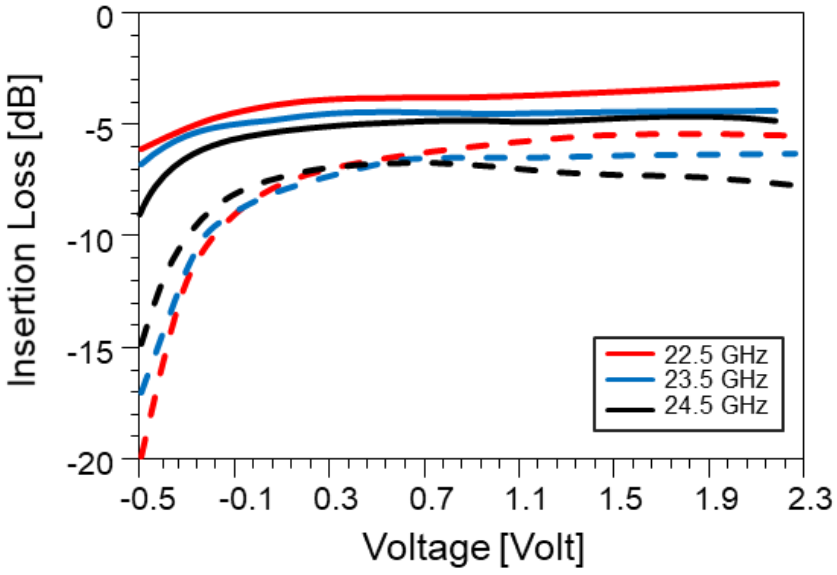



*Figure 4-15 Sim. (solid) and Meas. (dashed) of insertion loss versus bias voltage*

Simulated and measured return losses are exhibited in Figure 4-16. It's shown that in the frequency range from 22.5 to 24.5 GHz the device shows a good matching to 50 ohm.

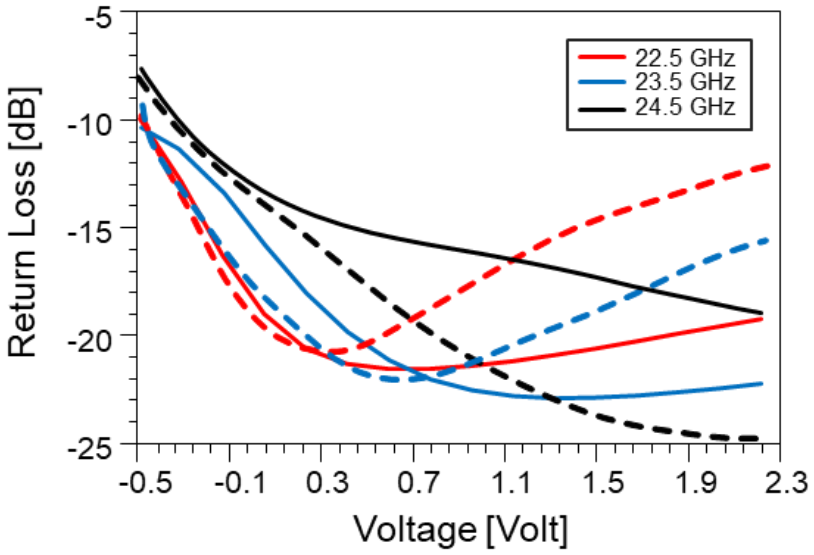



Figure 4-16 Simulation (solid) and Measurement (dashed) return loss versus bias voltage

In Figure 4-17 simulation and measurement results of the phase shifter are reported in the DC voltage range from -0.5V to 2.2V. The measured phase follows the trend of the simulation, but the measured phase shift range slightly reduced. It has been measured at 23.5GHz a phase shift of 150° with an RMS error of 19° (dashed green line in Figure 4-17).

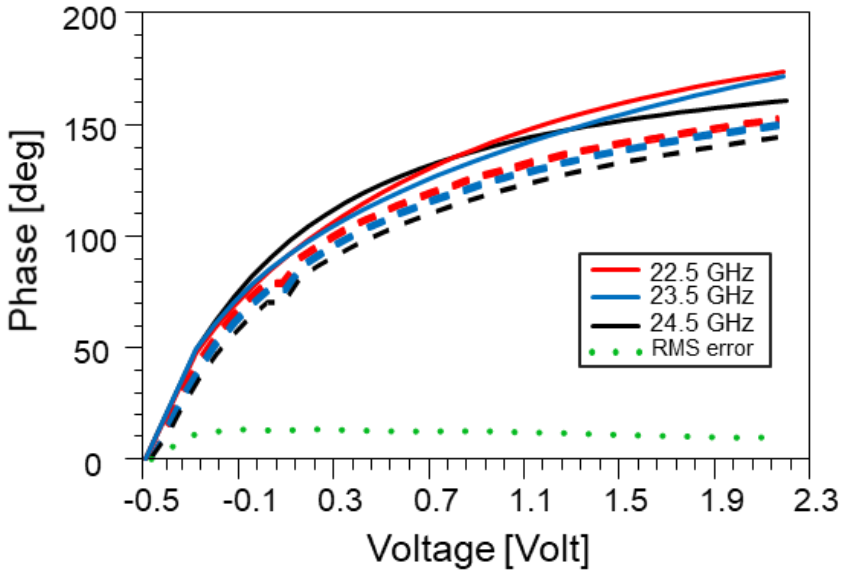



*Figure 4-17 Simulation (solid) and Measurement (dashed) phase shift and RMS error phase.*

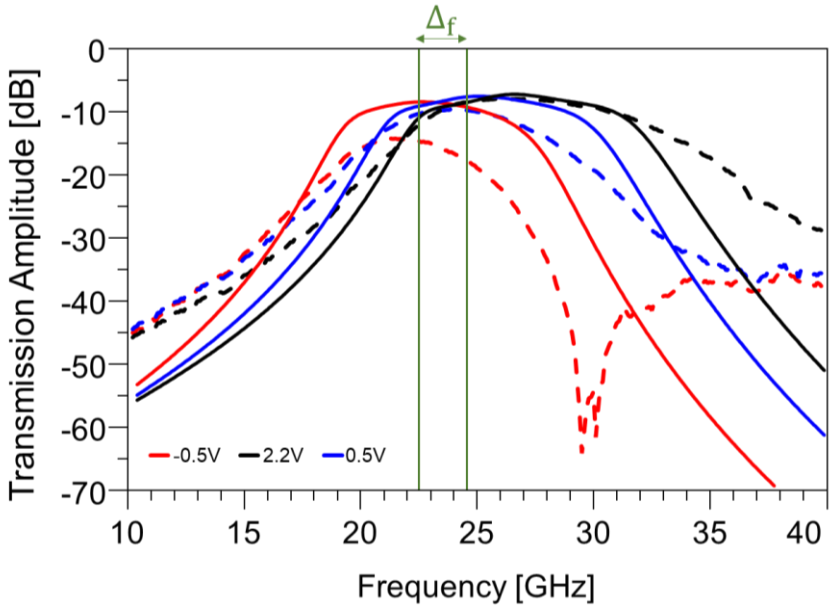



*Figure 4-18 Simulation (solid) and measurement (dashed) of amplitude transmission responses of a QWRF-PS obtained varying varactor diodes voltage feeding*

The transmission amplitude ($S_{21}$) vs frequency is reported in Figure 4-18. The dashed red line represents $S_{21}$ of the QWRF-PS when the bias voltage is fixed at -0.5V. As it can be observed, the band pass shifts by changing the bias condition from -0.5 to 2.2V. A comparison with the state of the art has been done in the Table 4-5.

| | [32] | [33] | [41] | [42] | [43] | [45] | This work |
|---|---|---|---|---|---|---|---|
| PS type | Distributed | Distributed (lumped element) | Distributed | Distributed | Tunable transmission line | Tunable filter | Distributed |
| Technology | 0.13 um CMOS | 0.6 um GaAs | 130nm SiGe BiCMOS | 32 nm CMOS SOI | 45nm CMOS SOI | SiGe | 0.25 um BiCMOS |
| Working frequencies | 5 – 40 GHz | 5 -6 GHz | 26-30 GHz | 55-65 GHz | 45 GHz | 11.5 GHz | 22.5-24.5 GHz |
| Range phase control | 60° at 10GHz | 360° | 190° | 180° | 75° | 360° | 180° |
| IL | 2.6dB ÷ -3.8 dB | 4 dB/± 1.7 dB | 9.3 dB | 3.5-7.6 dB | 3.3 dB | 4.2 | 6 dB /± 2 dB |
| Area | 0.165 $mm^2$ | 0.8 $mm^2$ | 0.18 $mm^2$ | 0.1 $mm^2$ | 0.072 $mm^2$ | 1.5 | 0.22 $mm^2$ |
| Phase error | N/A | 0° | 0.6° | 0.5°-1.2° | N/A | 18° | max 15° |

*Table 4-5 Comparison of tunable phase shifters*

The main feature of the proposed approach is that the PS operating band and the transmission losses can be controlled by design. The principle of operation can be applied to cover wider bandwidths and the insertion losses can be reduced by choosing a different process. From the comparison of the proposed implementation with another PS based on reconfigurable filters [40] it follows that the two designs have an almost equal bandwidth (i.e. about 8%) and similar ILs (7 dB in [40] at 12 GHz). It is interesting to notice that the proposed configuration has better RMS error (3.5° vs. 10°) while it occupies half of the chip area (0.2 vs 0.5 $mm^2$).

# 5. Metamaterials transmission line loaded with a Split Ring Resonator

Since the response of a medium to an electromagnetic field is determined by its properties (dielectric permittivity, ε, and permeability, μ), this allows for the classification of a medium depending on this sign of the constructive parameters. As illustrated in Figure 5-1, media with both permittivity and permeability greater than zero are known as a double positive (DPS) media, a medium with either permittivity or permeability less than zero is designated as ε negative (ENG) medium or mu-negative (MNG) medium respectively. The definition single-negative (SNG) medium can be used in both cases. More interestingly media with negative permittivity and permeability are called the double negative media (DNG) media, following the preceding nomenclature, however, several other terminology have been suggested, such as left-handed (LH), back wave, and negative-refractive index media, a DNG medium has not yet been found in nature to date, and for this reason the most popular metamaterials in the considered classification belongs to the category [41], [42].

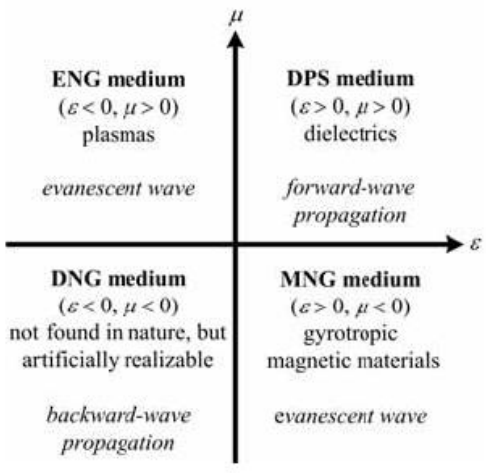



*Figure 5-1 Metamaterials classification according the signs of ε and μ*

## 5.1 *Metamaterials transmission line*

Transmission line metamaterials are a kind of artificial transmission line [41], [42] that consists of a host transmission line loaded with reactive elements, the latter providing high design flexibility in comparison to the conventional line. Specifically, one-dimensional transmission line metamaterials are effectively homogeneous structures whose electromagnetic characteristics can be controlled or engineered to some extent through a specific direction of propagation. After the first experiment verified the left-handed material, many of researches efforts on developing transmission line of metamaterials exhibits the backward propagation [42]–[44] this developing focused on the fact that Maxwell's equations with plane-wave propagation in homogeneous and isotropic media have an identical form as the equations describing the TEM propagation on a transmission line derived using circuit theory, also known as the telegrapher equation. Hence, such an analogy allows the series and shunt elements of well-known ladder circuit model of a transmission line to be related to the constitutive parameters of the medium (exhibiting the same propagation characteristics) by mapping the telegrapher to Maxwell equations the resulting relationship are

$$Z'_s = \frac{Zs}{l} = j\omega\mu$$

$$Y'_p = \frac{Yp}{l} = j\omega\varepsilon$$

Where $Z'_s$ and $Y'_p$ are the distributed per-unit–length series impedance (Ω/m) and shunt admittance (S/m) respectively and Zs and Yp are the per-unit-cell series impedance (Ω) and shunt admittance (S), respectively, and l is the unit cell length.

Accordingly, in conventional RH media, the mapping yields

$$\mu = \frac{L}{l} = L'$$

$$\varepsilon = \frac{C}{l} = C'$$

where $L'$ and $C'$ are the per unit length series inductance (H/m) and shunt capacitance (F/m) respectively, while L and C represent the series inductance (H) and shunt capacitance (F) per unit cell, respectively. The resulting well-known equivalent circuit is shown schematically in Figure 5-2a [42] whose propagation is forward with a propagation constant and characteristic impedance given by:

$$\beta_R = \omega\sqrt{L'C'}$$

$$Z_{cR} = \sqrt{\frac{L'}{C'}}$$

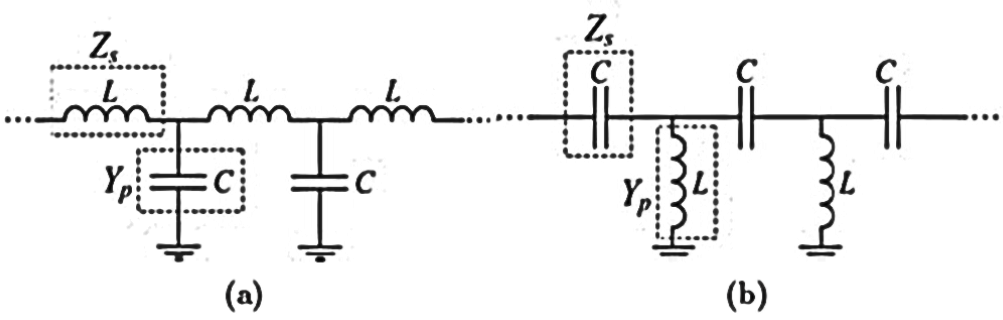



*Figure 5-2 Equivalent circuit model of transmission line (a) Conventional RH transmission line. (b) Dual LH transmission line.(source [42])*

In the transmission line approach of metamaterials this will establish analogy has been extended to the other combinations of the constitutive parameters depending on their sign. Thus for a LH medium the series inductance and the shunt capacitance should become negative according to ($Z'_s = \frac{Zs}{l} = j\omega\mu$). Since from an impedance perspective a negative inductance/capacitance may be interpreted as a positive capacitance/inductance, a ladder network as the one depicted in Figure 5-3 with alternately series-connected capacitors and shunt-connected inductors supports the propagation of backward waves, such a

network is called the dual of the equivalent circuit of RH transmission line. The mapping in this dual network is given by:

$$\mu = -\frac{1}{\omega^2 C'} = -\frac{1}{\omega^2 Cl}$$

$$\varepsilon = -\frac{1}{\omega^2 L'} = -\frac{1}{\omega^2 Ll}$$

Where C' and L' are now the unit length series capacitance and shunt inductance respectively, while C and L stands for the per unit cell series capacitance (F) and shunt inductance (H), respectively. The corresponding propagation constant and characteristic impedance yield respectively.

$$\beta_L = -\frac{1}{\omega\sqrt{L'C'}}$$

$$Z_{cL} = \sqrt{\frac{L'}{C'}}$$

Note that a LH transmission line is intrinsically dispersive by nature because its propagation constant is not a linear function of frequency, in contrast to a dispersion less RH line, it should be also emphasized that the mapping given in ($\varepsilon = -\frac{1}{\omega^2 L'} = -\frac{1}{\omega^2 Ll}$) is valid only in a long wavelength regime, where the period is much smaller that the guided wavelength:

$$\lambda_g = -\frac{2\pi}{|\beta|}$$

Which is defined only in passbands[42], [45] only under this circumstance the definition of effective constitutive parameters is fully feasible and ladder circuit describes properly either a RH or a LH transmission line, by ($\varepsilon = -\frac{1}{\omega^2 L'} = -\frac{1}{\omega^2 Ll}$) or ($Z_{cL} = \sqrt{\frac{L'}{C'}}$), respectively.

Figure 5-3 summarizes the generalization of the aforementioned transmission line approach of the metamaterials by means of the unit-cell equivalent T- circuit models, besides the RH or (DPS) and LH (or DNG) transmission lines, the equivalent circuit of SNG transmission lines are also indicated. It should be noted that waves cannot propagate in neither ENG nor MNG transmission lines because their models are exclusively made of inductors or capacitors. To sum up, the transmission line theory in metamaterials links field to circuit quantities, offering an alternative interesting physical interpretation leading to the same functional results.

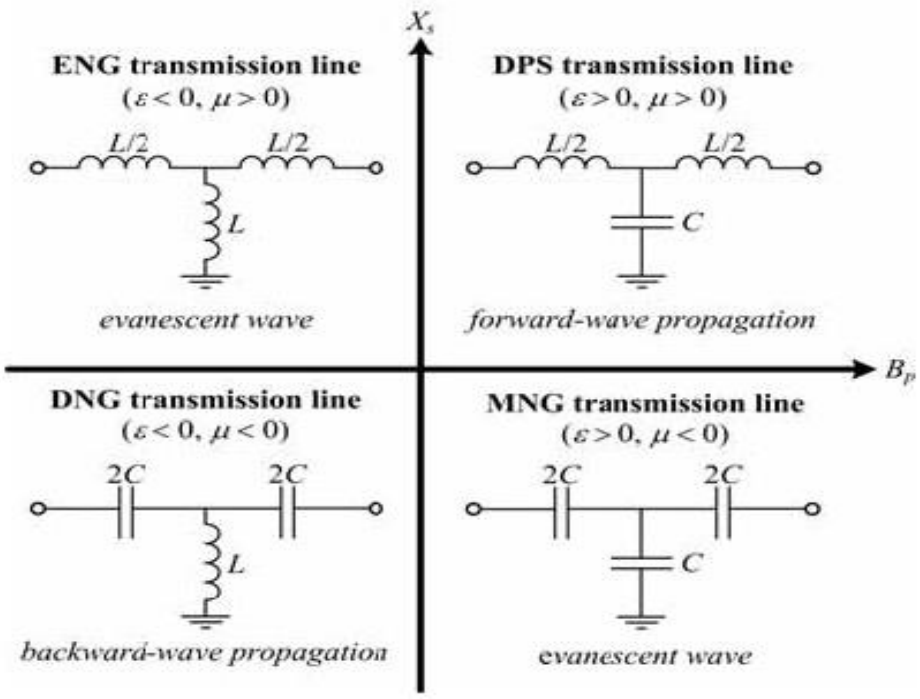



*Figure 5-3 Unit-cell equivalent T-circuit models of the transmission lines according to the sign of the series reactance and shunt suscepetance. (source [42])*

## 5.2 *Metamaterials filters*

The main aim of this section is to highlight the potential of metamaterials and metamaterials-based structures for the synthesis and design of microwave filters. Improved performance and novel functionalities, due to the unique and controllable electromagnetic properties of these structures, as well as device

miniaturization, because of the small electrical size of their constitutive elements, are the main areas where metamaterials concepts may produce a major impact. In the following, several applications of metamaterials will be considered and exhaustively analyzed. As metamaterials are frequency-selective structures by nature, their application to the design of compact microwave filters and duplexers seems to be straightforward.

Because such devices require resonant elements, the preferred (although not exclusive) approach for the synthesis of filters and duplexers based on one-dimensional (1D) metamaterials is the resonant-type approach. SRRs are useful particles for the synthesis of narrowband and wide-bandpass filters (also including bandpass filters for ultra-wide-band— UWB—applications). A systematic methodology for the design of planar filters subject to specifications will be presented.

Probably the most outstanding property of metamaterials transmission lines is the controllability of the electrical characteristics. This includes the dispersion diagram as well as the characteristic impedance of such artificial lines. Owing to this control, it is possible to design components with superior performance compared to conventional implementations (such as enhanced bandwidth devices), components based on new functionalities (such as dual band components), or microwave devices with small dimensions. In such devices, the conventional transmission lines and stubs are substituted by meta-lines, resulting in meta-circuits with smaller dimensions and/or improved performance.

## 5.3 *Split Ring Resonator state of art*

Artificial materials with negative permittivity and permeability, although conceptually introduced by Veselago in 1968 [46], have been experimentally demonstrated for the first time by Smith et al. [44]. In the Smith experiment, the artificial material, also called metamaterial, was implemented through a series of metal wires combined with split ring resonators (SRRs). The direct consequence of simultaneous negative values of $\varepsilon$ and $\mu$ is that the wave vector $k$ and the electric and magnetic field vectors (E and H) form a left-handed triplet generating antiparallel phase and group velocity within a certain frequency band. This feature has been successfully proved in many application domains. Of particular interest is the combination of a left-handed medium with a classical transmission line, which is inherently right handed. In this case, the forward mode propagating though the guided line coexists with a backward mode supported by the left handed medium. Transmission lines where the two effects are combined are usually referred to as composite right-/left-handed transmission lines [47] (CRLH TL). Their unnatural characteristics make it easy to control the properties of the lines, i.e. the input impedance and the phase constant, and to design compact passive structures such as filters [48] [49] [50], antennas with leakage wave properties [51], reconfigurable antennas [52], or phase shifters[53], between other. Although the main research efforts on CRLH TLs [54] have focused on single / multilayer PCB technology, low-temperature co-sealed ceramics or other film technologies often[55], recently, have also been demonstrated for on-chip applications. Examples of inductors and a monolithically implemented CRLH TL cascade capacitors were first proposed on high resistivity silicon substrates for offset applications [53] obtaining 30° out of

phase with a TL length of approximately $\frac{\lambda}{12}$. For a more compact implementation of the monolithically integrated 1-D metamaterial, the resonant-type approach was also investigated by loading a host transmission line with SRR [55]. In general, the implementation of SRRs in monolithically integrated microwave circuits (MMICs) could be detrimental due to the large chip surface requirements. Indeed, to obtain a resonant frequency below 100 GHz, an SRR of about 1 mm would be necessary depending on the specific configuration and technology. However, this limit has been overcome by using stacked split rings as reported in [56] where a configuration based on stacked SRRs coupled with a coplanar waveguide (CPW) was demonstrated on a standard 0.18 $\mu m$ CMOS process exhibiting stop-band behavior at frequencies below 50 GHz. A similar configuration was also proposed using differential transmission lines on 65nm CMOS [57] for applications in the W band.

## 5.4 *Design of capacitively-loaded Split Ring Resonators transmission line filters*

A new configuration of composite Coplanar Waveguide (CPW) for filter applications where the SRR frequency is reduced through capacitive loads is proposed. As it will be shown, the loading effect yields a reduction of the pass-band center frequency of approximately 40% in an SRR loaded CPW line. Indeed, simulated results will show how it is possible to reduce the pass-band center frequency of an SRR-based on-chip filter from around 65GHz to approximately 35 GHz without modifying its size.

### 5.4.1 SRR Coplanar Waveguide

The geometry of the SRR loaded CPW line is shown in Figure 5-4 along with the stack-up of the IHP Microelectronics standard 0.13 $\mu m$ SiGe BiCMOS process taken as reference for this work. The SRR is implemented in the TM1 layer.

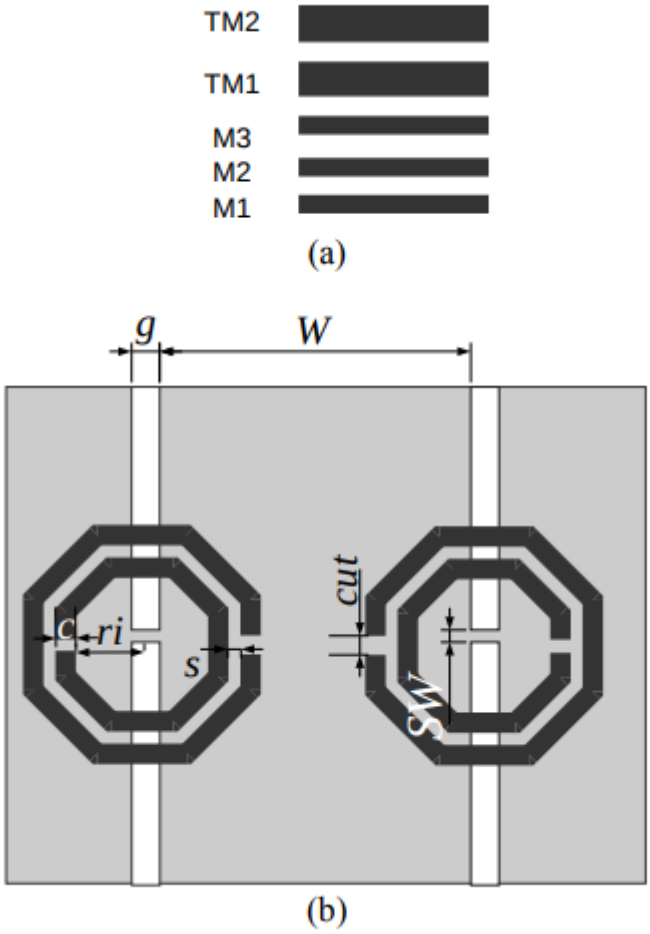



*Figure 5-4 SiGe BiCMOS Split Ring Resonator (SRR) loaded Coplanar Waveguide (CPW) geometry: a) SiGe BiCMOS stack up; b) SRR (TM1) and CPW (TM2) geometrical parameters.*

At variance of standard PCB implementation of metamaterial structures, the shape of the resonators is octagonal as required to better match the design kit rules. The CPW has been located on the top metal layer (TM2) which has a thickness of 3 µm. The CPW line is short circuited through a gap of thickness SW. For the case at hand, the width of the CPW, W, was fixed at 300 $\mu m$ and the gap, $g$, at 42 nm. It's worth noticing that the CPW is ungrounded.

### 5.4.2 SRR-CPW equivalent circuit

The analytical model of the CPW-SSR line has been studied by several scientists. Its most general formulation is reported in [58]. The model proposed in Figure 5-5, derived from this reference, can be divided into two parts. The lower part of the circuit models the CPW line and the input and output ports. In particular, the shorted section of line, $SW$, is responsible of the inductance $2L_p$ that generates a resonant frequency associated with the right hand CPW mode. The lower is the value of the gap $SW$, the lower is the resonant frequency of the right-hand mode. For the process at hand, $SW$ can be lowered down 2 $\mu m$.

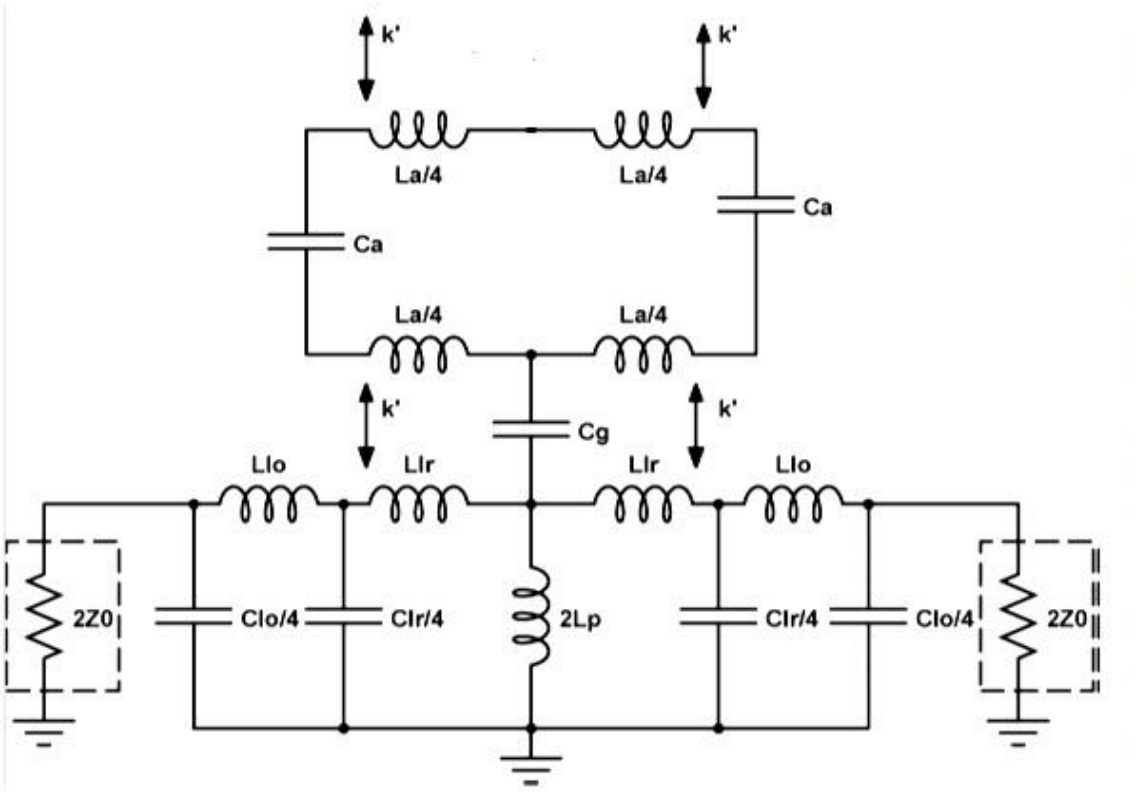



*Figure 5-5 Equivalent circuit of the SRR loaded CPW line*

Lower values are not allowed by the process fabrication rules. The SRR equivalent circuit is represented by the inductances $L_a$ and by the capacitances $C_a$ in Figure 5-5. The inductance $L_a$ is associated to the magnetic current flowing on the SRR while the capacitance $C_a$ is related to the displacement current taking place

between the outer and inner SRR rings. Therefore, the size of the rings, $r_i$, directly affects the resonant frequency of the SRR. Although an analytical model exists [59], the capacitance taking place at the SRR open gaps is usually neglected and it might be included in the model only for special configurations.

### 5.4.3 Design example

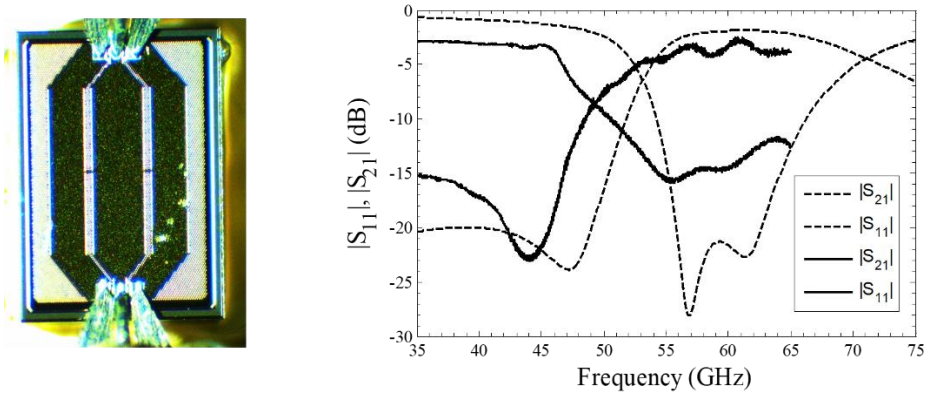
Based on the circuit described in the previous section, an SRR-CPW pass-band filter was designed and tested. The main geometrical parameters are reported in Table 5-1.

| Parameter | Value in um |
|---|---|
| cut | 24 |
| g | 42 |
| $r_i$ | 0.1 |
| W | 300 |
| SW | 6 |
| C | 61 |
| S | 30 |

*Table 5-1 SRR CPW line dimensions*

Simulations has been carried out using a commercial Finite Element Method software. The simulated resonant frequencies of the structure at hand are of about 56.7 and 66 GHz providing a pass-band behavior from 54 to 68 GHz. A prototype of this chip has been fabricated and tested. Measured and simulated scattering parameters are shown in Figure 5-6b. As it can be observed in Figure 5-6a, the feeding lines are two CPW 80 μm which required a transition to match the 300 μm width of the CPW line. The overall chip size is equal to 1. $2mm^2$ while the DUT area is equal to 800×600 μm. The experimental validation has been

conducted measuring the scattering parameters through a manual probe station and connecting the 67A Nichel-based GSG probes to an Anritsu 37397C 65 GHz Vectorial Network Analyzer.




(a) (b)

*Figure 5-6 SRR-CPW line unloaded pass-band filter: simulated*

As it can be seen in Figure 5-6b, simulated and measured results show a good agreement between theory and experiment. Nonetheless, some discrepancies and a small frequency downshift can be observed in the prototyped device which can be partly ascribed to fabrication inaccuracies including layer misalignment and substrate tolerances. Moreover, the probe pads and traces were not included during simulations thus limiting the accuracy of the simulations. The FBW is 19.3% for measurements and 20% for simulation. Measured insertion loss is -3.2 dB and return loss is 14.8 dB at 57.3 GHz. The left-handed and right-handed resonances are observed at 55.5 and 59.5 GHz, respectively. Both resonances are close enough to balance the transmission line thus augmenting the bandwidth of the passband.

### 5.4.4 Capacitively Loaded Split Ring Resonator (SRR)

The next step has been to demonstrate how the operating frequency of the SRR-CPW line can be reduced by capacitively loading the SRR. Metal Insulator Metal (MIM) capacitors, indeed, are readily available in the standard MMIC process

and can be easily integrated in the SRR-CPW line layout. Two different configurations of capacitively loaded SRR-CPW line are has been investigated and, in the following, will be presented the full-wave FEM-based results. In all cases, the geometrical parameters of the structure are the same of the structure presented in Table 5-1 and taken as a reference case. In order to reduce the SRR resonant frequency, a MIM capacitor is used to load the gap of the outer SRR element as shown in Figure 5-7. In this case, the left-handed mode shifts down from 48 to 34 GHz when the capacitor increases from 20 to 80 fF.

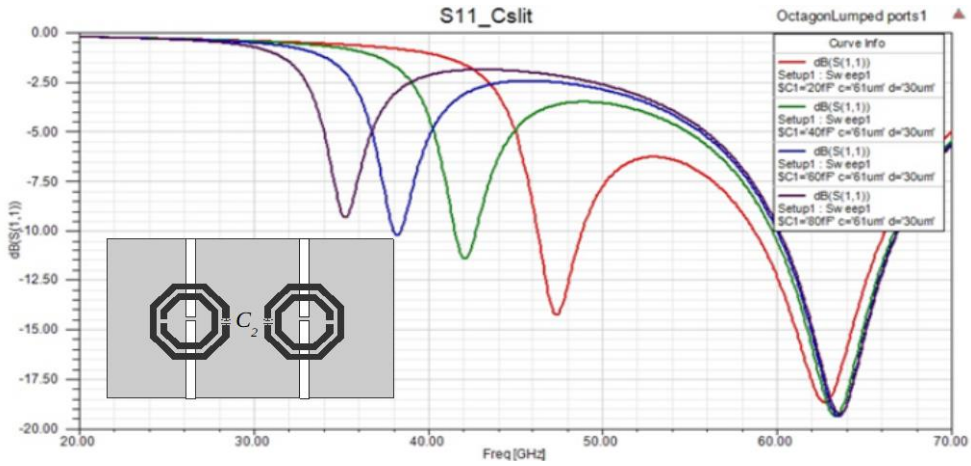



*Figure 5-7 Capacitively loaded CPW-SRR line. MIM capacitor between the outer SRR gap*

In order to obtain a compact-size SRR-CPW line pass-band filter, the configuration of Figure 5-4 was optimized including two MIM capacitors integrated in the gaps of the outer SRR element. The capacitive load reduces the SRR resonant mode (left-handed) whereas the right-hand mode can be reduced by decreasing $SW$. Full wave simulation results of the optimized structure are presented in Figure 5-8. As it can be observed, the filter pass-band frequency can be shifter down to 34-37 GHz without increasing its size with respect to the reference case of Figure 5-6.

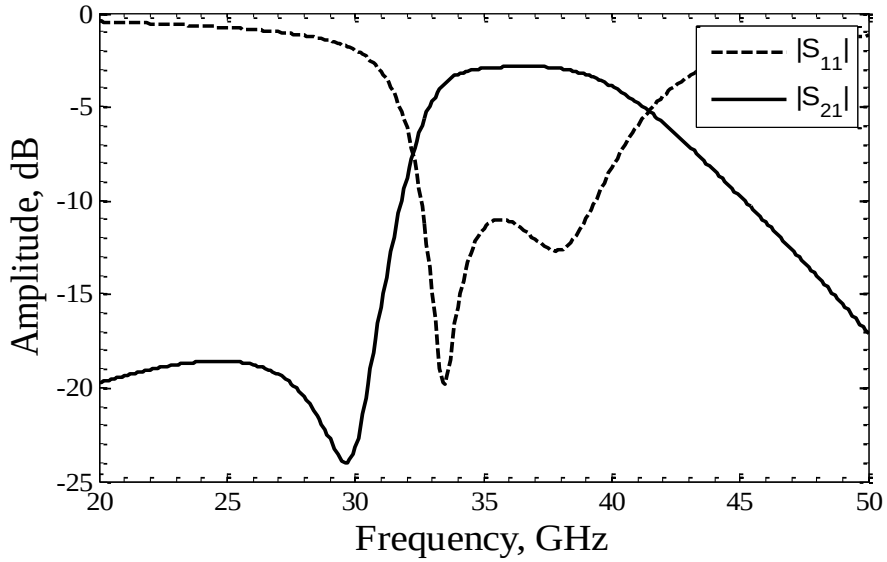



*Figure 5-8 Miniaturized loaded CPW-SRR line: full wave simulated results.*

### 5.4.5 New configuration of the capacitively loaded Split Ring Resonator (SRR)

As it was introduced in previous paragraph, the left-handed and right-handed modes depend on the SRR dimensions and electric coupling occurring in the structure, respectively. Therefore, if the properties of the resonators and the capacitances $C_p$ are modified, the response of the transmission line can be controlled.

This behavior can be easily implemented in MMIC technology by adding three lumped element capacitors which are embedded into the process stack up in the form of Metal-Insulator-Metal (MIM) capacitors. The position and interconnections of the SRR are shown in Figure 5-9

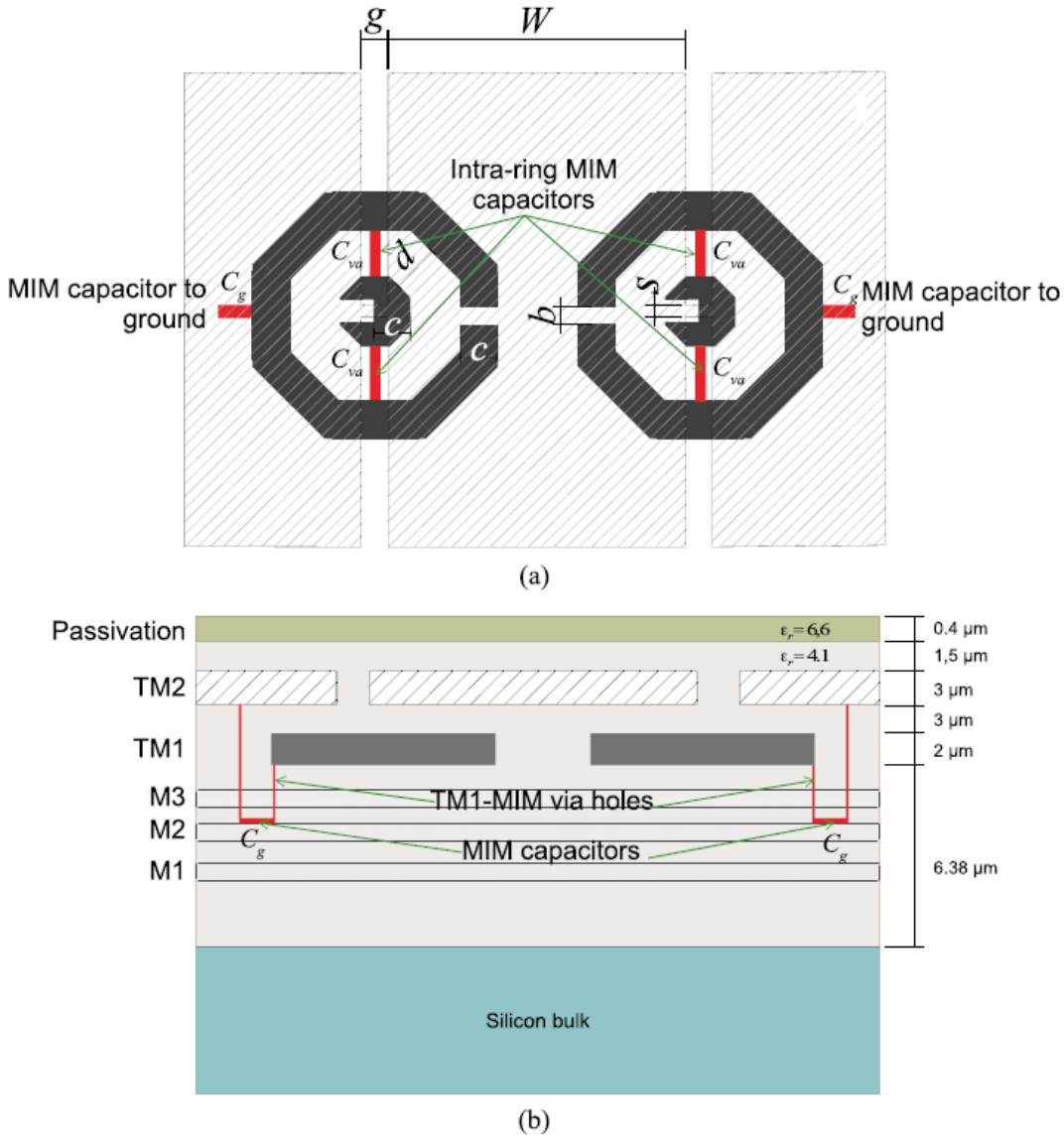



*Figure 5-9 CPW loaded SRRs with lumped capacitors: (a) MIM capacitors shown in the top view; (b) size view including the vertical interconnections from the MIM capacitors, the CPW ground, and the SRRs.*

.

The capacitors denoted as $C_{va}$ are situated between the two rings of the SRR and control the left-handed resonance. On the other hand, the capacitor denoted as $C_g$ connects the outer ring of the SRR with the ground of the CPW and governs the right-handed resonance that appears at higher frequencies. By controlling the values of these lumped capacitors, the frequency response of the CPW line can be shifted down while keeping the initial dimension described in Table 5-1.

The equivalent circuit of Figure 5-5 has been modified to properly model the new configuration shown in Figure 5-9. As it can be observed in Figure 5-10, the new circuital model includes the new capacitances $C_{va}$ and $C_g$. Besides, a new inductance $L_g$ that accounts for the short metal strips and via hole that connect the SRR and the ground is added to the circuit.

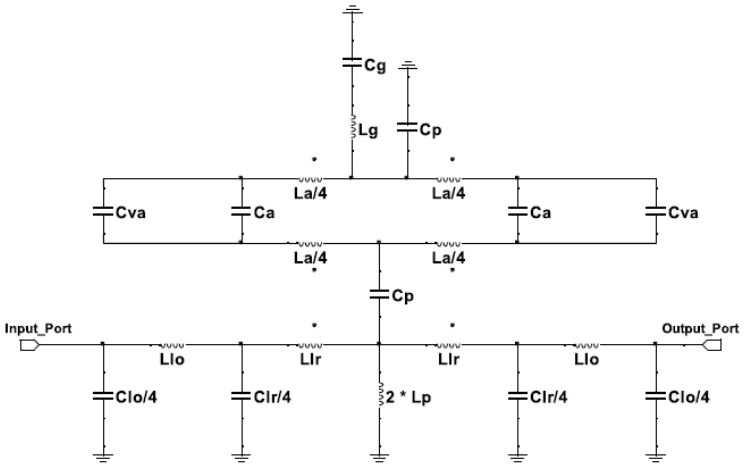



*Figure 5-10 Equivalent circuit of the CPW line and the loaded SRRs.*

The new compact configuration shown in Figure 5-9 has been validated by means of lossless full-wave and circuital simulations with the aim of obtaining the lowest transmitted band without changing the geometry of the SRRs. The values of $C_{va}$ and $C_g$ have been derived from the geometry of the MIM capacitors and are equal to 0.06 pF and 3 pF, respectively. The inductance $L_g$ has been estimated from conventional metalized via holes models. Final values are reported on Table 5-2 while the resulting scattering parameters are shown in Figure 5-11.

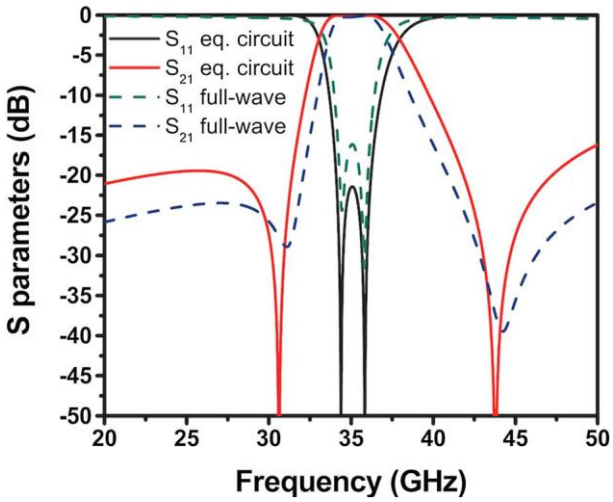



*Figure 5-11 Simulated equivalent circuit and full-wave scattering parameters of the unit cell.*

As it can be observed, the capacitive load allows to obtain a passband at 35 GHz that is 41.6% lower than the response achieved in the paragraph 5.4.4.

| Parameter | ValueC(pF)/L(nH) |
|---|---|
| Clo | 0.02541 |
| Clr | 0.01111 |
| Cp | 0.14664 |
| $C_g$ | 3 |
| $C_{va}$ | 0.06 |
| Llo | 0.0917 |
| Llr | 0.04 |
| Lp | 0.0168 |
| $L_g$ | 0.0285 |
| Ca | 0.04640 |
| La | 0.44 |
| *k* | 0.6384 |

*Table 5-2 Equivalent Circuit Parameters*

It is important to mention that a new transmission zero arises for this configuration. It is due to the LC resonant circuit formed by the new inductance and capacitance $L_g$ and $C_g$. It is worth noticing that the presence of this additional transmission null allows a higher degree of freedom which can be useful not only to control the passband frequency but also to tune the upper out-of-band response of the circuit. Indeed, compared to the response of Figure 5-5, the capacitive loaded SRR show a more symmetric behavior and a sharper Insertion Loss in the upper band thus making this circuit attractive for filter configurations.

### 5.4.6 Capacitive Loaded Split Ring Resonator (SRR) with integration of the varactor

The final step has been to replace the MIM capacitors with variable capacitors (varactor) in order to obtain a frequency tunable transmission line. So, the idea was to check which capacitor (inner or outer capacitors) was more feasible to realize as variable capacitor. Two extra capacitors have been added to the circuit As it shown in Figure 5-12 adding the capacitor $C_{Btwn}$ is like it is going to varying the capacitance $C_a$ already included in the circuit Figure 5-10.

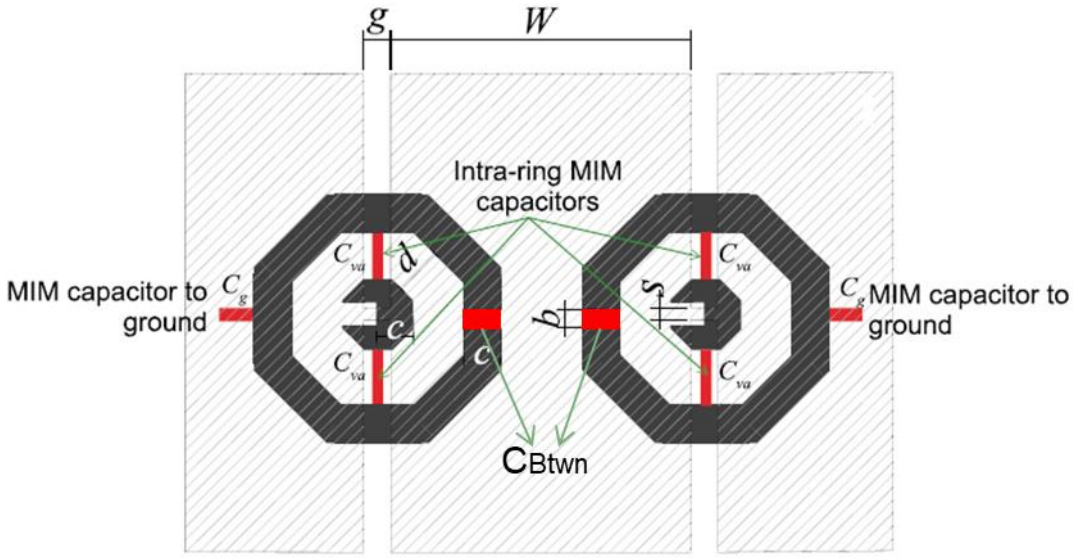



*Figure 5-12 CPW loaded SRRs with lumped capacitors ($C_{Btwn}$)*

The SRR has been rotated by 180° in order to put the varactor instead of the capacitor $C_{Btwn}$ . After a Full wave electromagnetic FEM simulation of the structure it is obtained that a variation of the capacitor $C_{Btwn}$ (85fF → 165 fF) is necessary in order to realize a frequency tunable transmission line (Figure 5-13).

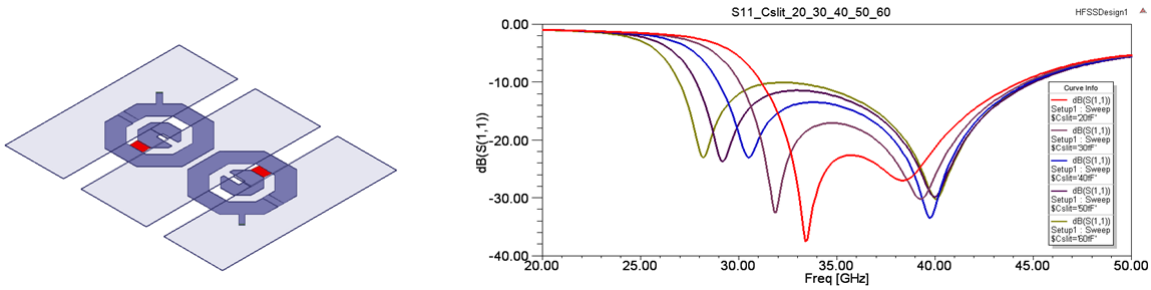



*Figure 5-13 Final layout of SRR CPW and frequency shift changing $C_{Btwn}$*

The last step has been to realize a varactor that provide the same capacitance range of $C_{Btwn}$. To design the varactor, It has been used the same procedure of the paragraph 4.3.2. The C-V and Q-V characteristics are shown in Figure 5-14.

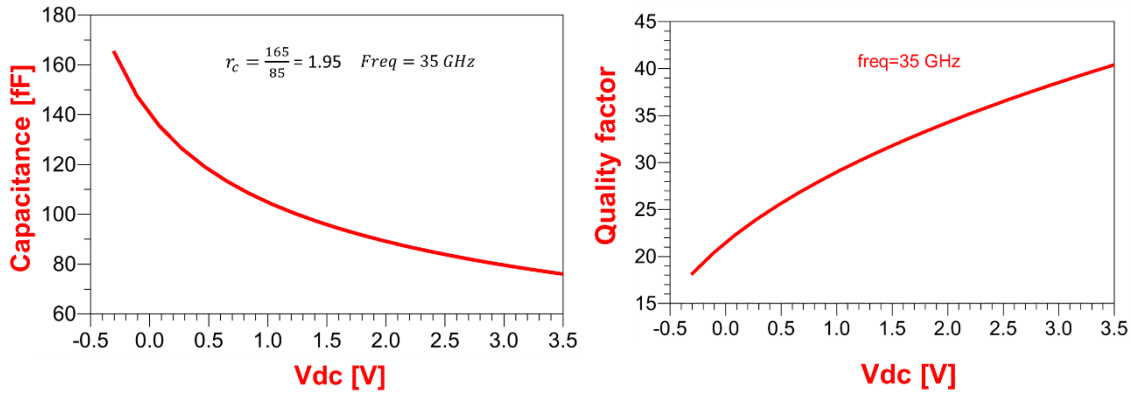



*Figure 5-14 C-V curve and Q-V curve of the varactor designed for the SRR CPW*

Figure 5-15 shown the simulation results obtained replacing the capacitor $C_{Btwn}$ with the designed varactor.

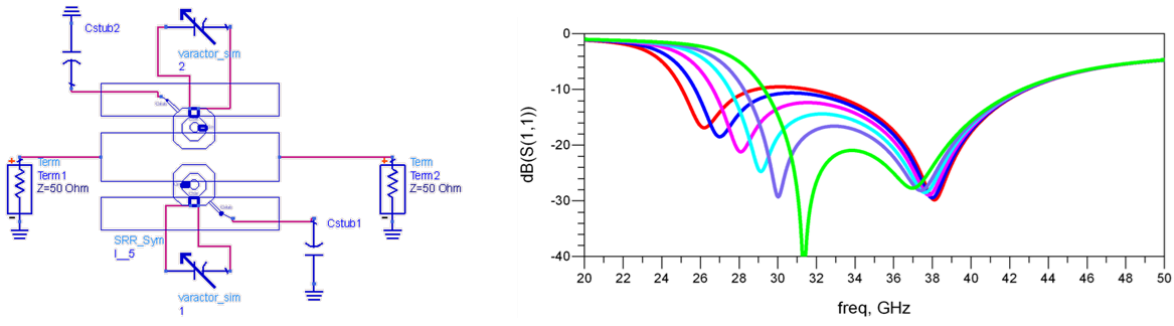



*Figure 5-15 Schematic e return loss of the SRR CPW with varactor*

Unfortunately, regarding this final part of the work there are no measured results, but the realization on SiGe BiCMOS IHP SG25H3 technology is planned in the next run.

# 6. Duplexer for SAT-COM On-the-Move application

KA-Band SAT-COM On-The-Move (SOTM) systems are drawing increasing interests from both governments and companies. Main applications of this technology include two-way wideband communication for commercial and military users on mobile platforms such as aircrafts, ships, as well as trains or other land vehicles [60]. The most compact solution in the design of such devices is achieved when an array of elements (30 GHz Tx and 20GHz Rx) is installed on a shared aperture. This approach requires the integration on the chip of a switching network or a duplexer to feed the radiating elements. Usually duplexer-based solutions lead to better system results allowing the implementation of a full-duplex system. Indeed, frequency division duplex (FDD) transceivers require the simultaneous operation of the transmitter and receiver [61]. There are different approaches which can be employed for the design of a duplexer. In the most general case, two highly selective filters, one centered at the receive (RX) band and the other at the transmit (TX) band, can be designed along with a coupling circuit. Due to the finite isolation of the duplexer, the strong TX signal leaks to the receiver input, desensitizing the receiver through several mechanisms. First, the transmitter noise falling into the RX band raises the receiver noise floor. Second, when the transmitter leakage is mixed with a blocker due to the receiver third-order nonlinearity, the resulting distortion can fall on the desired channel. Third, in a direct conversion receiver, second-order nonlinearity down converts this transmitter leakage to baseband. Finally, reciprocal mixing between the transmitter leakage and the receiver local oscillator (LO) down converts LO phase noise onto the desired signal also causing

desensitization. All these considerations dictate the duplexer isolation requirement in the TX and RX bands on one side, and the receiver linearity, phase noise, and transmitter RX band noise on the other side. A higher duplexer isolation relaxes the noise requirement of the transmitter, and the linearity and phase-noise requirements of the receiver. For example, a TX–RX isolation of 52 dB in the TX band and 45 dB in the RX band is a common requirement for most cellular applications.

## 6.1 *Duplexer state of art*

There are several works in CMOS technology and only one work in SiGe BiCMOS technology.

In [61] a differential hybrid transformer duplexer that covers 3GPP bands I, II, III, and IX between 1.7 and 2.2 GHz is introduced. It achieves a differential to differential isolation of 60 dB in the transmit (TX) band and 40 dB in the receive (RX) band, and a differential to common-mode isolation of 60 dB in both bands. The duplexer with a cascaded low-noise amplifier (LNA) achieves a noise figure of 5.6 dB in the RX path and an insertion loss of 3.7 dB in the TX path. The duplexer and LNA are implemented in a 90-nm CMOS process, consume 20 mA, and occupy an active area of 0.6 $mm^2$.

In [62], a hybrid transformer-based integrated tunable duplexer is demonstrated. High isolation between the transmit and receive ports is achieved through electrical balance between the antenna and balance network impedances. A novel high-power-tolerant balance network, which can be tuned at both the transmit and receive frequencies, allows high isolation in both the transmit and receive bands even under realistic antenna impedance frequency dependence. To maintain high isolation despite antenna impedance variation, a feedback loop is

employed to measure the transmitter leakage and correct the impedance of the balance network. An isolation > 50 dB in the transmit and receive bands with an antenna voltage standing-wave ratio within 2:1 was achieved. The duplexer, along with a cascaded direct-conversion receiver, achieves a noise figure of 5.3 dB, a conversion gain of 45 dB, and consumes 51 mW of power. The insertion loss in the transmit path was less than 3.8 dB. Implemented in a 65-nm CMOS process, the chip occupies an active area of 2.2 $mm^2$.

In [63] an RF duplexer has been fabricated on a CMOS IC for use in 3G/4G cellular transceivers. The passive circuit sustains large voltage swings in the transmit path, and isolates the receive path from the transmitter by more than 45 dB across a bandwidth of 200 MHz in 3G/4G bands I, II, III, IV, and IX. A low noise amplifier embedded into the duplexer demonstrates a cascade noise figure of 5 dB with more than 27 dB of gain. The duplexer inserts 2.5 dB of loss between power amplifier and antenna.

In [64] is presented a wideband integrated RF duplexer supports 3G/4G bands I, II, III, IV, and IX, and achieves a TX-to-RX isolation of more than 55dB in the transmit-band, and greater than 45dB in the corresponding receive-band across 200MHz of bandwidth. A 65nm CMOS duplexer/LNA achieves a transmit insertion loss of 2.5dB, and a cascaded receiver noise figure of 5dB with more than 27dB of gain, exceeding the commercial external duplexers performance at considerably lower cost and area.

The only work regarding the duplexer in SiGe BiCMOS technology is presented in [60]. This work reports the design and measurements of a SiGe BiCMOS duplexer developed for T/R (transmit/receive) Ka-band SAT-COM on-the-move user terminals. The IC presented in this work is designed for the integration in a hexa-core chip for dual-band phased array applications. Due to the particular

configuration of the chip, the duplexer has four ports: one common port, one input port for the Rx channel and two output ports for the Tx channels. The chip size is 570x400 $\mu m^2$ including the measurements pads.

## 6.2 *Design of a duplexer for SAT-COM On-the-Move application*

The goal of the work was to design a duplexer that allows the distribution of the signal at both frequencies 20-30 GHz from a main IN/OUT network (Distribution Network, DN) to all the radiating elements. Figure 6-1 shows the principle of operation of the duplexer.

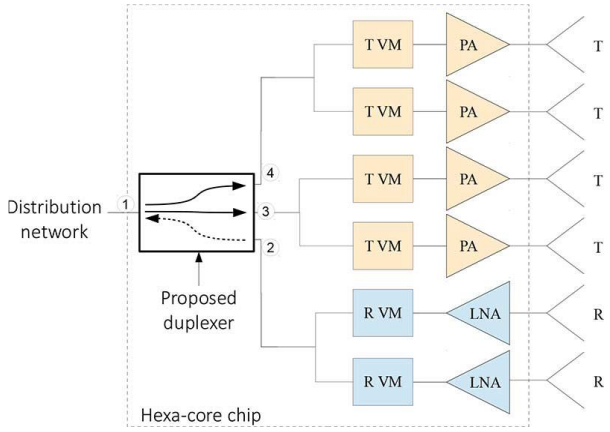



*Figure 6-1 General architecture of a Ka band chip with 6 core (4 Tx and 2 Rx)*

It has been proposed a novel duplexer using lumped-elements elliptical filters to achieve high isolation and multiple Tx outputs, while occupying small area.

The proposed duplexer is a four-port device in which the input signal, received from the distribution network (port 1), is divided into port 3 and 4 and is then used to supply two Tx branches. The remaining port, i.e. port 2, receives the signal from the front-end Rx and delivers it to the distribution network. The method used for the design of a duplexer with an IN/OUT port (Distribution Network) and 3 ports that go towards the branches leading to the antennas through vector

modulators and PA or LNA amplifiers (2 Tx and 1 Rx) will be illustrated in this chapter.

The basic principle that has been thought to adopt is to realize the TX branches (that operate at 30 GHz) with high pass filters while the branch used in RX (operating at 20 GHz) with a low-pass filter as shown in Figure 6-2.

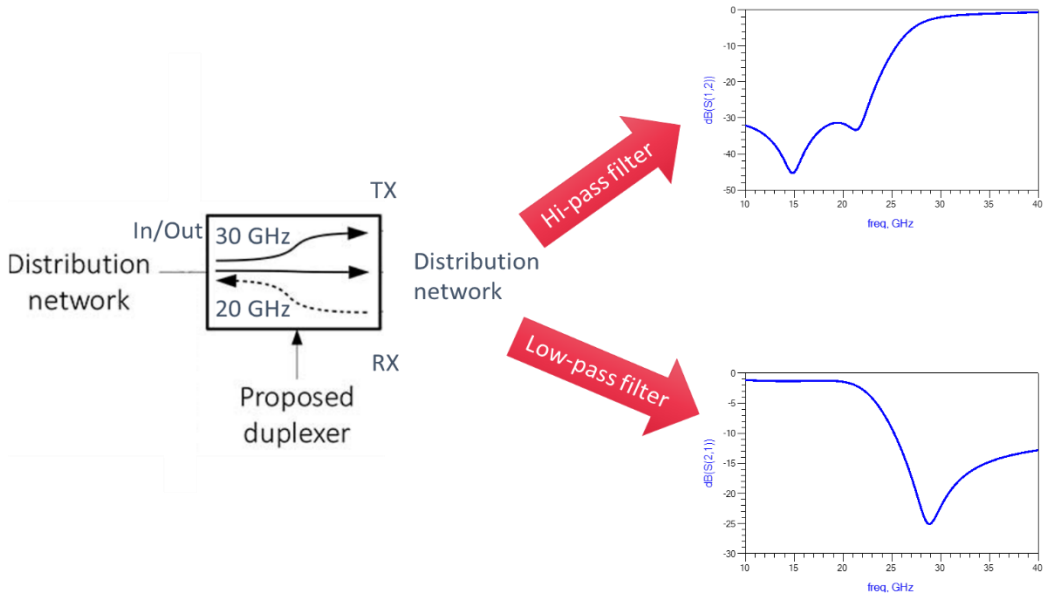



*Figure 6-2 Design of the duplexer using HI/LOW pass filter*

The first design phase involves the synthesis of the filters with the aid of a software to decide the order of the filters. This first phase was carried out using an Ansys Electronic Desktop Designer tool. It was decided to use lumped element elliptical filters of the fifth order. The resulting schematic is shown in Figure 6-3a.

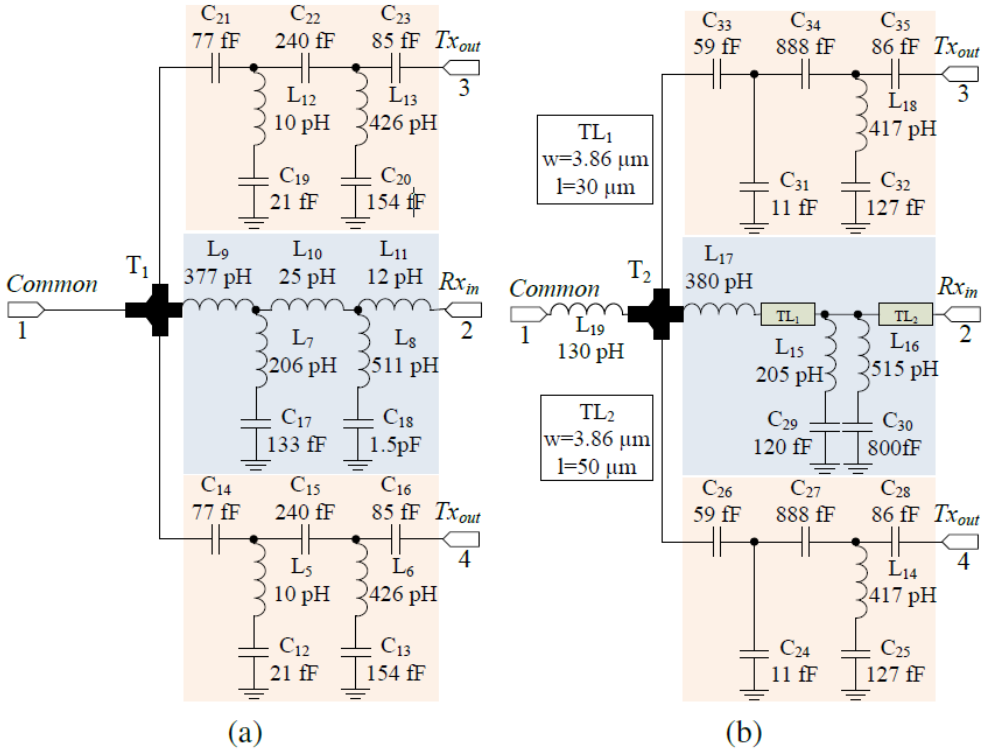



*Figure 6-3 Duplexer equivalent circuit. (a) Schematic and (b) layout optimized.*

Next, a circuit simulation of the entire duplexer was carried out, connecting the filters (High and Low pass) to the distribution network.

From a first analysis the duplexer on the distribution network side is not matched.

The Tx branches of the duplexer comprise fifth-order high-pass elliptical filters. At 30.15 GHz, if a 50-Ω load is presented to the Tx-out ports, the filter input impedance magnitude is approximately 100 Ω, hence the two of them in parallel approaches 50 Ω. At 20.35 GHz, the same filters have very high input impedance acting like an open. The Rx branch comprises a fifth-order low-pass elliptical filter. Analogously, at 30.15 GHz and 20.35 GHz the filter has a very high and a near 50 Ω input impedance, respectively. A T-junction combines the three filters into a single node. Thereby, in both TRx BWs the input impedance seen at the common port is near to 50 Ω and, due to the open behavior of other channels' filter, ideally, the signals flow only between the common and intended ports.

Subsequently, the components were optimized using full wave electromagnetic simulations in ANSYS Electronics to consider the layout parasitic. As shown in Figure 6-3b, L5 and L12 has been removed because the interconnection between the capacitors are almost enough to implement the required 10pH. The inductances L10 and L11 were implemented as narrow transmission lines (TL1 and TL2). The TL1, which substituted L10, was placed before the resonator L15-C29 without much detriment to the Rx transmission coefficient. Thereby, some spatial separation was added between the inductors to prevent from coupling. The components were then optimized for the new configuration and the input impedance was tuned by L19 to improve the return loss at the common port.

The final layout generated in Advanced Design System (Keysight) is shown in Figure 6-4a. SiGe BiCMOS 0.25 $\mu m$ technology is used to realize the layout. Figure 6-4b shows the final layout of the device in a 3D view generated in ANSYS HFSS. The final size of the circuit is only 224 $\mu m$ x 306 $\mu m$.

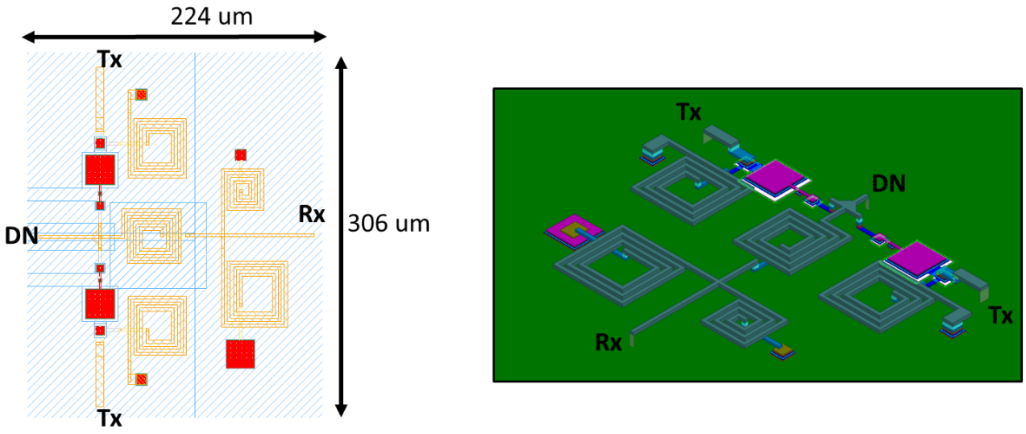



*Figure 6-4 Top view and 3D view of the final layout of the designed duplexer*

Full wave simulation of the overall structure has been done in HFSS and the results are shown in Figure 6-5. The results show that the circuit has a good matching on all IN/OUT ports. The losses on the individual branches, are lower than 2dB at the working frequencies (2.3 dB on the Tx branch and 1.4 dB on the

Rx branch). Isolation (<25 dB) was guaranteed between the Rx branch and the Tx branch around the working frequencies of 20GHz and 30GHz.

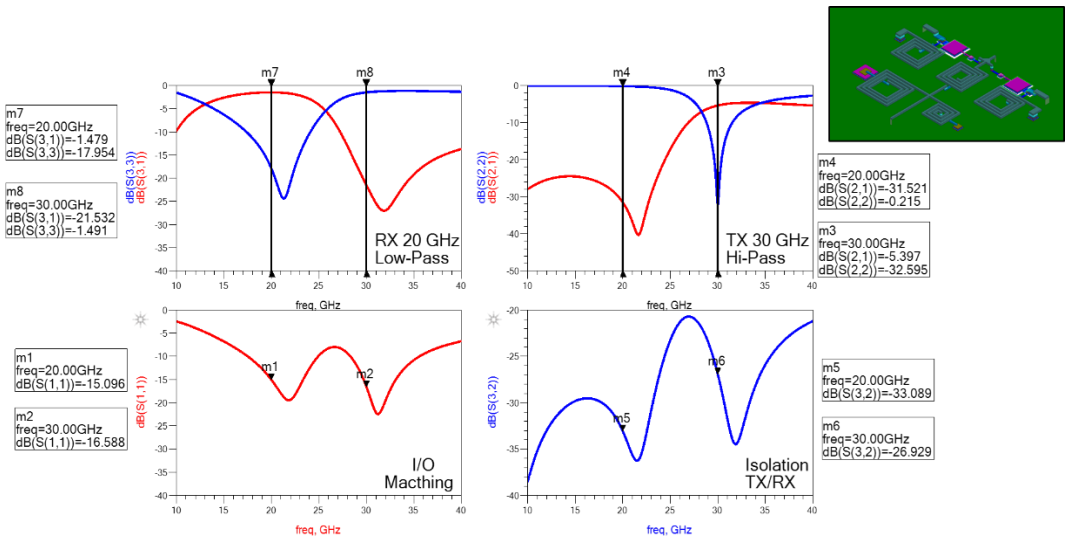



*Figure 6-5 HFSS simulation results of the designed duplexer*

In HFSS, sensitivity analysis has been performed on the possible sensitive elements of the circuit (principally by varying the geometrical parameters of the inductors). Lastly, an optimization of the layout was carried out, evaluating the minimum distance between the inductors, in order to check that no coupling is generated between the various branches of the circuit.

In addition, an input matching study was performed in the distribution network. It was designed to operate as a matching circuit at both 20-30 GHz frequencies. Elliptical filters are able to achieve higher isolation if compared with Butterworth counterparts of the same order. The chosen filter and the above-mentioned modifications led to a very compact duplexer with 304um x 309 um total area, representing only 41% of the area of the previous version presented in [65].

### 6.2.1 Measurement and simulation comparison

Two port measurements have been performed terminating the other probe with a 50Ohms load. Due to the symmetry of the TX paths, one output was terminated

with a 50Ohms resistor on-chip. As a drawback, isolation between the TX Paths could not be measured, but this is not a critical point.

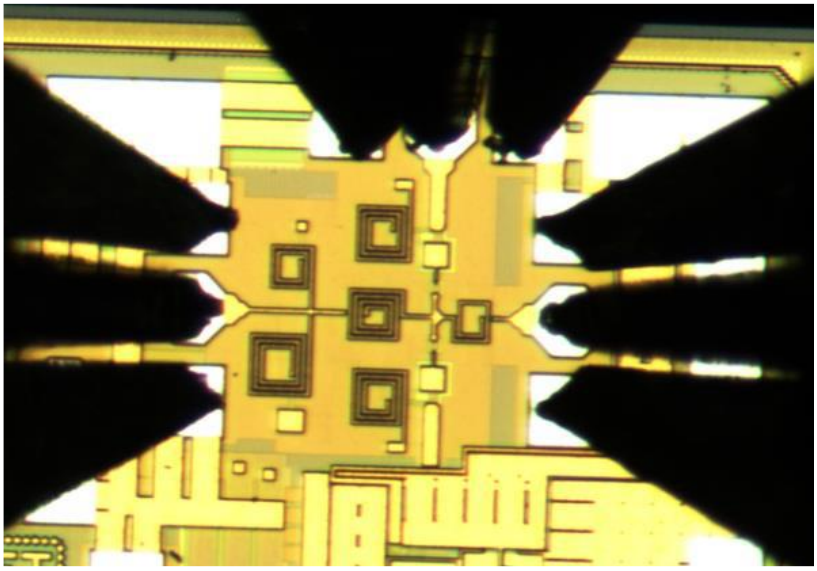


*Figure 6-6 Microphotograph picture of the duplexer*

VNA Configuration:

- 10 to 40GHz, 50MHz
- Output power: -5dBm, no power slope

In the following images, always the thick red line are simulations results while the others are de-embedded measurements.

In the plots below 3 samples were measured:

- Port 1 – 4 are simulation results
- Port 5 – 8 are Sample 1 results
- Port 9 – 12 are Sample 2 results
- Port 3 – 16 are Sample 3 results

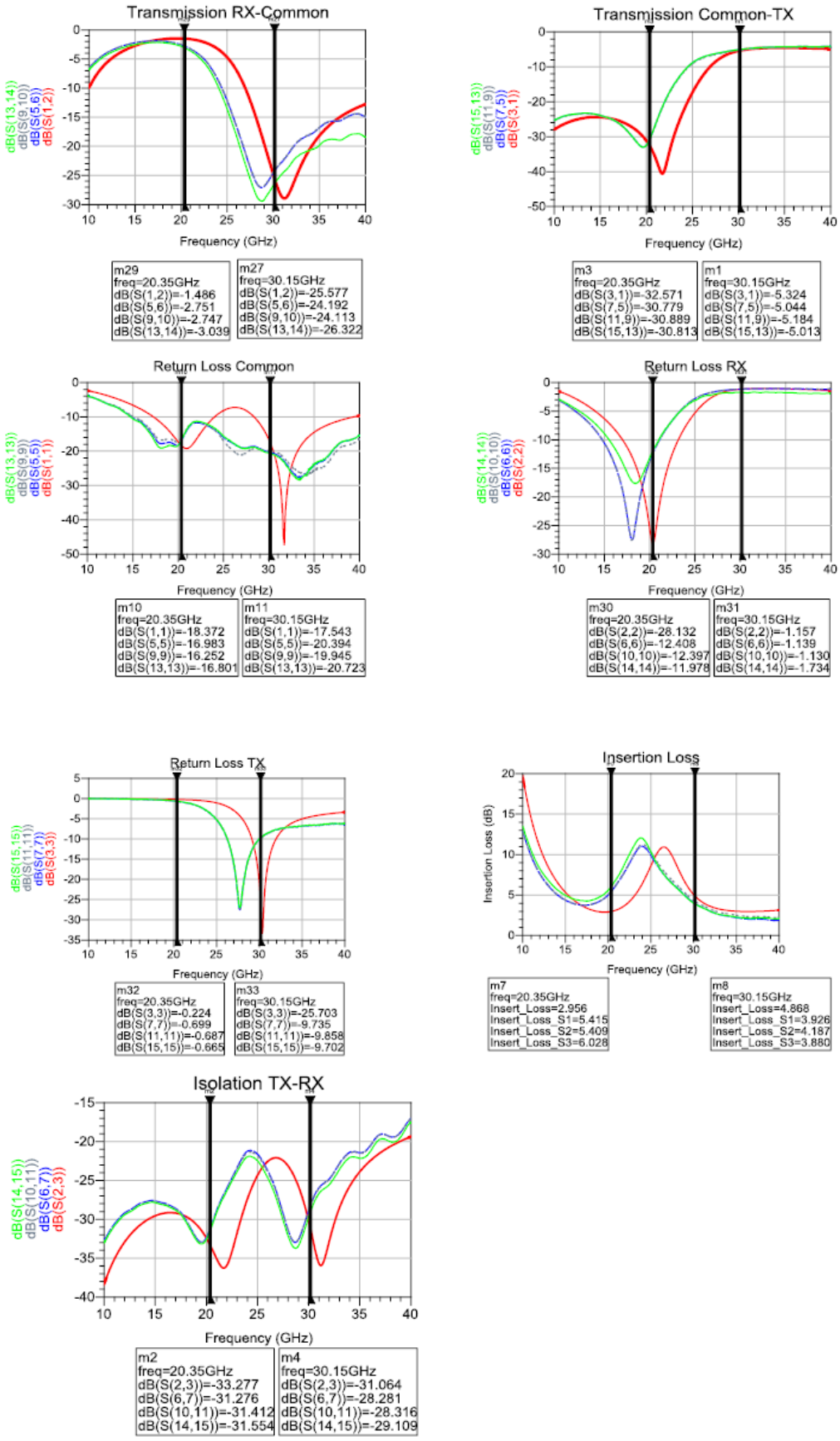



*Figure 6-7 Measured and simulated results of the designed duplexer*

The measured isolation is above 28.9 and 26.3 dB inside the Rx and Tx BWs, respectively. At frequencies in between, the isolation reaches the minimum of 21.2 dB at 24.1 GHz. The |S12| is above -3.3 dB in its bandwidth of interest while the |S31| is above -5.3 dB including the 3 dB of the power division. At the Rx and Tx frequency bands, RLs better than 13.7 and 19.9 dB are obtained at the common port. The shift towards smaller frequencies observed in the measured results affected the return loss at port 3.

It is observed a shift of about 3GHz to lower frequencies on the measured results. This shift had as main impact the reduction of return losses and increase the insertion loss at the RX bandwidth.

### 6.2.2 Comparison with the state of art

The only work that is comparable with the designed duplexer is the [60], because is the only one realized on chip with SiGe BiCMOS technology and with the similar architecture. In Table 6-1 the comparison of this work with the state of art. Remarkable, the reduction of the occupied chip area and the improvement of the isolation. In fact, with this design it has been obtained a reduction of the overall size of the occupied chip area of 32% and isolation improved at 20 GHz from 12 dB to 29 dB and at 30 GHz from 20 dB to 29 dB.

| *Ref.* | *Technology* | *Area [mm²]* | *Freq [GHz]* | *IRL [dB ]* | *ORL [dB]* | *Isolation [dB]* | *IL [dB]* |
|---|---|---|---|---|---|---|---|
| *[60]* | *0.25 µm BiCMOS* | *0.1* | *20 Rx<br>30 Tx* | *15 Rx<br>10 Tx* | *13 Rx<br>8 Tx* | *12 Rx<br>20 Tx* | *3.1 Rx<br>5.4 Tx* |
| *This work* | *0.25 µm BiCMOS* | *0.068* | *20 Rx<br>30 Tx* | *17 Rx<br>20 Tx* | *12 Rx<br>10 Tx* | *33 Rx<br>31 Tx* | *1.4 Rx<br>5.3 Tx* |

*Table 6-1 Comparison of designed Wilkinson Power combiner/divider with the state of art*

# 7. Conclusions

In this thesis, the possibility of designing and realizing various circuits for 5G applications was investigated proposing new design concepts and validating them through experimental assessments. All the proposed components are directly or indirectly referable to 5G application scenarios. The aim of the proposed work is to implement several building blocks for reconfigurable antennas and phased arrays in SiGe BiCMOS technologies. In particular, an 8x8 Butler matrix was designed in SiGe BiCMOS 90 nm technology (BiCMOS9MW of ST Microelectronics) operating at 24 GHz. The matrix was integrated on a PCB test board (with wire bonding technique) to be measured. Finally, two Wilkinson power combiners / dividers were presented in Ka band (20GHz and 30GHz). They were designed with the same approach employing lumped elements and achieving a simple and compact design in SiGe BiCMOS 0.25$\mu m$ technology (SG25H3 of IHP Microelectronics). The measured results show a phase imbalance of 1° and 0.1 dB of amplitude imbalance. Insertion loss is less than 2 dB (1.9 in Rx case and 1.5 in Tx case).

Moreover, a new phase shifter architecture based on a pass-band filter was investigated. The proposed configuration is based on half-wavelength coupled filters and it was manufactured in SiGe BiCMOS 0.25$\mu m$ technology (SG25H3 of IHP Microelectronics). The measured results show a phase shift of 150° at the centre working frequency with an RMS error that results in an average of 19°. Return loss demonstrates that the circuit is well matched in the whole band but due to the limited accuracy of the pin diode in the Ka-band, experimental insertion losses are much higher than the simulations.

Another topic addressed in this research work is the possibility to realize CPW-SRR structures in a standard SiGe BiCMOS process for pass-band filter applications. In a first part of the work, SRRs coupled to a CPW structure were reviewed and their equivalent circuit was described and implemented using Agilent ADS. The validity of the equivalent circuit implementation was proved by comparing the ADS results with full-wave simulations. In a second part of the work, an implementation of the SRR-CPW in the SiGe BiCMOS 0.25*um* IHP process was presented. A 60 GHz pass-band MMIC filter based on metamaterials was taken as a reference presenting its geometry as well as the lumped element model and the full-wave EM simulation results. Moreover, the main effort was to introduce new type of SRR configurations capable to down-shift the pass-band frequency of the SRR-CPW structure without increasing its size. Thanks to the usage of capacitive loads, it was possible to reduce the center band frequency of a CPW SRR configuration from 60 to 35 GHz without increasing its size.

Finally, a duplexer for K/Ka SAT-COM on the Move application was designed. This device has 4 ports: 1 common port, 1 port for Rx signal and 2 Tx ports. The proposed duplexer was implemented adopting a high-pass and a low-pass filter section for each Tx and Rx section respectively. Both filters were designed taking as a reference a lumped circuit model which was then mapped in SiGe BiCMOS through an on-chip lumped element network. An impedance study of the input matching network was performed and the distribution network was designed to operate as a matching circuit at both 20-30 GHz frequencies. The final layout was implemented in SiGe BiCMOS 0.25 $\mu m$ technology (SG25H3 by IHP Microelectronics). The final results exhibited an isolation between the ports of more than 30 dB while the chip area was reduced of about 40% with respect to other similar works.

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