BUILDING BLOCKS FOR SIGE BICMOS MULTICORE CHIP FOR KA-BAND SATCOM ON THE MOVE USER TERMINALS

by

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BUILDING BLOCKS FOR SIGE BICMOS MULTICORE CHIP FOR KA-BAND SATCOM ON THE MOVE USER TERMINALS

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ABSTRACT

This project presents building blocks for an innovative configuration of reconfigurable Ka-band Tx/Rx SatCom user terminal antenna operating in the 29.5–30.8GHz and 19.7–21.0GHz bands. The proposed approach is based on a low-profile active phased-array implemented integrating a multilayer printed circuit with reconfigurable SiGe BiCMOS MMICs. The radiating part of the array is implemented employing dual band elements arranged in an interleaved configuration. Each radiating element is equipped with one complete Tx/Rx unit. Chips developed for this project are referred to as “intelligent pixels” as they integrate all the RF analogue, mixed-signal and digital control circuitry. Each multiple Tx and Rx cores which can independently operate amplitude and phase control, as it is required to implement 2-D beam steering arrays. Furthermore, power amplifiers, Power divider, vector modulator, switching network and low noise amplifiers are embedded into each transmit and receive core respectively to fulfill link budget requirements for Sat-Com applications. In the proposed configuration, each SiGe BiCMOS MMIC chip controls 2 Rx and 4 Tx antenna elements.

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Author Alireza Shamsafar

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DEDICATION

This thesis is dedicated to my lovely wife Elnaz Abaei, my father Rasoul Shamsafar and my mother Nahid Baradaran Hossieni who they help me a lot during these years.

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CHAPTER 1

INTRODUCTION

1.1 Introduction of Ka-band systems

The Ka-band is the band that covers the frequencies of 26.5–40 GHz [1] [2] and it is part of the K band of the microwave band in the electromagnetic spectrum.

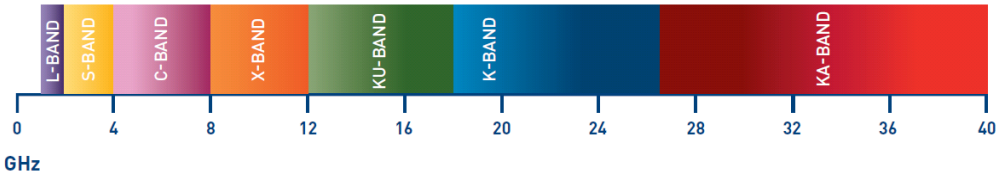

Figure 1-1: Frequency spectrum.

The 30/20 GHz band is used in communications satellites, uplink in either the 27.5 GHz - 31 GHz bands. Ka-band has become the band of choice for many satellite operators due to its increasing capacity availability and its applicability for broadband services. The higher frequency enables the satellite spot beams to be much smaller than those typical of Ku-band. In turn, this enables the frequencies for each beam to be re-used in different spot beams without risk of interference. This significantly increases the capacity of the satellite. The latest Ka-band satellites have 38 times the data capacity of a comparable

Ku-band satellite. The increasing interest for Ka-band satellite communications systems is mainly due to the following features:

1. **Large bandwidth**: this is the base reason for developing Ka-band satellite system in the time that lower frequency bands are congested.
2. **Small antenna size**: with respect to Ku-band systems, user terminal antennas can be designed to have a reduced size thus resulting in a reduction of the interference from adjacent satellite systems.
3. **Larger system capacity**: Ka-band satellites provide smaller spot-beams to increase the satellite power density and allow large frequency reuse, which help to have higher spectrum occupancy. Many user terminals can use the service simultaneously.
4. **Ubiquitous access**: accesses are available at any point inside the satellite footprint especially in locations where wired network are impossible or economically unfeasible.
5. **Flexible bandwidth-on-demand capability**: this characteristic maximizes the bandwidth and resource utilization, and decrease the cost to end users.

The main commercial applications operating in the Ka-band are the following[3]: emerging Voice over IP (VoIP)[4], tele-medicine, tele-education, voice, local television, VSATs, "home-use VSATs", satellite news gathering, and military intelligence. Such services are being implemented on different networks of satellites; some of them are already in orbit, such as:

- Astra 3B (2010, EADS Astrium), 4A, 1L (2007, Lockheed Martin);
- HotBird 6 (2002, Alcatel Space)

- O3b Satellite Constellation (2013-2014, Thales Alenia Space)
- Inmarsat 5 Global Xpress(2014, International Maritime Satellite Organization)
- Viasat-1 (2012, Viasat)
- Eutelsat 3D (2014, Eutelsat)

Some of the civil services that are already offered or will be offered in the near future in connection with these satellites include internet services (e.g. ViaSat, Astra2Connect, Tooway, InmarSat) or TV broadcasting (e.g. DVB-S2).

One of the most interesting and promising application of Ka-band sitcom systems is related to their use in mobile platforms such as airplanes, trains or trucks. In this context, one of the most critical aspects is related to the development of the phased‑array antenna system. Indeed, as it will be clarified on Chapter 2, antenna requirements for Sat-Com user terminal are usually very challenging. Typically, it is required beam scanning over very wide angles, low interactions with the environment, dual band (Tx and Rx) operation, low-cost and low-profile.

In the most typical approach, these requirements are satisfied by employing two separated radiation apertures for the Rx and Tx channel. Pointing of the two dual-polarized antennas is usually mechanical in azimuth and electronically steered in elevation. This approach results in a complex antenna architecture which can be hardly mounted on vehicles or airplanes without affecting their aerodynamic and aesthetic profile. Furthermore, the cost of this solution remains high even for mass production. Arrays with full electronic beam scanning were proposed using customized GaAs (MMICs)[5][6]. Although this is a step in the right direction, it is still not enough to greatly reduce the cost of the user terminals. Indeed, independent silicon chips will be

required to control Tx and Rx modules and it is not possible to integrate multiples cores in the same MMIC with high yield.

This work introduces a new configuration of Ka SatCom user terminal antenna as it is being developed within the framework of the European FP7 project (FLEXWIN) [7]. The proposed configuration is based on highly reconfigurable RFIC components referred to as "intelligent pixels" combined with a quasi-planar antenna array. Each element of the array is therefore integrated with a multicore chip developed on the SiGe BiCMOS technology, where amplitude and phase control elements are integrated with environmental sensing and digital controls controlled through a I2C bus. The IHP (Innovations for High Performance Microelectronics) SiGe SG25H3 MMIC technology was employed in this work. This process provides a 0.25 μm technology with a set of npn-HBTs ranging from a higher RF performance (fT/fmax= 110 GHz/180 GHz) to higher breakdown voltages up to 7 V.

In terms of re-configurability, this approach proposes to achieve a significant advance towards smart RF micro-systems enabling the realization of highly reconfigurable and multifunctional millimeter-wave building blocks which can be integrated with environmental sensing blocks and with digital controls.

1.2 Thesis organization

In this thesis design and characterization of building blocks for a multicore chip for Sat-Com Ka-band applications will be presented. System driven requirements will be described in Chapter 2. MMIC process details will be given in Chapter 3 along with a description of passive and active components employed in the proposed designs. Satcom

user terminal with electronic beam scanning and some details on the antenna array configuration will be reviewed in Chapter 4 along with link budget considerations. In Chapter 5 the design of Low Noise Amplifier (LNA) for Tx branch will be shown and the measurement results will be compared with simulations. CMOS switches and their design and limits for the application at hand will be presented in Chapter 6 introducing a new configuration for Rx/Tx switching network based on CMOS single switch. The ability to control amplitude and phase of each array element will be achieved using Vector Modulators (VM) which is presented in Chapter 7. The multicore configuration requires the use of on-chip Beam Forming Network (BFN) whose main building blocks are power combiners which will be presented in Chapter 8. As an alternative to switching networks, a diplexer network was designed and tested as shown in Chapter 9. For the characterization of the multicore chips specific test boards have been designed and prototyped as described in Chapter 10. This chapter will also provide a summary of the hexa-chip measurements.

CHAPTER 2

KA-BAND SATCOM SYSTEMS

2.1 A Ka-band systems

The term Ka-band system is not just related to the operating band but it is recognized as a shorthand term for a new generation of communications satellites that encompasses a number of innovative technologies such as on-board processing (OBP) for multimedia applications[8], and switching to provide full two way services to and from small ground terminals[9]. To do this efficiently, multiple pencils like spot beams are employed and, in some cases, inter-satellite links are also used [10]. Apart from the conventional geo-stationary orbit; both low ground and middle ground orbit systems have been planned[11]. Ka-band satellite systems have also been known as multimedia satellites or ATM satellites or broadband switched and broadband interactive satellites. The multimedia and ATM are generally inaccurate as Ka-band satellites can be used for other applications than multimedia or ATM platform. The term "ATM Satellite" is also incorrect because on-board switching can involve either ATM switching or circuit switching or both. In other words on-board processing and switching are already employed in satellites providing mobile communications to handheld receivers.

There are several experimental Ka-band satellites such as ITALSAT (Italy), ACTS (US), DFS (Germany) and Olympus (European Space Agency), as well as commercial

communications systems, to help solving the problem of saturation of the available orbital slots at C and Ku-band and also to provide new services for different type of users[12].There are many challenges for using Ka-Band SatCom systems that depend on the application context. One of the most interesting Ka-band applications is related to the establishment of high capacity links for users in a mobile platform such as an airplane, ship, train or truck. For this application, the most critical element in the system is the user terminal antenna which must be designed to reach several critical requirements such as:

- interactions with the aircraft aerodynamics which mainly results in changes of drag and lift and which can be extremely critical with dish antennas;
- very wide angle scanning performance, e.g. operation on polar routes;
- uninterruptible communication links, whatever the trajectory, aircraft man oeuvres and flight attitude;
- operate at both frequency bands (up-link and down-link);
- costs due to antenna architecture (active phased arrays) or manufacturer monopoly.

An ideal antenna architecture, capable to meet all previous requirements, would consequently bring decisive advantages over existing solutions by combining the following capabilities:

- broadband data transmission capability in transmit and receive operation;
- low profile and low weight;
- big coverage areas enough to guarantee service availability on all main flight routes;
- advanced beam steering capabilities;

- low cost;

It is widely known that active phased array antennas are likely the most promising candidate to fulfill many of the above mentioned challenges, except for the cost aspect. Furthermore, the design of a compact, fully integrated phased array at Ka-band poses several technological challenges which have not been yet fully solved. For this reason, mechanically steerable parabolic reflectors are still used in many Ka-band systems, even on the move platforms. There are some efforts have been made to fabricate electronically or mechanically tracking terminals. As a result, there are three main options for the design of a Ka-band user terminal antenna:

- fully mechanical;
- electromechanical;
- fully electronic.

2.2 SatCom user terminal antennas

Mobile SatCom systems introduce new complexities in the design of on move terminals antennas. The direct line-of-sight between antenna and satellite antenna requires the antenna to see from horizon to overhead (zenith – 90) in elevation and 360 in azimuth angle, with total hemispherical coverage. This is actualized in the case of transceiver antenna through the application of moveable rotatable high-gain antennas to attain full coverage.

The moveable antenna itself imposes even more stringent requirements. Therefore, in spite of constant vibrating, pitching, rolling and yawing the Mobile SatCom antenna’s narrow radiation beam must be pointed accurately to satellite.

Since 1970, satellite communications developed quickly aiming at replacing HF radio with the new Fltsatcom military mobile system. For instance, since this time several types of UHF antennas developed were used, such as the crossed-dipole array, its improved version and the so-called wash-tube similar to an SBF antenna and one type of SHF parabolic dish antenna. However, the first real global Mobile SatCom system was the Marisat system, which used SES and L-band antenna systems similar to current Inmarsat-A and B terminals.

Mobile antennas have to satisfy the requirements of some characteristics in relation to construction strength, easy installation and cost. Easy installation and appropriate physical shape are very important requirements in addition to compactness and lightweight. In the case of moveable SatCom antennas, the installation requirements are strongly depend on application and place to install for example to that of aircraft and cars is different with ships because even in small ships there is a enough space to install an antenna. Otherwise, the only problem is because all types of ships satellite antennas are sometimes under stress from vibration and sloping caused by storms, rolling and pitch or is subject to corrosion by salt. To avoid these problems, a ship’s antenna has to be protected by plastic cover (radome) and properly installed on a strong mast, which is suitable for a certain size of antenna. However, in the case of road vehicles, especially small cars, low profile and lightweight equipment is preferred. In the case of aircraft, more conditions are required to satisfy standards. Such as low air drag that is one of the most important requirements for aircraft antennas. Vehicles and aircraft need smaller and more aerodynamic antenna. Several different type of antenna can be used in array to provide a desired radiation pattern. This type of antenna is called an array antenna that

consist of more than two elements; this can be done by different types of antennas, such as microstrip, cross-slot, cross-dipole, helixes or other antennas elements and is suitable for move able SatCom systems. Each element of an array antenna can be excited by different amplitude and phase to obtain desired radiation pattern.

The pointing direction of the SatCom user terminal antenna can be defined in terms of azimuth and elevation angles:

- Azimuth Angle – The azimuth is the angle between North line and horizontal satellite direction as seen from the antenna, as shown in Figure 2-1. Thus, the actual azimuth angle for the various satellites due to the antenna's (airplane) plotted position can be found.
- Elevation Angle – The elevation angle is the satellite height above the horizon as seen from the antenna, as shown in Figure 2-1. In this case, the actual elevation angle for the various satellites due to the antenna's (airplane) plotted position can be found.

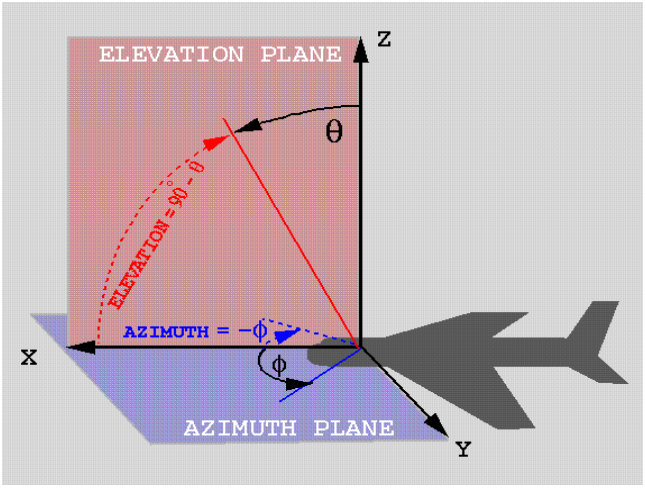

Figure 2-1: HGA Coordinate System. (www.matis.net)

2.2.1 Fully mechanical pointing

In this category of antennas we put the type of the antennas whose beam is steered directions (elevation and azimuth). The main challenge is that these user terminals antennas need a precise mechanical pointing system to point precisely at a defined satellite in the sky [13]. The ITU (International Telecommunication Union), FCC (Federal Communications Commission), ETSI (European Telecommunications Standards Institute) and other regulatory agencies have very strict alignment requirements for satellite antennas in order to avoid interference. The pointing for Ka-band user terminal antennas require to point a target in the sky that is too small [14]. Despite these challenges, many companies have successfully developed “mechanical” antenna terminals that have been used on a wide variety of mobile systems. The first fully mechanical pointing antenna was developed more than 30 years ago [15]. Fully mechanically pointing is used usually for reflector antenna parabola antenna and etc. However they have some disadvantages that include:

- Cost
- Large form factor
- Weight
- Power usage
- Difficult to install

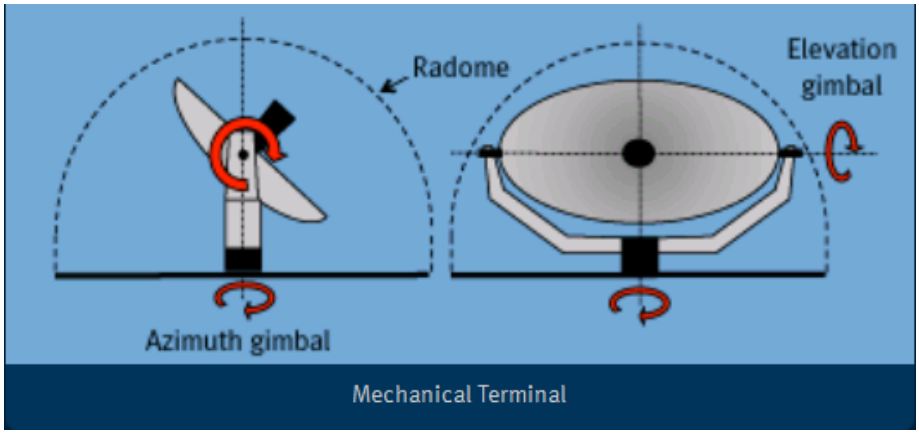

Figure 2-2: Mechanical Antenna pointing (www.kymetacorp.com).

The mechanical pointing systems that can be described by the following set of parameters

- Pointing resolution is defined as the minimum antenna beam movement step in azimuth or elevation;
- Sensitivity is defined as the beam changing in direction per unit of actuator adjustment;
- Hysteresis (backlash) span is defined as the difference between actual beam direction for a given actuator setting position after being approached with two opposite directions;
- Lock-down shift is defined as the azimuth-elevation vector changes when the locking fasteners are tightened after all final adjustments have been made.

The main error sources are:

- Absolute azimuth and elevation errors are defined as the difference between the scale readings and the absolute values of azimuth and elevation.
- Boresight-axis misalignment use to asymmetric antennas that is defined as the angular difference between the optical boresight and the skew axis of rotation that

may occur caused by a different factors such as reflector shape errors, accuracy of mounting points of the reflector, and feed position errors.

- Vertical plumb error is known as the difference between the azimuth axis of rotation and the local vertical axis. This usually occurs because of foundation or base pole being not perfectly leveled.
- Beam squint for circularly polarized antennas, is defined as plus and minus half of the difference between the LHCP and RHCP main beam directions. The squint angle is on the order of +/- 0.15^{o} step for an antenna.[16]
- Moreover the above static errors, sources of dynamic error change by time. They include:
- Wind deflection. One of important physical design point of the antenna is stiffness against reflector wind load versus cost, weight, and complexity.
- Unequal solar heating of the reflector antenna. At different position of sun, the shadow of the edge of a large reflector can take a long time to traverse the width of the reflector. During this time, the sunlit portion of the reflector dissipates greater solar heat load than the shadowed portion.
- Foundation settling is known as changes vertical plumb error over time.
- Station keeping is defined as small changing of the satellite with respect to the earth.[17]

2.2.2 Electronic elevation and mechanical azimuth pointing

One of efficient way to point the beam of the antenna in satellite communication is to use hybrid pointing methods (e.g. electromechanically steerable antennas). It means that in one direction the antenna can be routed mechanically and in other direction electronically. Mechanical routing to cover azimuth direction can be done by router or mechanical arm. In elevation beam steering can be done by changing the phase and amplitude of feeding. The goal of this procedure is to keep the beam direction on the desired satellite.

Viasat aero mobile terminal 2540/2532 is an example of this type of antennas that operate in Ka-band and can be mounted permanently on fuselage of aircraft. The array is Ka-band dual polarized horn array and Rx/Tx integrated circuit embedded into the aperture to increase the gain of array as shown in figure 2-3.

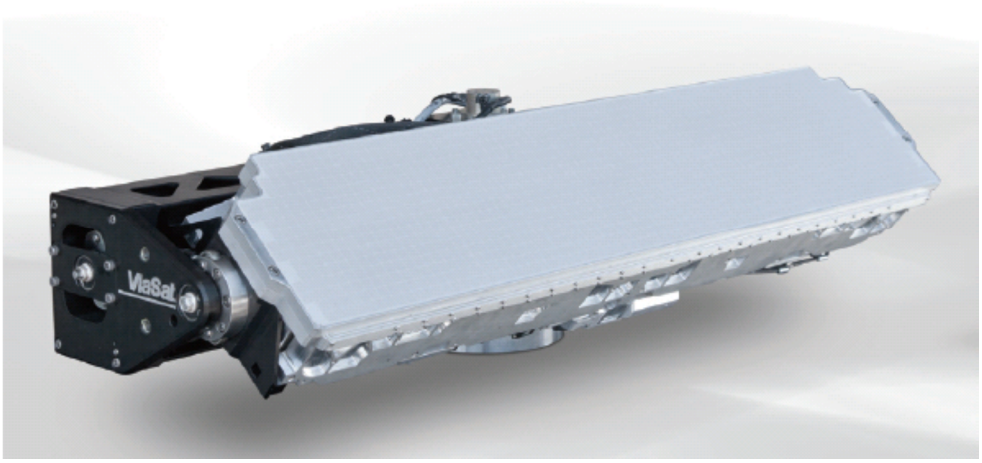

Figure 2-3: Viasat aperture array antenna.(www.viasat.com).

Maximum weight of this antenna is 34 kg and the maximum height is 0.22 m. It consume 180 W from the 48v DC power supply that cause antenna gain-to-noise-temperature (G/T) around 12.5 dB/K. Azimuth coverage of this antenna is from 0 to 360 degree and

Elevation coverage is from 0 to 75 degree. Tx mode frequency band is 28.1-30 GHz and Rx operate from 18.3 to 20 GHz. The overall antenna cover with plastic cover (radome) and connected to power supply and modem unit as shown in figure 2-4.[18]

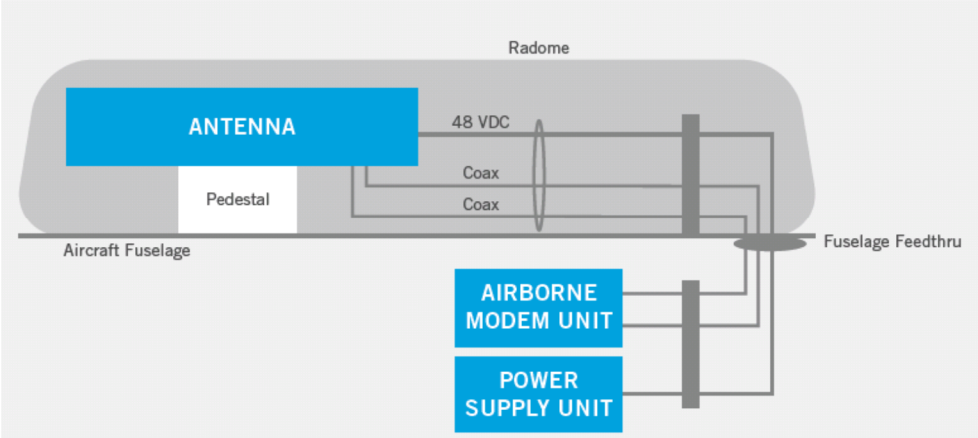

Figure 2-4: System diagram of Viasat antenna.(www.viasat.com).

2.2.3 Other emerging trends

One of the emerging need for SatCom on the move systems is related to the possibility to have a user terminal antenna flat, easy to fabricate and to calibrate and less expensive than the systems currently in use. The configuration which is most well suited for these requirements is based on fully-electronically scanned antenna arrays. Electronic pointing has some advantages that are listed below:

- high gain width less side lobes;
- ability to switch the beam to from one target to other target in a few microseconds;
- ability to provide an directive beam under computer control;
- free eligible Dwell Time.

On the other hand fully electronically beam pointing has some limits and disadvantages that are:

- the coverage is limited to constant degree steps in azimuth and elevation;
- deformation of the beam in the case of deflection;
- low frequency agility;
- very complex structure (processor, phase shifters);
- still high costs;

Example of existing electronically beam pointing is a VICTS antennas with digital beam forming network. Thin Kom's VICTS antenna technology provide a broadband, low profile, and effective cost for on -the-move connectivity challenges. Thin Kom's VICTS antennas can steer 360° in azimuth and 90° in elevation, allow us to have continuous and reliable tracking for all users' needs and is compatible with DBS providers. Satellite internet and other satellite data streaming needs can be realized with thin Kom's VICTS antenna technology. The VICTS antenna is shown in Figure2-5. [19]

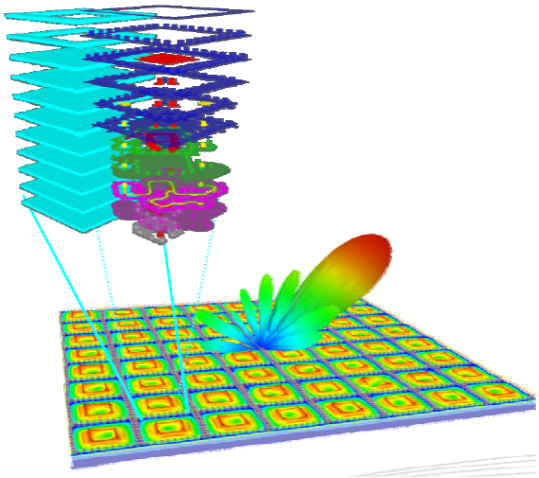

Figure 2-5: LTCC frontend antenna circuitries (IMST GmbH, Germany).

2.3 Objective of the thesis

In this thesis, a fully electronic beam scanning solution for Ka-band user terminals is investigated. The proposed configuration is based on printed radiating elements combined with multi-core SiGe core chips which enable full control of amplitude and phase on each element of the array.

For many years, the main emphasis of SiGe MMIC development was on demonstrating individual function blocks, showing that typical GaAs MMIC components such as low-noise amplifiers, up- or down-converters can also be fabricated on Silicon substrates. However, it turns out that for small and medium volumes, the cost of Silicon-based MMICs is actually higher than for their GaAs counterparts. This has to do with the more complex technology and hence larger number of mask levels, with the larger sizes of Si wafers (which can be a curse for small markets), and also the higher minimum number of wafers per batch in Silicon processing.

The true advantage of Silicon-based MMICs appears when increasing complexity. Here, Si/SiGe BiCMOS as well as RFCMOS benefit from

- The higher processing maturity and yield,
- The higher thermal conductivity of Silicon vs. GaAs (1.5 vs. 0.46 W/cmK at 300K) which allows much denser on-chip packing of active components.
- Suitable for low noise applications such as LNAs due to better noise behavior vs GaAs

CHAPTER 3

IHP 0.13UM SIGE BICMOS PROCESS TECHNOLOGY

3.1 MMIC Introduction

A Monolithic Microwave Integrated Circuit or MMIC is an integrated circuit (IC) operating at microwave frequencies (300 MHz to 300 GHz) which active and passive components are fabricated on one semiconductor substrate. Due to monolithic characteristic, MMICs as fabricated as small parts of whole semiconductor wafer. MMIC wafer is shown in figure 3-1. The process of the wafers is forming of micrometric or even nanometric features on their surface. Because of this reason fabrication process is costly and time consuming. MMIC technology provides the core components for many applications of microwave and telecommunication. There are some advantages of applying MMIC technology that listed below [20]:

- Cheap in large quantities, especially for complex circuits
- Good reproducibility
- Small
- Light
- Less parasitic
- Larger bandwidth

MMICs were usually fabricated using gallium arsenide (GaAs), an III-V compound semiconductor. GaAs has two advantages as compare as Silicon (Si), the usual material for IC realization: device (transistor) speed and another one is semi-insulating substrate. Both of them help to design of Microwave frequency circuit functions. However, the speed of SiGe-based technologies has increased as transistors feature sizes have reduced and MMICs can now also be fabricated in SiGe technology. The advances in silicon transistor performance from 1998 to 2004, for both the MOSFET and the Silicon Germanium (SiGe) HBT processes, coupled with the high integration density of five to seven metal layers, have allowed high performance MMICs to be developed at microwave and even millimeter-wave (mm-wave) frequencies. For the SiGe technology, the transistor maximum (unity gain) frequency *ft* in standard commercial runs increased from 40 to50 GHz in 1998 to >200 GHz in 2004 [21]. By 2005, M/A-COM completed the development of an automotive SiGe 24-GHz radar transceiver with 2 GHz of instantaneous bandwidth [22], and IBM demonstrated a 60-GHz short-range communication system capable of handling more than 3 Gb/s [23]. In 2003 and in 2005, the Army Research Laboratories and Defense Advanced Research Projects Administration (DARPA) asked [24]: Silicon RFICs be used to lower the cost of phased arrays for defense applications, especially at X/Ku/K-bands and also at mm-wave frequencies, while still maintaining all the functionality (noise figure (NF), power, bandwidth, etc.) of phased arrays are challenging.

In order to design MMICs, it is necessary to have precise characterization/ modeling of elements (mainly FETs) and impedance analysis based upon it, circuit design suitable to

monolithic integration, and element and device fabrication technology appropriate to microwave frequencies and above [25].

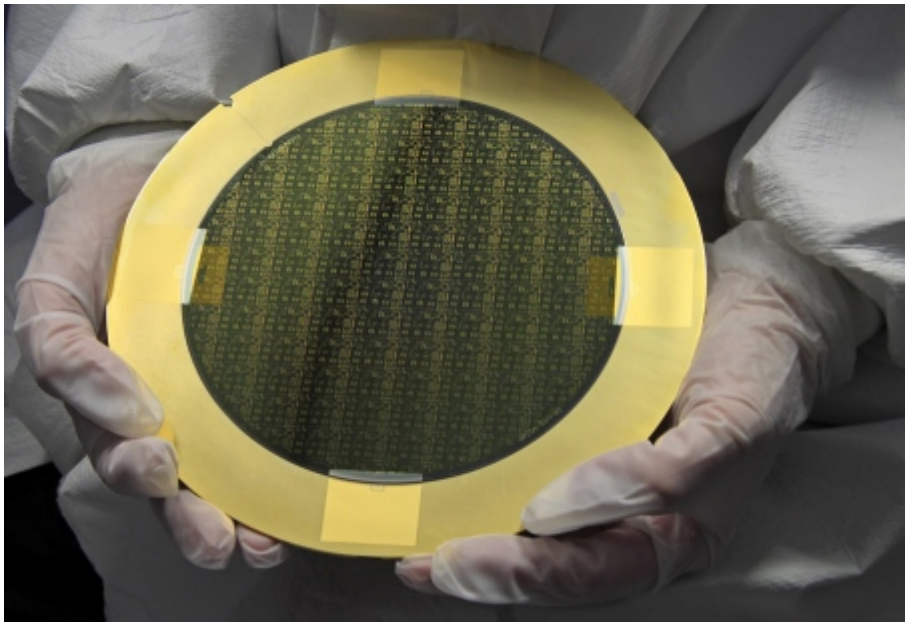

Figure 3-1: MMIC wafers. (www.microwave-eetimes.com).

In this chapter, we'll briefly present the most relevant elements of the SG25H3 IHP (Innovations for High Performance Microelectronics) SiGe BiCMOS technology which is currently used in many research and industrial projects to develop RF circuits for wireless telecommunications and broadband communications, aerospace, automotive, security and automation applications [26]. In this project, IHP SiGe BiCMOS technology has been used for realization of the multi-core RFIC chip and related sub-circuits.

3.2 SG25H3 process

SG25 is the basic 0.25 µm CMOS process. It provides NMOS, PMOS, isolated NMOS and passive components such as poly resistors and MIM capacitors. In addition to the

basic CMOS process 3 frontend options and 2 aluminum backend options are offered. The IHP SG25H3 0.25 µm microwave bipolar complementary metal oxide semiconductor (BiCMOS) process offers high-performance technology with SiGe hetero junction bipolar transistors (HBT) up to fT/fmax = 110 GHz /180 GHz and HBTs with higher breakdown voltages up to 7 V. The technology is suited for applications between 24 GHz and 60 GHz, making it especially useful for the designers of wireless, broadband and radar products. SG25H3 is one of a 0.25 µm and 0.13 µm BiCMOS technology set with HBTs up to 300 GHz fmax that IHP offers customers for Multi Project Wafer and Prototyping Services. The standard backend option offers 3 thin metal layers and two Top Metal layers (Top-Metal1 - fourth 2 µm thick metal layer, TopMetal2 – fifth 3 µm thick metal layer) and a MiM layer. Together with a high dielectric stack this enables increased RF passive component performance. In next sections we will provide more detailed information about this technology. Stack up of SG25H3 technology with 5 metallization layers illustrates in figure 3-2.

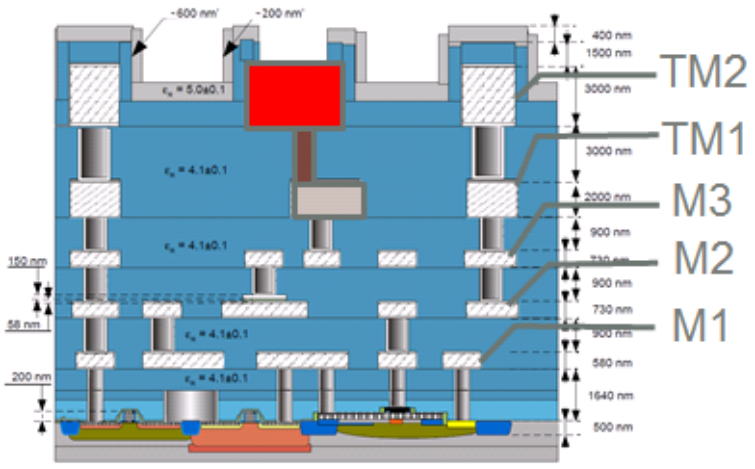

Figure 3-2: Stack up of SG25H3 technology with 5 metal layers (www.ihp-microelectronics.com).

3.2.1 Active components

Active components provided in SG25H3 technology are divided in two main categories: bipolar (BJT) devices and CMOS (FET) devices. There are several types of BJT included in the SG25H3 Design Kit (DK). The basic selection parameters are related to the number of collector and to the maximum current handling. For instance, the BJT component ihp_npnH3shp1 can handle a collector current of 2mA while the ihp_npnH3shp2 can handle 4mA. The maximum current handling capabilities are obtained with the ihp_npnH3shp16 (figure3-3) that can operate until a maximum of 32mA. This type of components is widely used in the design of Low Noise Amplifiers and in power amplifiers. CMOS devises also divided to 2 main groups: NMOS and PMOS. Each component has three main design parameters which are the width, the length and the number of gates. For an example ihp_rfnmos_h3 is the NMOS device that is frequently used in RFIC components design such as switches or vector modulators with different number of the gates.

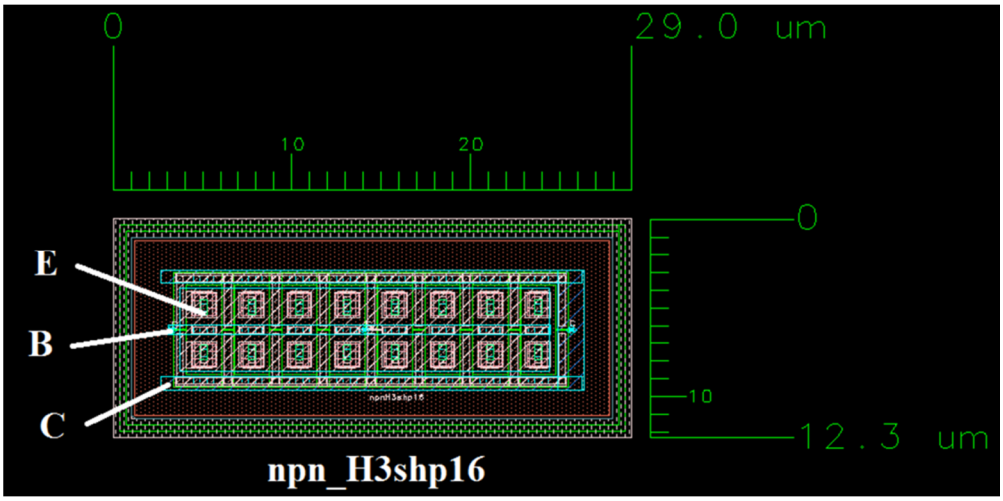

Figure 3-3: Layout of ihp_npnH3shp16 bipolar transistor with 16 emitters as it is provided in the IHP SG25H3 design kit.

3.2.2 Passive components

A lumped passive component in a microwave circuit is defined as microwave element whose size across any dimension is much smaller than the operating wavelength. In other words, in lumped elements there is no appreciable phase shift between the input and the output phase. Usually for good approximation the maximum dimension must be less than $\lambda/20$ [27].

In the following sections it is reported a brief description of inductors (L), capacitors (C) and resistors along with their basic characteristics.

3.2.2.1 *Inductors*

An ideal inductor stores or releases magnetic energy and does not store electric energy which is typically associated with capacitive effects. Ideally, an inductance does not dissipate any power because it does not have any resistive loss. Magnetic energy is stored as long as current flow remains through the inductor. However realizing inductor with low capacitance or resistance effect on SiGe chip is still challenging. Generally inductors can be realized in several ways such as wire bond, single loop or spiral. The printed spiral inductor can be used for on-chip applications because they are smaller than the other types and also their fabrication is easier. On the other hand, the inductance value of spiral inductors can be controlled by different geometrical parameters of the spiral. There are typically four geometries that can be used to create spiral inductors (figure3-4):

- Rectangular
- Hexagonal

- Octagonal
- Circular

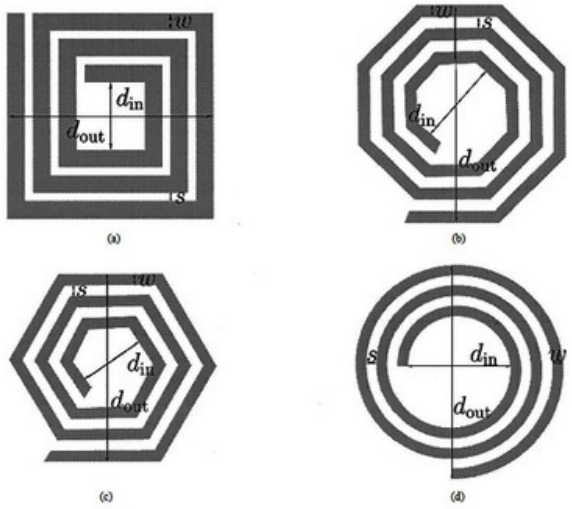

Figure 3-4: Planar spiral inductor layouts (a) Square (b) Octagonal (c) Hexagonal (d) Circular (www.vlsi.itu.edu.tr)..

To satisfy the layout design rules that provided by IHP for SG25H3 technology, circular and hexagonal spirals cannot be used. Top metal 1 and Top metal 2 are used for realizing the inductor to increase the amount of the inductance while size reducing. In Metal 1 it is usually printed the inductor ground plane which can be a solid rectangle with slits, a rectangular ring or a periodic structure. Air bridges are realized by arrays of vias from Top Metal 2 to Top Metal 1. The use of arrays reduces the total resistance of the inductor and improves its reliability. The equivalent model of printed spiral inductors is shown in figure 3-5 and it consists of a capacitance between inductor and ground and capacitance between inductor input and output terminals. There is also series resistance, R_S, that models the losses in conductor and dielectric.

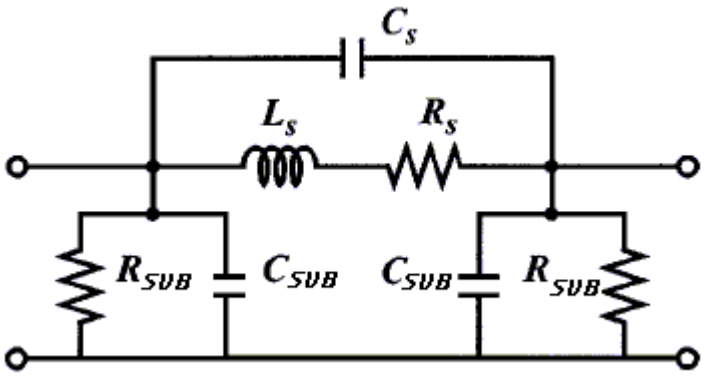

Figure 3-5: Spiral inductor model.

Important parameters that can effect of value of inductance are listed below.

- Number of turns (N)
- Spacing between turns (s)
- Turn width (W)
- Outer Diameter (dout)
- Inner diameter (din)

To obtain a certain amount of inductance at the desired frequency band, physical dimensions must be optimized. A first guess of the geometrical parameters can be obtained using an analytical expression [28]. However, in case of SG25H3 technology it is not possible to apply any closed formula because the thickness of the metals is considerable with respect to the substrate.

Usually, full wave EM simulations are used to fine tune the inductance value of spiral inductors [29]. An example of spiral inductor with inductance of 0.4 nH is shown in figure 3-6 and Physical characteristics are shown in table 3-1. Top metal 2 is used for main path and top metal 1 is used for under path to have maximum distance between inductor and reference plane in metal 1. The array of 9 vias from top metal 2 to top metal

1 used to decrease the overall resistance and, in turn, to increase the quality factor of the inductor.

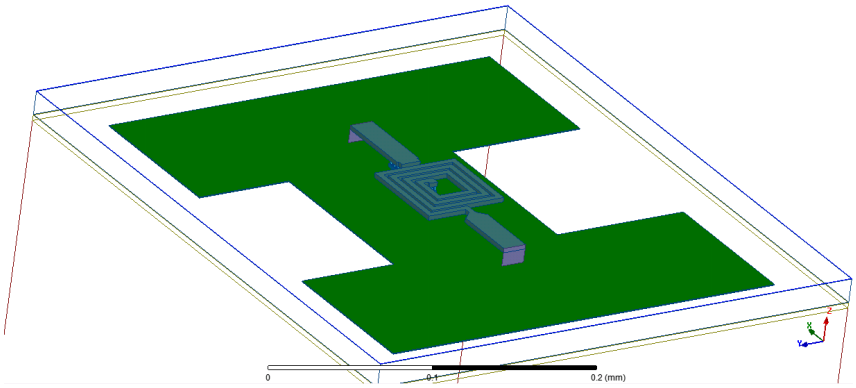

Figure 3-6: L=0.4 nH spiral inductor HFSS model.

Table 3-1: Physical characteristics of 0.4nH designed spiral inductor.

Number of turns	4
Width of inductor line	4 um
Spacing between lines	2 um
Width of spiral	68 um
Length of spiral	83 um

The unwanted capacitance and parasitic effects usually occurs due to the small gap between turns. To reduce these effects the distance between turns can be increased. However this might significantly increase the overall size of inductor

Typically, several parameters are considered to design inductors as listed in table3-2.

Table 3-2: Importanat parameters in piral inductor design.

Effective inductance	nominal inductance
Impedance	impedance of the inductance
Quality factor	ratio of energy stored to power dissipated in the inductor
Self-resonance frequency	frequency that imaginary part of input impedance of inductance became zero
Maximum current rating	maximum current that inductor can handle due to design role provided by ihp SG25H3 technology

An example of fabricated 0.4nH spiral inductor is shown in figure 3-7.

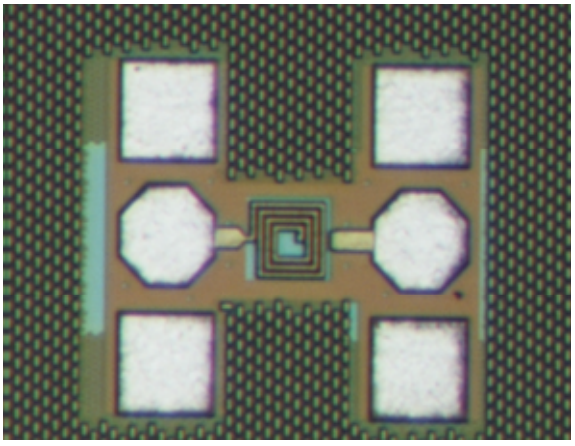

Figure 3-7: Micro photo of 0.4nH rectangular spiral inductor shown in figure3-6.

The effective inductance values obtained from simulations and measurements are shown in figure 3-8. As it can be observed, there is a very good agreement between the

numerical and the experimental results. Furthermore, it can be noticed that the amount of the inductance remains stable over frequency.

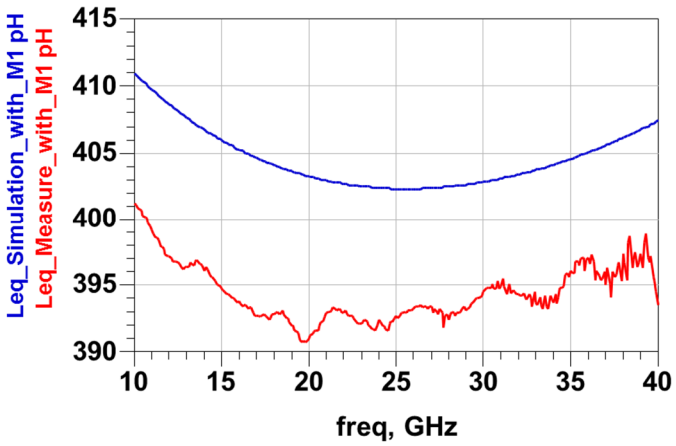

Figure 3-8: Simulation and measurement results of the inductance of the 0.4nH spiral inductor shown in figure3-7.

The measured and simulated quality factor of 0.4nH spiral inductor is shown in figure 3-9. As it can be seen, there is a small difference between the simulation and the measurement results which is mainly due to simulation inaccuracies The measured and simulated results of the same spiral inductor without ground plane located in metal1 are shown in figure 3-10 and figure 3-11. The quality factor and also the value of inductance of spiral inductor without ground plane in metal 1 is higher as compare as the case that metal 1 considered as a ground.

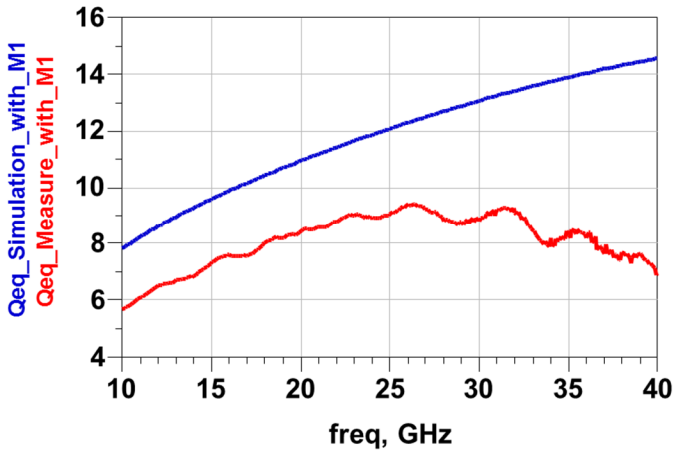

Figure 3-9: Quality factor of simulation and measured 0.4nH spiral inductor.

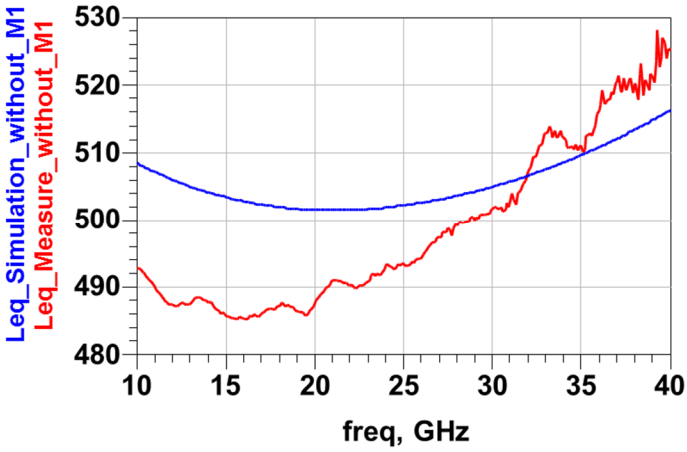

Figure 3-10: Simulation and measurement results of the inductance of the spiral inductor shown in figure3-7 without metal 1 below.

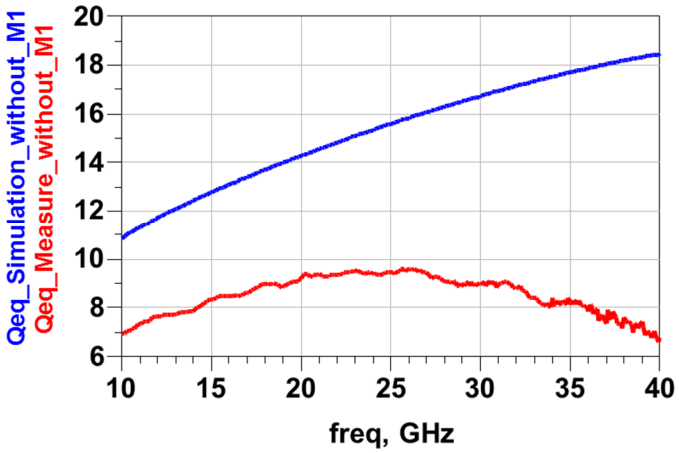

Figure 3-11: Quality factor of simulation and measured spiral inductor without metal 1 below.

3.2.3 MiM Capacitors

Capacitance is defined as the capacity to store energy in an electrical field between two conductors. The value of capacitance strongly depends on the area of the electrodes and on the dielectric material between the two electrodes. The capacitor might have two or more conductors (series or parallel capacitance). There are different methods to realize the capacitance that can be used in MMIC applications including MiM (metal-insulator-metal) capacitors, microstrip capacitors, inter-digital capacitors [30]. Generally, the most useful method in SiGe chips is to use MiM capacitors [31]. MiM capacitors are realized in SG25H3 technology by two very metal layers with an interlayer distance of 58nm. The lower layer is metal 2 and the upper layer is a very thin metal layer of thickness 150 nm that is connected to metal 3 with arrays of vias. In other words, the MiM capacitor is accessible from metal 2 and metal 3 as shown in figure 3-12. The MiM

capacitor dielectric constant is 7.3 thus helping to reach higher values of capacitance in small areas

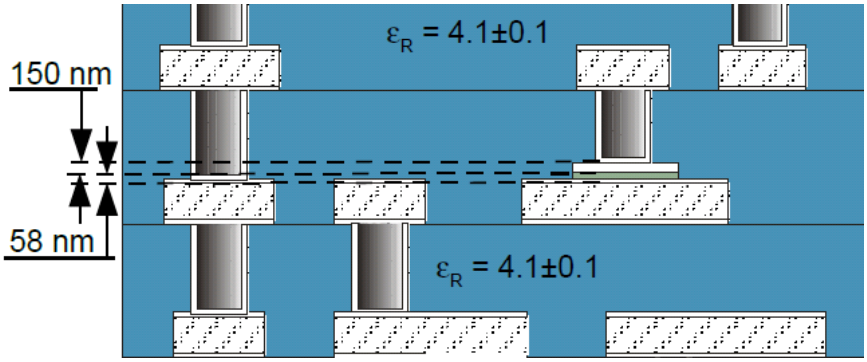

Figure 3-12: MiM capacitor realization in SG25H3 technology.

MiM capacitors main geometrical parameters are listed in table 3-3.

Table 3-3: MiM capacitor design parameters.

Parameter	Definition
Capacitor value	typical value for capacitance
Effective capacitance	nominal capacitance value
Tolerances	the accuracy provided by technology
Quality factor	ratio that shows the capability of energy storing in MiM capacitor
Rated voltage	maximum voltage that can be applied to capacitor terminals without destroying dielectric or conductors
Rated current	maximum current that MiM capacitor conductor plates can handle

The most important parameter to obtain a determined value of capacitance is the conductor plate size that can provide minimum 29 fF up to maximum 4.7pF. The equivalent model of MiM capacitors, shown in figure 3-13, includes series and parallel resistance and small series inductance that came from conductor loss and dielectric losses.

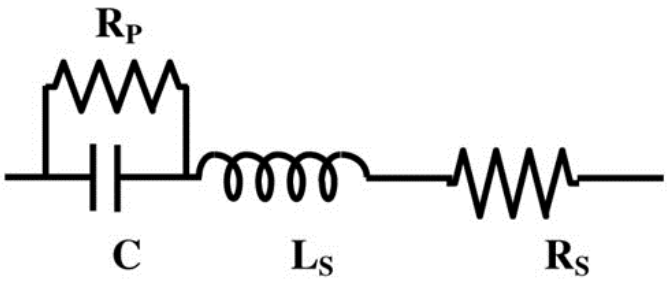

Figure 3-13: Equivalent circuit model of capacitor.

HFSS model of 1pF MiM capacitor is shown in figure 3-14. Metal 1 is considered as a reference plane for MiM capacitor and electrodes are accessible from metal 2 and metal 3.

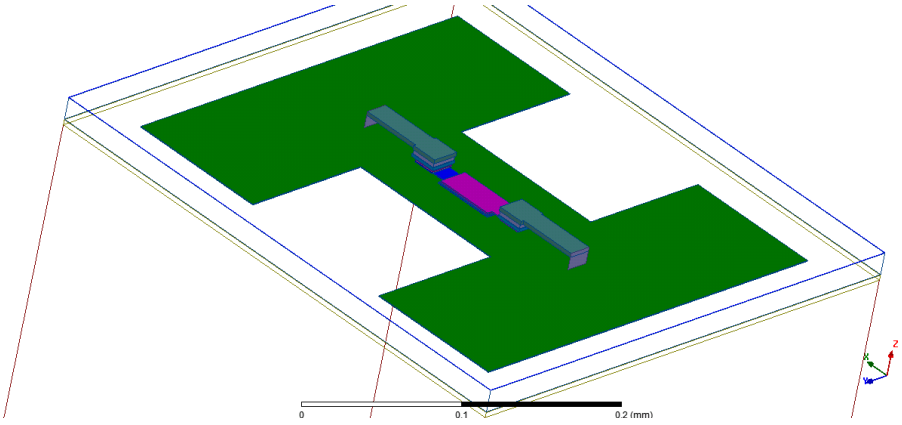

Figure 3-14: HFSS model of 1pF MiM capacitor.

The approximate value of capacitance obtain from Eq.3-1

$$Ceq = \frac{\varepsilon A}{d} \qquad \textbf{Eq. 3-1}$$

Where ε is the Permittivity of material between plates, A is the area of metal plate and *d* is the separation of the electrodes that in SG25H3 technology ε_r is 7.3 and *d* is equal to 58 nm. Micro photo of fabricated prototype is shown in figure 3-15.

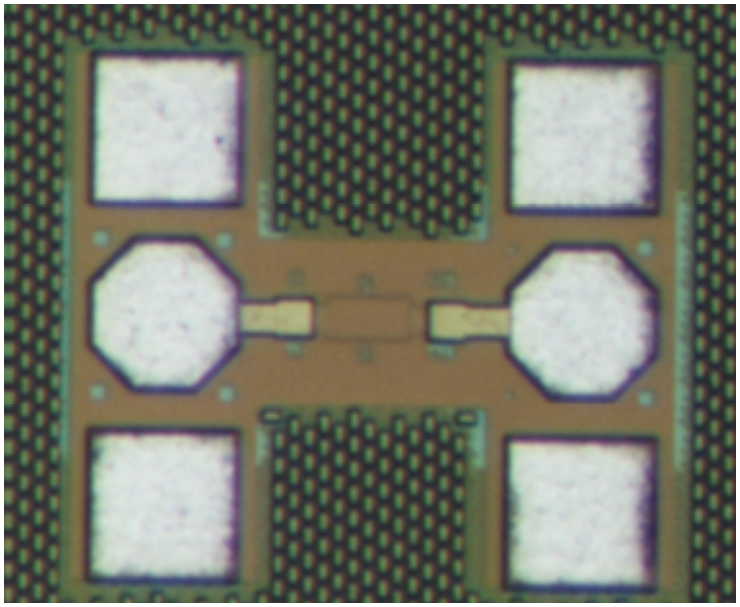

Figure 3-15: Micro photo of fabricated prototype of 1pF MiM capacitor.

Simulation and measurement results of a 1pF MiM capacitor are shown in figure 3-16 and figure 3-17.

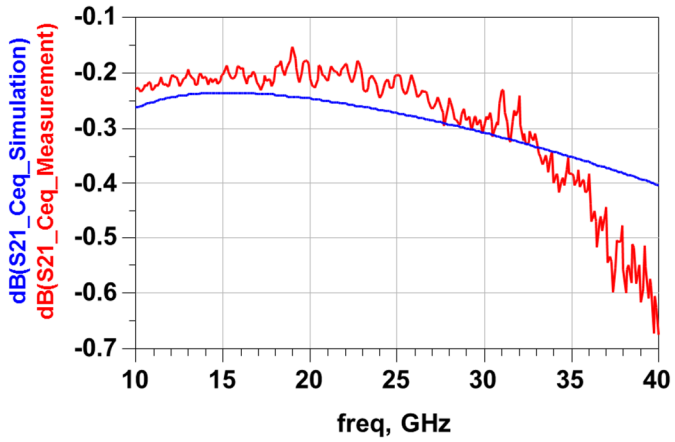

Figure 3-16: S_{21} of simulation and measurement of 1pF MiM capacitor.

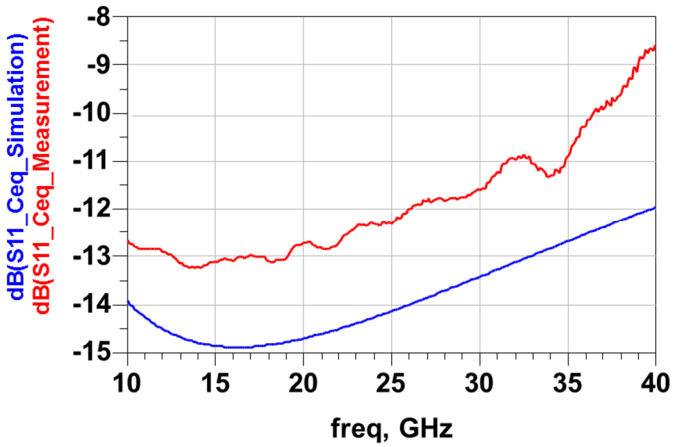

Figure 3-17: S_{11} of simulation and measurement of 1pF MiM capacitor.

3.2.4 Resistors

Lumped element resistors are widely used in MMIC and RF IC applications. Resistors can be employed for several types of applications such as terminations, isolation resistors, feedback network resistor, impedance matching network or biasing networks [32].

The main parameters to be considered in the design of MMIC resistors are listed in table3-4:

Table 3-4: MMIC resistor design parameters.

Parameter	Definition
Resistance value	typical value for capacitance
Maximum current handling capacity	maximum current that MMIC resistor can handle
Size of resistance	the physical dimensions of resistor
Nominal tolerance	the accuracy provided by technology
Temperature coefficient of resistance	the ratio that shows the resistor value change by temperature changes

In SG25H3 technology resistances are realized by lossy material on a dielectric base that provides variable resistance depending on the size and the type of materials. Resistors in this technology are divided into four categories which cover different ranges of resistors and different maximum currents. The four types of resistors are listed in table 3-4.

Table 3-5: Resistor types and application

Resistor type	Application
Ihp_rsill_h3	used for small resistance value smaller than 500 ohm. Sheet resistance is 7 ohm
Ihp_rpnd_h3	used for small and medium resistance value smaller than 4 K ohm. Sheet resistance is 210 ohm
Ihp_rppd_h3	used for medium and big resistance value bigger than 2 K ohm. Sheet resistance is 280 ohm
Ihp_rhigh_h3	used for big resistance value bigger than 5 K ohm. Sheet resistance is 1.6 K ohm.

The layouts of the different types of resistance are shown in figure 3-18.

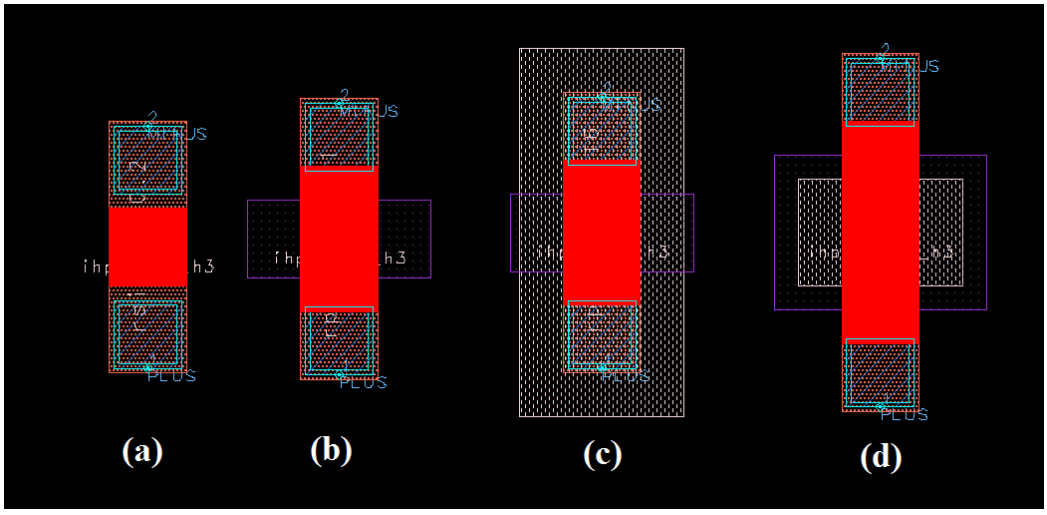

Figure 3-18: Layout of (a) ihp_rsill (b) ihp_rpnd (c) ihp_rppd (d) ihp_rhgh.

CHAPTER 4

SATCOM USER TERMINAL WITH ELECTRONIC BEAM SCANNING

4.1 Antenna array configuration

According to the SatCom specifications as given in chapter 2 we decided to use direct radiating array with electronic beam scanning. The direct radiating array is designed to have dual-band operation, i.e., 19.7 GHz – 21.0 GHz for receive and 29.5 GHZ – 30.8 GHz for transmit. It is expected that this array exhibits beam scan capability up to 60° in both elevation and azimuth planes. In order to avoid grating lobes, the distance between adjacent elements must be maintained at about 0.5λ. Such characteristics can be obtained considering an array of dual band and single band elements interleaved in the array. Difficulties result from the RX-TX frequencies of operation which, for the application being considered, are in a ratio of 2/3. Two main issues must be tacked to account: 1) the identification of an array topology able to accommodate the elements in a way that they are spaced at about half a wavelength at both frequencies; 2) the design of a dual band element compact enough to be placed in the array. Furthermore, elements have to be designed reducing coupling between radiators and between feeding lines to a minimum, in particular coupling between RX elements, coupling between TX elements and coupling between TX and RX elements must be minimized.

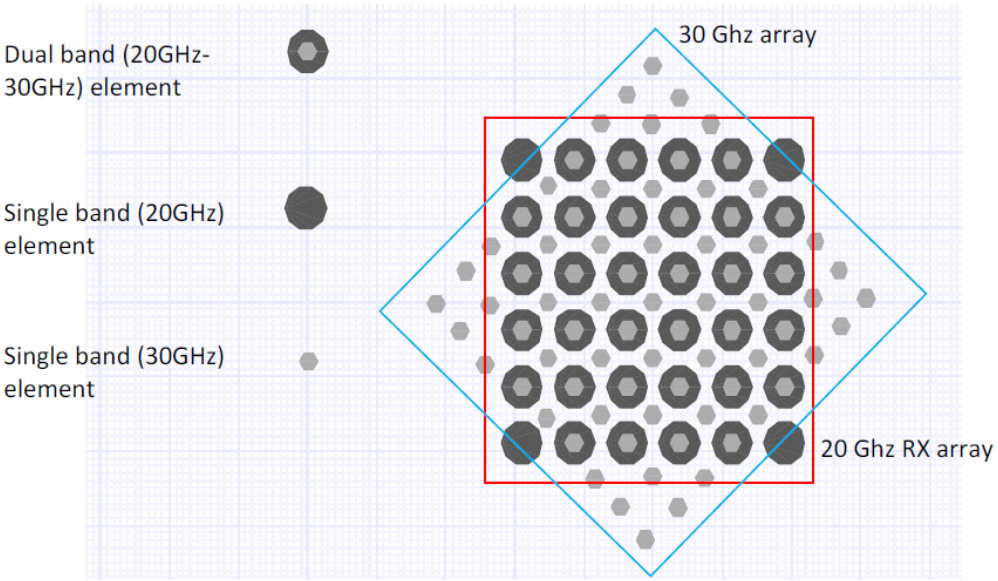

Figure 4-1: Antenna array layout.

Due to the constraints given by the ratio between the TX and RX wavelengths, dual band elements cannot be placed at distances which are close to half a wavelength at both frequencies of operation. The large separation between the operating wavelengths can be balanced interleaving dual band elements with single band elements operating at the higher frequency. The principal planes of the RX and TX arrays are rotated by 45°. With this configuration, if the RX elements are spaced 0.5 wavelength at 20 GHz, the TX elements result to stay at 0.53 wavelength at 30 GHz. As it can be seen, other than dual band radiators, single band elements operating at 20 GHz and at 30 GHz have been employed.

As it shown in figure 4-1 three type of radiating element are used in the antenna array, dual band radiator, RX single band radiator and TX single band radiator. Antenna elements have a multilayered structure and are fed by stripline. The radiating element is composed by an annular slot surrounded by vias for propose of increasing the isolation between adjacent elements. The inner border of the elements slot is also surrounded with

vias forming a coaxial structure. In figure 4-2 and figure 4-3 are shown the 20GHz and 30GHz element geometry.

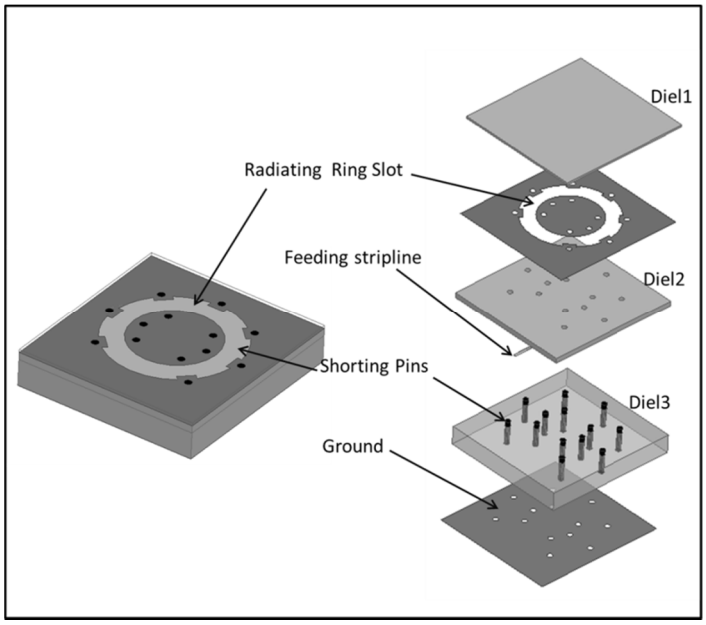

Figure 4-2: 20GHz radiating element geometry.

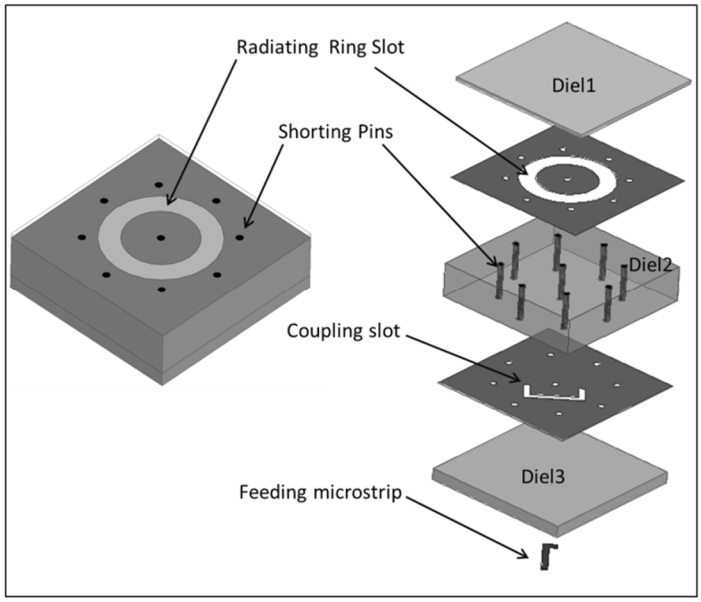

Figure 4-3: 30GHz radiating element geometry.

The two elements can be combined to form a dual band radiator as shown in figure 4-4.

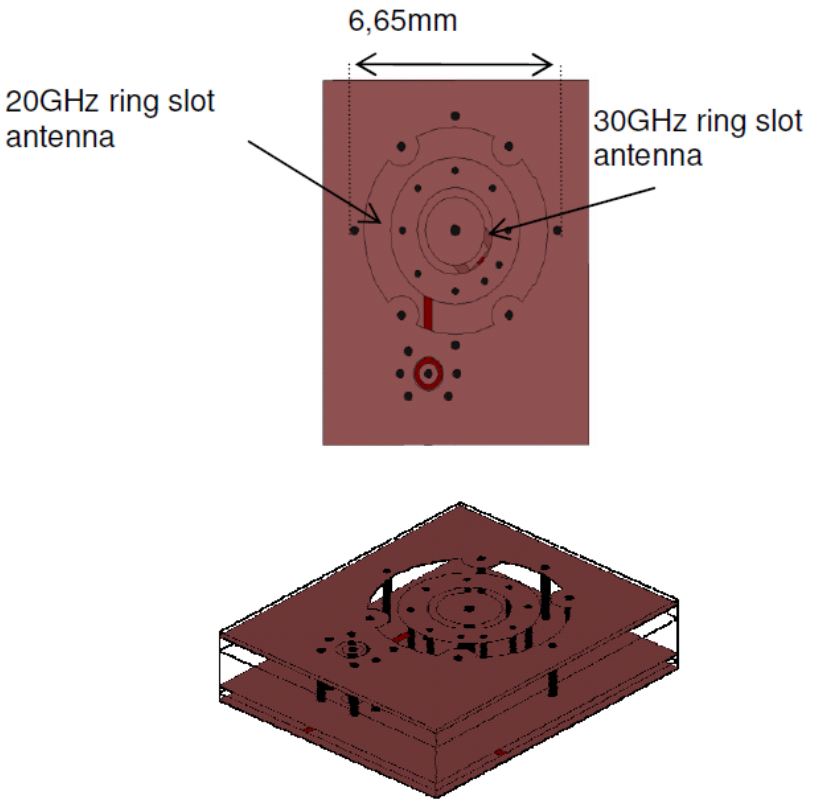

Figure 4-4: Dual band radiator layout (FLEXWIN Deliverable D2.1).

Each radiating element is fed with different techniques. The RX ring is electromagnetically coupled to a stripline while the TX ring is fed by means of a slot. Feeding structure is shown in figure 4-5.

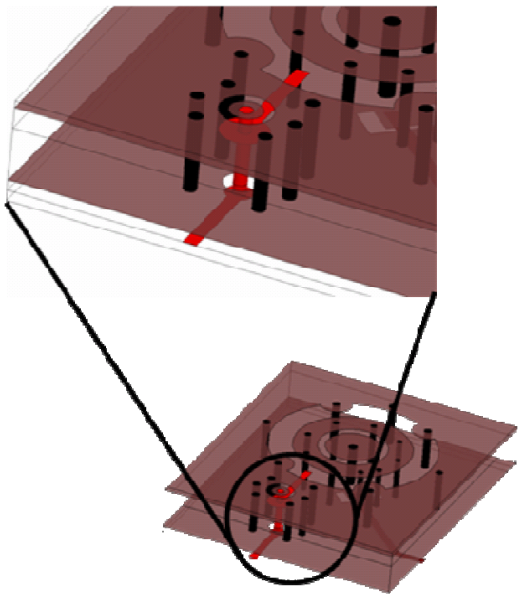

Figure 4-5: Feeding of dual band radiating element (FLEXWIN Deliverable D2.1).

Figure 4-6 shows S_{11} obtained from simulation for the dual band radiating element. Isolation between TX and RX port is shown in figure 4-7 for both frequencies band.

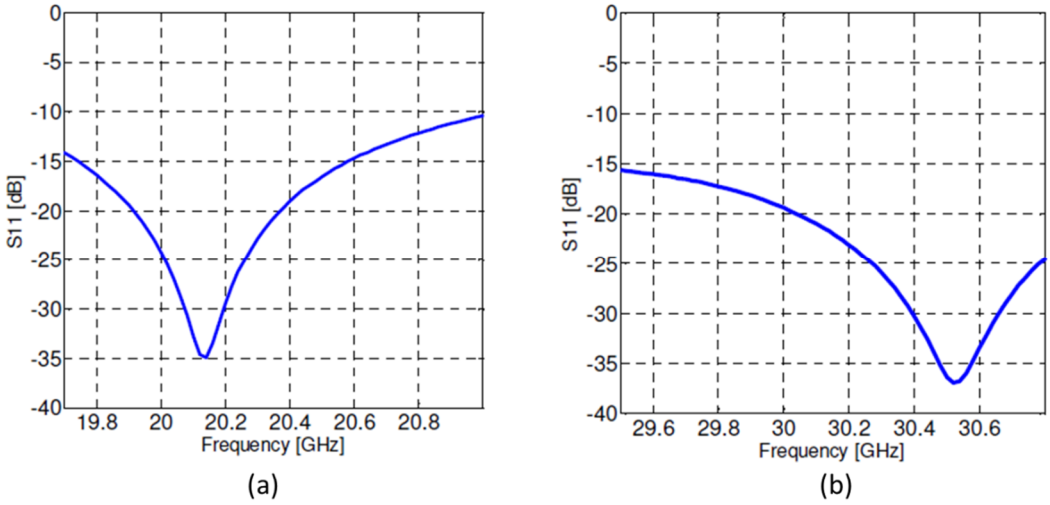

Figure 4-6: Simulated S_{11} at (a) RX port (b) TX port.

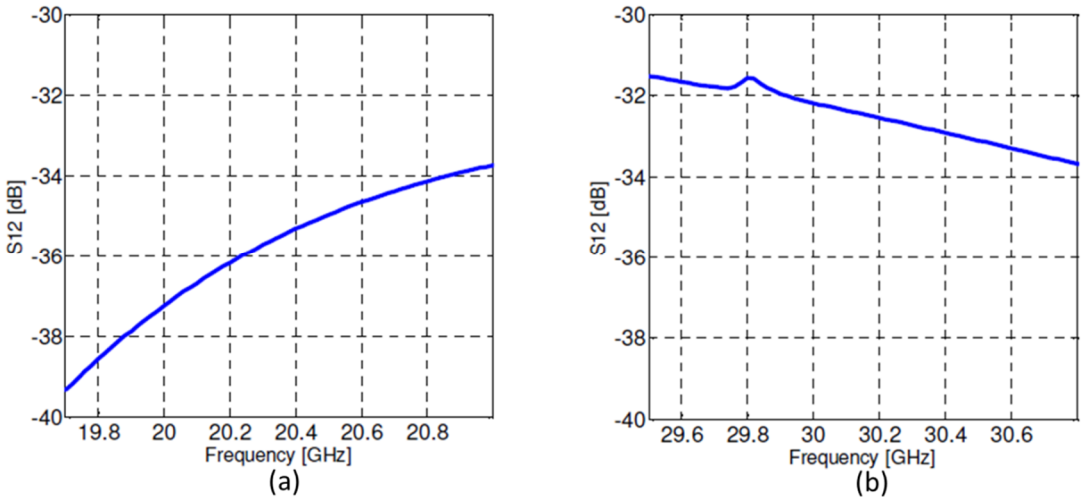

Figure 4-7: Simulated isolation in (a) RX band (b) TX band.

Simulated gain is 3.8 dB at 20 GHz and 4.5 dB at 30 GHz. In order to investigate the element gain on the operational bands, simulations have been carried out for a 2×2 array. Figure 4-8 shows the element gain vs. frequency for the 2×2 configuration. Results are satisfactory over the entire bandwidth.

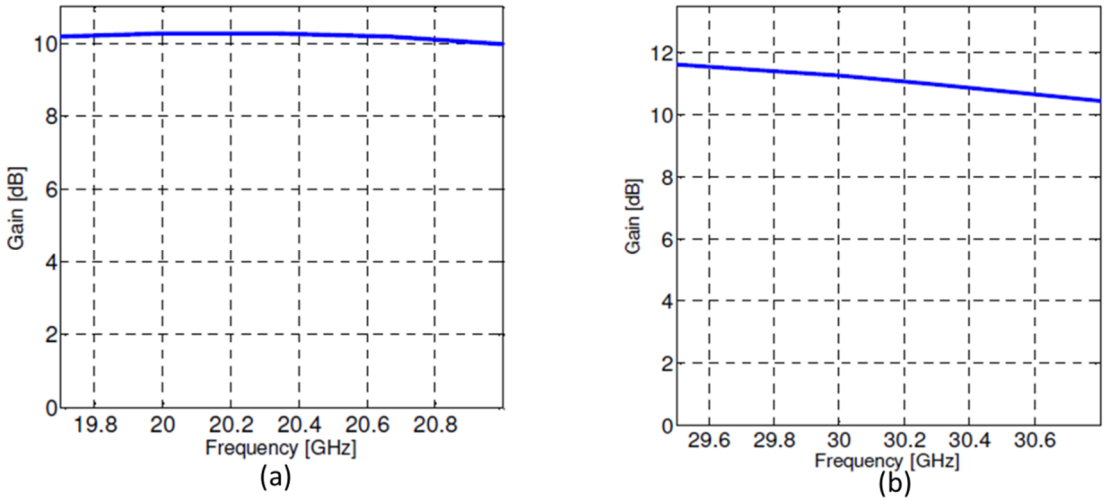

Figure 4-8: Simulated gain for 2×2 sub-array for (a) TX band (b) RX band.

Figure4-9 illustrates the architecture of antenna array and shows the radiating elements connected to the same chip are highlighted.

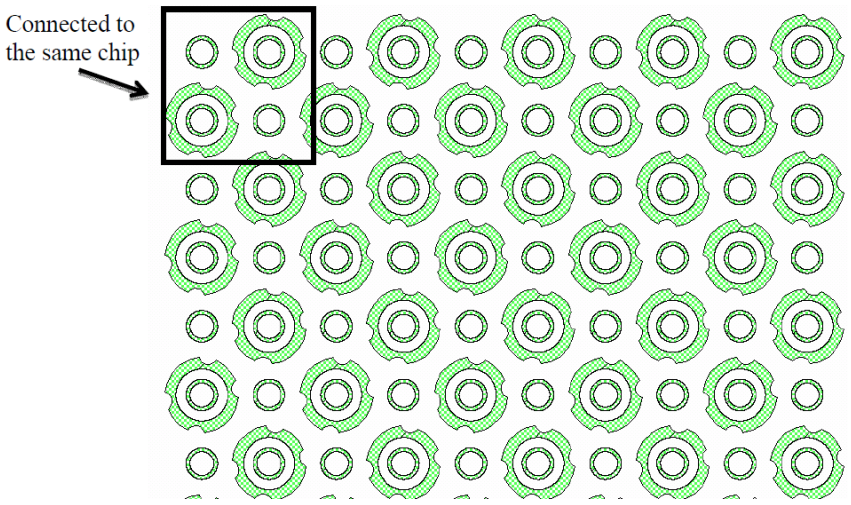

Figure 4-9: Layout of antenna array.

The specifications for the antenna array derive from the final full-scale antenna specification and are listed in Table 4-1.

Table 4-1: Specifications for antenna array.

Frequencies:	Receive: 19.7 – 21.0 GHz Transmit: 29.5 – 30.8 GHz
Polarization:	Single linear
Beam steering:	Electrical in azimuth and elevation
Coverage:	±60°
Height:	less than 5 cm
Total output power per element:	1.4 mW

Number of elements:	approx. 100
Receiver noise figure per element:	5 dB
Transmit/receive functionality switch:	BiCMOS based

Chips are placed in the lower part of the array. Coaxial transition have been used to connect the chips to the feeding striplines as shown in figure 4-10 and figure 4-11.

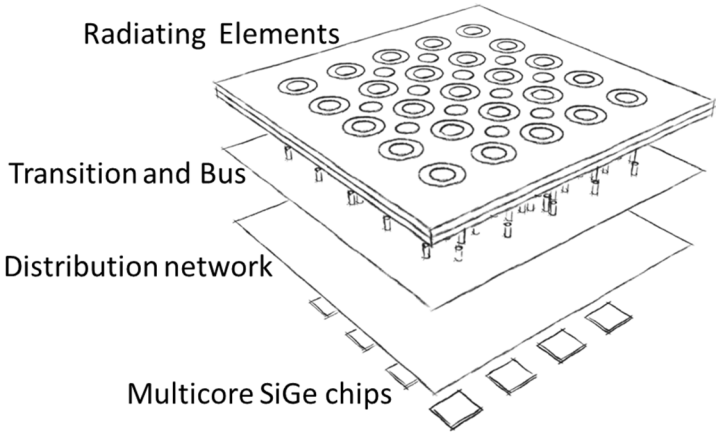

Figure 4-10: Antenna array feeding network with multicore SiGe chip.

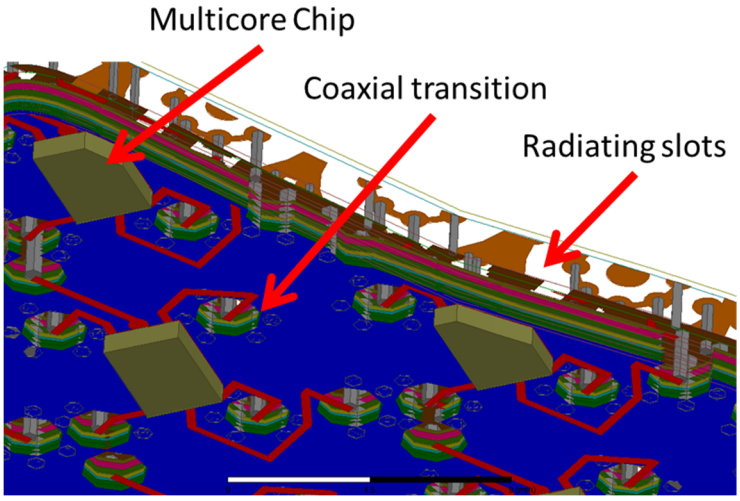

Figure 4-11: Chip position and feeding lines to radiating elements.

Each multicore SiGe chip feed six antennas as shown in figure 4-7. Two RX (20 GHz) antennas and four TX (30 GHz) antennas connected to one chip. This mean for approximately 100 elements we need at least 17 chips to feed them.

4.2 Chip configuration and architecture

As discussed in pervious section each chip must provide 7 RF terminals. Two terminals for RX antennas that must operate at 20 GHz, four terminals for TX antennas that operate at 30 GHz and one terminal that musty operate at both frequencies that connect to distribution network. There are also I2C buses and data lines for controlling the voltages and functionality of the chip. To satisfy the specification required for antenna array, multicore SiGe chip is designed by employing of several RF blocks such as low noise amplifiers, power amplifiers, vector modulators, switches and power divider-combiner. Reconfigurability or in another word electronic beam steering is the characteristic gained by selectable and controllable components of the chip such as switches and vector modulators.

The architecture of the chip is based on different functionality that expected from chip. The main issues in TX mode are to minimize noise figure and have good matching in all terminals. On the other hand providing enough output power in RX mode is the main goal. For these reasons in RX mode LNA is used to decrease the noise figure and in TX mode PA is used to reach the maximum gain in output. Switching network (SW) is used to separate TX and RX mode and provide enough isolation between them. Vector modulators (VM) in both modes are employed to obtain variable output that cause reconfigurability. Wide band power divider-combiner (PW) provide the possibility to

divide and combine the power that comes or goes to distribution networks in to the different branches. Figure 4-12 shows the block diagram of chip and control units as well.

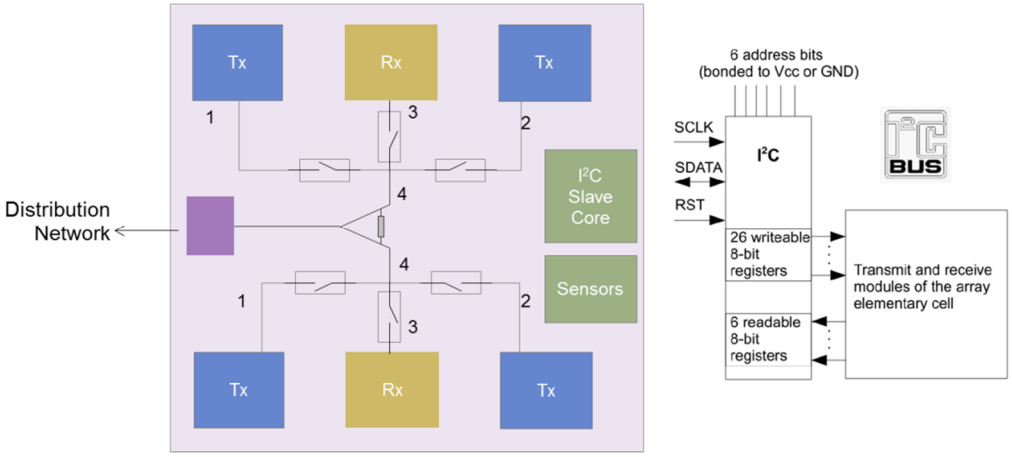

Figure 4-12: Block diagram of the chip and I2C control unit.

Figure 4-13 shows a detailed blocks and the connection between them, as shown in the main line come from the distribution network and then goes to wideband Wilkinson power divider, then each branch is connected to the switching network. Switching network has 1 input and 3 out puts, one of them is connected to RX radiating element, while remaining two are connected to TX radiators.

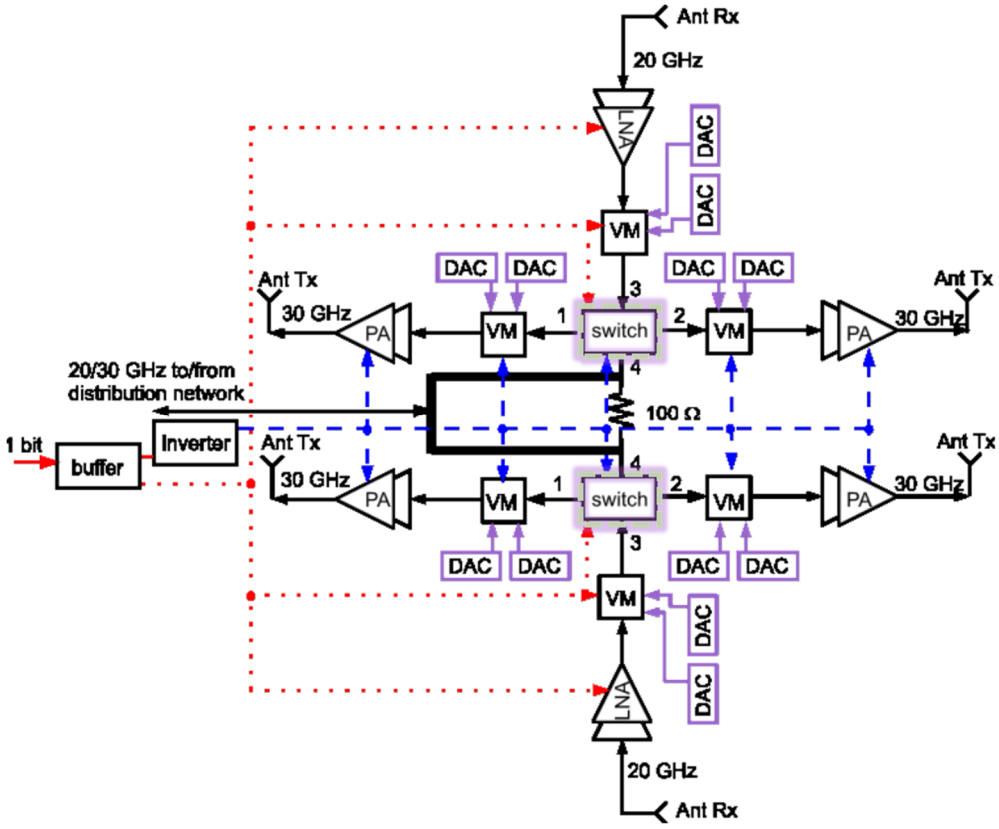

Figure 4-13: Block diagram of multicore SiGe chip with RF blocks.

Selecting transmit or receive mode is done by switching network while DACs control the voltage of vector modulators.

4.3 Link budget and chip components specs

In this section is discussed the link budget and the related antenna performance analysis for Ka-Band SatCom applications based on the knowledge of existing satellite communication systems. Transmit and receive concern divided in two different parts that must be considered.

In the case of transmit antenna following parameters were considered:

- G/T (Antenna gain to noise temperature) of the receive antenna on the satellite

- required S/N(Signal to noise ratio)on the satellite
- available output power of the intelligent pixel chip

By assuming a G/T of 16dB/K with a required S/N of 10dB on the satellite, the necessary EIRP (effective isotropic radiated power) of the transmit antenna on the mobile platform can be calculated. The resulting EIRP for the targeted mobile antenna system is 53dBW. To have enough amounts of output power and also considering the number of transmitting elements, each radiating element must have at least 40mW of output power. Due to this power SiGe multi core chip must generate 50 mW at RF output. For this reason PA and gain blocks (GB) is used to reach this level of RF output power.

In the case of receiving antenna the following parameters are considered:

- EIRP of the transmit antenna on the satellite
- required S/N on the mobile terminal
- available noise-figure of one intelligent pixel in the FLEXWIN receiver chain

By assuming an EIRP of 56dBW for the satellite transmitter antenna with a required S/N of 10dB at the mobile system, the necessary G/T of the receive antenna can be calculated. The resulting G/T of the mobile receive antenna is 10dB/K. By assuming 39 dB of the gain for antenna array, the SiGe chip must have noise figure around 5 to satisfy the specifications.

To satisfy the specification for SatCom application for array antenna, each RF block must meet specifications listed below:

LNA (20 GHz):

- Gain: 20 dB
- NF: <4 dB
- IP1dB: -20 dBm

Vector modulator RX (20 GHz):

- Gain: -5 dB
- IP1dB: -2 dBm

Vector modulator TX (30GHz):

- Gain: -5 dB
- IP1dB: 15 dBm
- Pin: 9 dBm
- Pout: 4 dBm

Wide band power divider-combiner:

- Isolation in off state: 25 dB at 30 GHz
- Insertion loss: <1,5 dB at 20 GHz

CMOS switching network

- Isolation in off state: 12 dB @ 20 GHz
- Insertion loss: <1,5 dB @ 30 GHz

Power amplifier

- Gain: 13 dB
- Gain in bias of state: -5dB
- IP1dB: 10 dBm
- OP1dB: 23 dBm 1dB-compression point, i.e. 17 dBm at 6 dB back-off

- Pin: 4 dBm
- Pout: 17 dBm

DAC:

- 8 bit resolution with I2C bus steering interface.

CHAPTER 5

LOW NOISE AMPLIFIER

5.1 Low-noise amplifier design strategy

One of the main components of any wireless transceiver system is the LNA. For Ka-band SatCom systems the LNA design presents significant challenges both in terms of matching bandwidth, noise figure and power dissipation [33]. In particular, for the application at hand, the most significant issue is to combine gain and noise performance, typically critical in SiGe BiCMOS technology. Many approaches can be employed for the design of MMIC LNAs. For example, wideband operation can be achieved using distributed topologies [34]. However, distributed amplifiers typically consume high die area and they suffer from high noise figure (NF). Other design techniques, such as common gate [35] and ladder-matched LNA configurations [36], can be taken into account but they also suffer from high NF. Additional methods include staggered compensation [37] and transformer feedback techniques [38] which can be used to extend the bandwidth. The limited noise performance are a common issue for all these configuration and they can be only mitigated using shunt-resistive feedbacks as shown in [39].

5.1.1 LNA requirements and preliminary performance analysis

As discussed in chapter 4, the LNA to be used in the hexa-core chip should meet the following specifications:

- Gain: >20 dB
- NF: <4 dB
- IP1dB: -20 dBm
- Frequency band 19.7 GHz to 21GHz
- Low power consumption
- Small size

To meet these requirements, a comparative analysis has been performed to define the best configuration. In general, the number of lossy components has been kept to a minimum in the RF pass to reduce the noise figure and two cascaded stages have been employed to increase the gain.

To select the type and size of the bipolar SG25H3 transistor, several parameters have been evaluated such as linearity, power consumption, maximum saturation current level, minimum noise figure and the gain of the transistor. Similarly, the transistor current bias should be selected carefully to avoid any power loss in the RF and bias path. Two types of the transistors were selected for the LNA design, namely the IHP_npnH3shp16 bipolar transistor for RF amplification and the IHP_npnH3shp1 transistor for the DC current bias network. The DC behavior of the IHP_npnH3shp16 transistor for different base currents (IBB) is shown in figure 5-1.As it can be observed from DC and noise figure simulations results of single transistor in figure 5-1 and figure 5-2, a collector to emitter voltage, $V_{CE,}$ equal to 1.5V is the optimum value for the DC bias point of IHP_npnH3shp16 transistor while the base current can be changed from 10uA to 100uA.

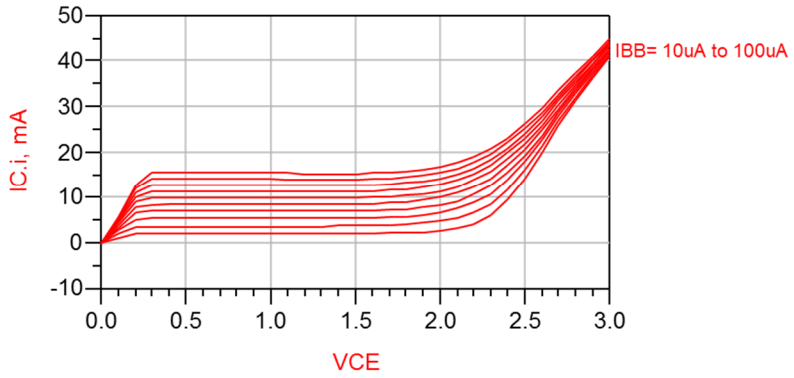

Figure 5-1: DC behavior of the IHP_npnH3shp16 for different base currents.

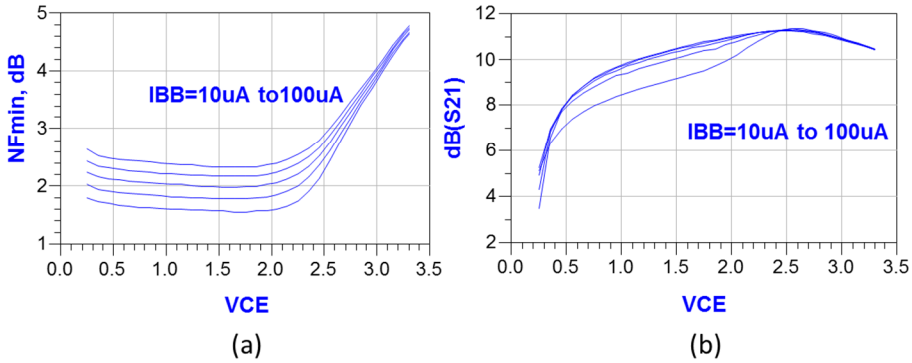

Figure 5-2: (a) minimum noise figure (b) gain of IHP_npnH3shp16 for different base currents.

Figure 5-2 shows the noise figure and the gain of the single transistor with different base current bias conditions. A series LC matching network is employed at the input of the LNA and a series capacitor, C, and grounded inductor, L, matching network are employed in the output stage of the LNA to provide impedance matching both in input and output.

5.1.2 Schematic description

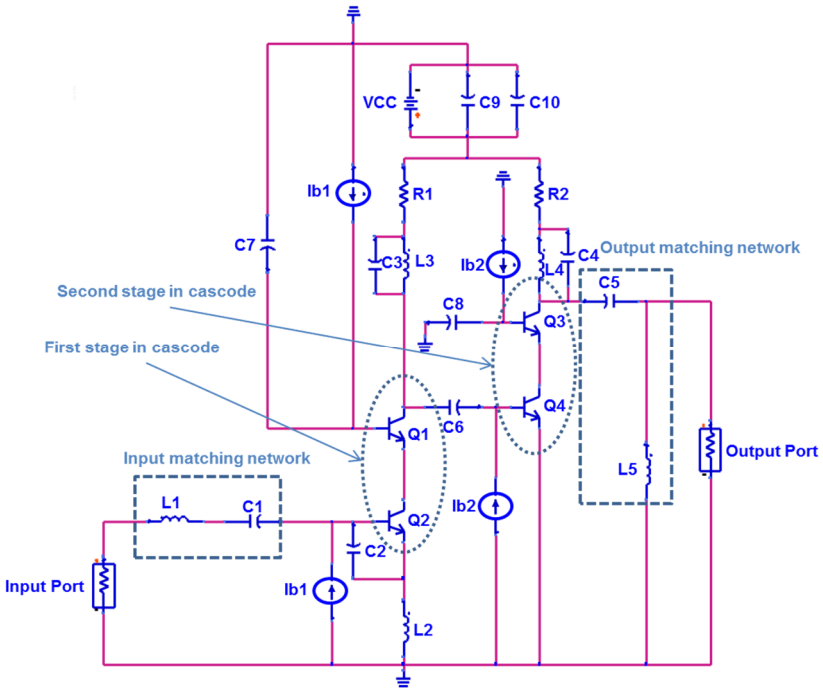

Figure 5-3: Schematic of designed dual stage cascode LNA.

The 20 GHz LNA is designed making use of a dual stage cascode configuration with inductor degeneration. With respect to other configurations, the proposed approach is used to reach higher gain with low power dissipation. For the case at hand, dual cascode stages can provide enough gain to meet the required specifications but they require a matching network at the input and output ports. As shown in Fig. 5.3, the matching networks are implemented using a series inductor (L1) and capacitor (C1) at the input port where C1 also acts as DC blocking capacitance. The series capacitor C5 with parallel grounded inductor, L5, is used to implement the output matching network. On the output port the capacitor C5 is the DC blocking capacitor. Current sources are designed with mirror configuration described in 5.1.3.Two capacitors (C9 and C10) with different values are connected in parallel with the DC voltage source to avoid DC bias loading

effects on RF part. In other words, these capacitors are used to ground the voltage used by the cascaded stages.

The small inductor (L2) is used as a degeneration inductance. The aim of using this additional inductance between the emitter connection and the RF ground is to influence the LNA input/output matching, noise matching, stability and linearity. The variation of this inductance, will allow minimizing the noise of the amplifier without compromising on its gain. In this design, a rectangular spiral inductor (L2) was employed. Its geometry was simulated with full wave FEM simulator [29]. The spiral inductor was printed on the highest metal layer (TM2) while the RF ground was located on the lowest metal layer (M1). This extra inductance provides a series negative feedback, improving amplifier third-order performance and 1dB gain compression point, at the cost of gain reduction. For the designed LNA, approximately 1 to 2 dB of gain is traded to improve linearity. In other words, typical gain in a similar design with direct emitter grounding was 24 to 26 dB, noise figure was 2.8 and stability factor was around 8.5. This gain was reduced to 23 dB with noise figure of 3.3 and stability factor increased to 20.4 by using inductive emitter degeneration. The schematic of the designed LNA is shown in figure 5-3 while values of the individual components are reported on table 5-1.

Table 5-1: Component values of the 20GHz LNA

Component	Value	Component	Value
C1	727 fF	L1	260 pH
C2	30 fF	L2	120 pH
C3	2000 fF	L3	170 pH

C4	2000 fF	L4	170 pH
C5	845 fF	L5	380 pH
C6	1020 fF	R1	40 Ohm
C7	2000 fF	R2	40 Ohm
C8	2000 fF	Ib1	30 uA
C9	250 fF	Ib2	60 uA
C10	2000 fF	VCC	3.3 V

The LNA performance should be evaluated from different angles, including the stability analysis, the input and output matching, the gain, the 1dB compression point and the power consumption.

5.1.2.1 *Stability analysis*

Stability is one of the most critical aspects for cascode LNA configurations. Stability factor analysis is performed using the K-factor whose definition K is reported in Eq.5-1.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \qquad \textbf{Eq. 5-1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

K bigger than 1 means the LNA is unconditionally stable [40]. In order to improve the stability performance, a load inductor (L4) with lower quality factor in the collector of second cascode stage. To reduce the quality factor, the overall area below the spiral inductor must be covered with a ground plane located in M1. To further increase the LNA stability, 40 Ohm resistors (R1 and R2) are also added in series to the load inductors of the first and second cascode stages in the collectors.

Another important aspect that must be carefully considered is the maximum DC current that can flow in the first and second stage. For the case at hand this current is equal to 15uA. Based on the design rules provided in the IHP SG25H3 DK, the minimum width of the lines which can handle this current flow is equal to 1 um. This value has to be used as a lower limit in the design of the spiral inductors.

5.1.3 LNA biasing

To reach 20 dB of gain, 30uA of current bias for the first cascode stage (Ib1) and 60uA of current bias for the second stage (Ib2) are required. DC current sources are realized with the current mirror technique by employing the smallest transistors included in the SG25H3 design kit, namely the IHP_npnH3shp1 which provides 30uA and 60uA of bias current for two stages as shown in figure 5-4. The 2 pF parallel capacitor is used to ground DC voltage bias at RF frequencies.

The output current is controlled by the value of the resistors namely R1, R2 and R3. The 2.5 V bias DC voltages are connected to the current mirror through the enable circuit shown in figure 5-5. This circuit is designed to switch on and switch off the LNA by turning on and off the bias currents respectively. The values of the components used in the enable circuit and current mirror for different currents are reported on table 5-2.

Table 5-2: Components value for biasing ciruits of designed 20GHz LNA.

Ib1 = 30 uA		Ib2 = 60 uA	
Parameter	Value	Parameter	Value
R1	40 Ohm	R1	40 Ohm

R2	1009 Ohm	R2	809 Ohm
R3	949 Ohm	R3	330 Ohm
R	8 kOhm	R	8 kOhm
C	2 pF	C	2 pF
V DC	2.5 V	V DC	2.5 V

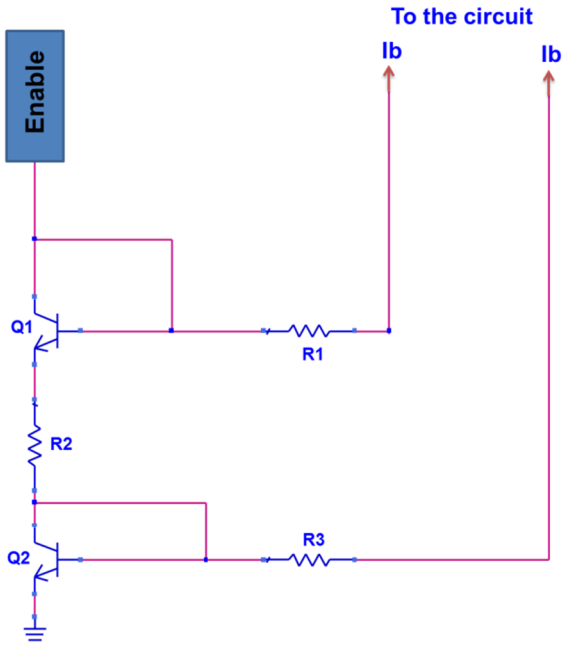

Figure 5-4: Schematic of designed current mirror.

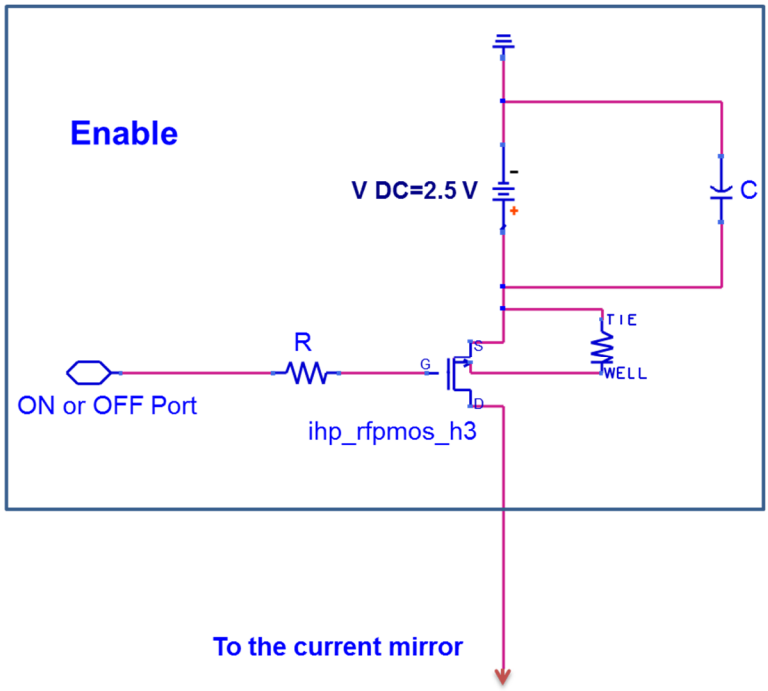

Figure 5-5: Schematic of the enable circuit employed in the current mirror.

5.1.4 Layout generation

The layout of the LNA was designed according to the procedure described in appendix A where the LNA was used as a reference case. All inductors used in the LNA are simulated using a full wave HFSS simulator and imported in Cadence layout editor to generate the LNA layout. The layout of the LNA with RF pads and DC voltage pads is shown in figure 5-6.

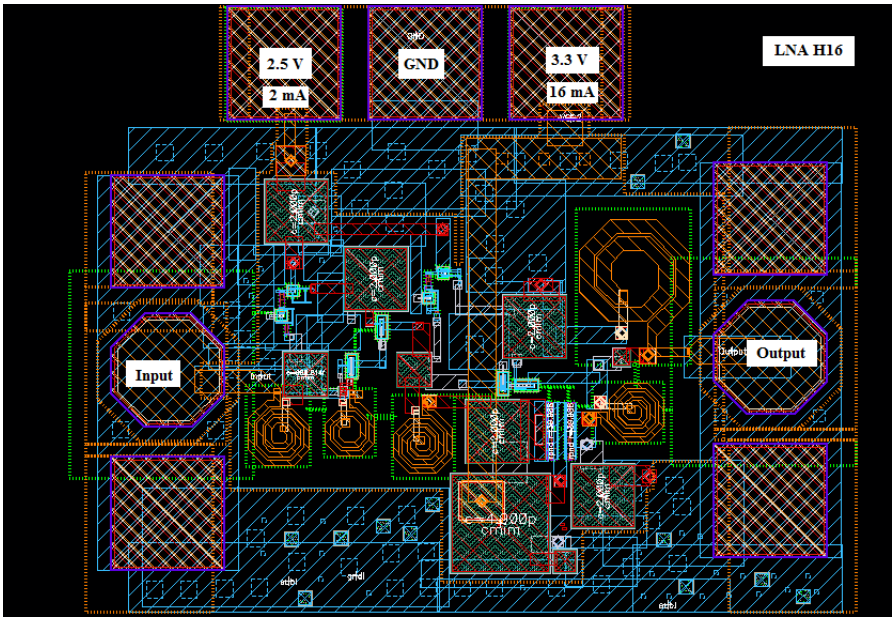

Figure 5-6: Layout of 20 GHz LNA with RF and DC pads.

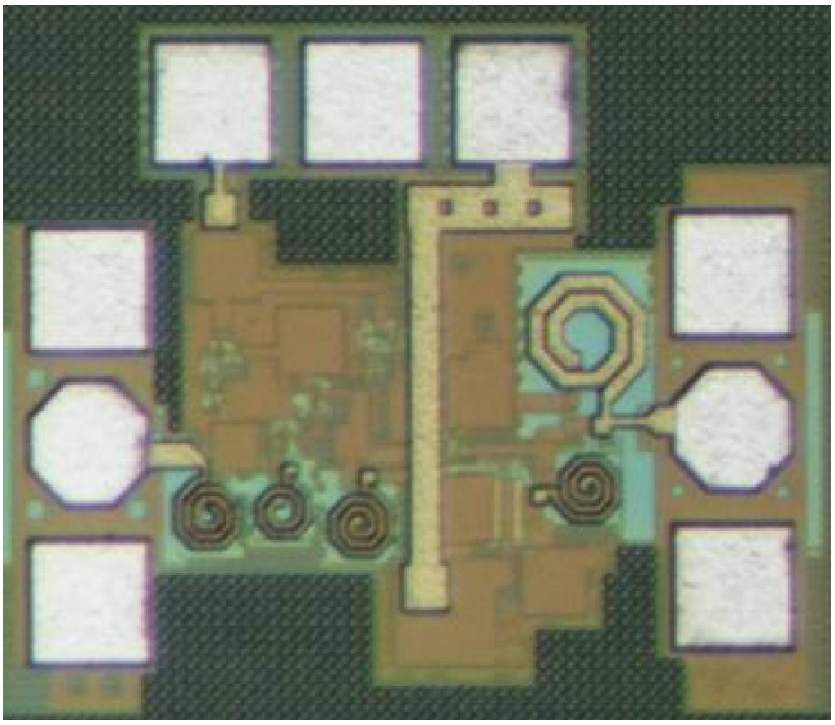

Figure 5-7: Micro photo of fabricated 20GHz LNA prototype.

5.2 Measurement and results

Figure 5-7 shows a micro photo of fabricated prototype of the 20GHz LNA. Figure 5-8 shows the measured and simulated results of the LNA gain. The maximum measured gain occurs at 20 GHz and the 3-dB bandwidth includes the entire operating band. A difference between simulations and measurements can be observed. This variation has been mainly ascribed to conductor and dielectric losses and accuracy limitations of the DK bipolar model. Another error source is surely related to the fact than only a limited portion of the layout has been analyzed through full wave simulations.

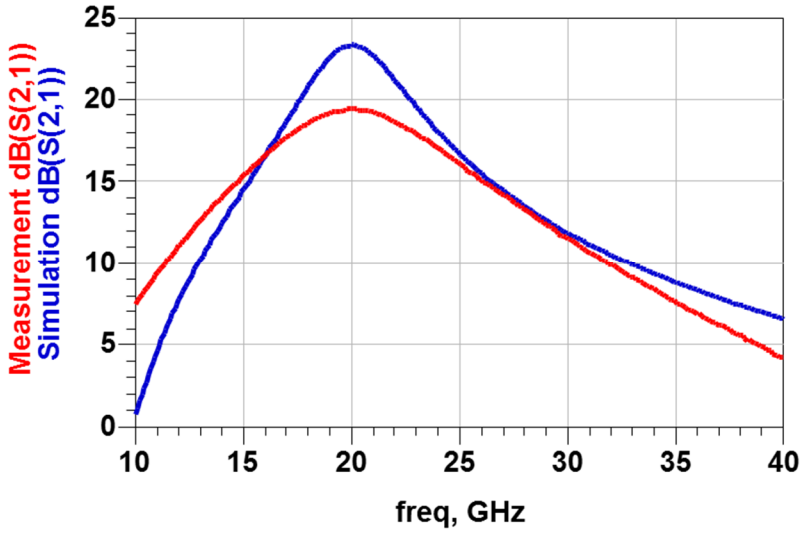

Figure 5-8: Measured and simulated gain of designed LNA.

The simulated and measured reflection coefficients at the input and output ports show similar differences as it can be observed in figure 5-9 and 5-10. However, all results satisfy the specifications required for the LNA on the operating frequency band. The measurements confirmed also that the current consumption of the LNA is very close to

the simulated values that is 15 mA and 1.5 mA for the 3.3V DC for the 2.5V DC voltage sources respectively.

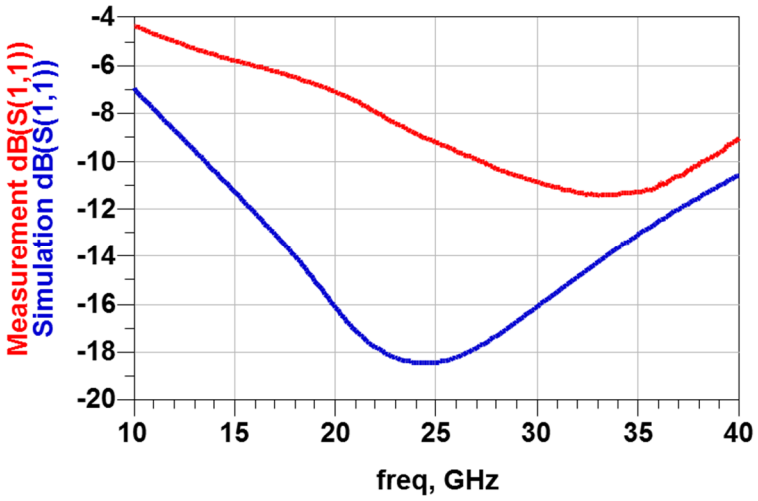

Figure 5-9: Measured and simulated input matching (S_{11}) of designed LNA.

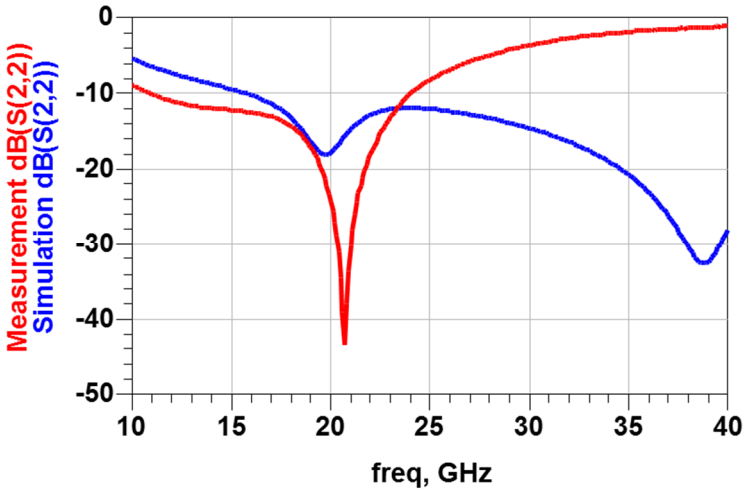

Figure 5-10: Measured and simulated output matching (S_{22}) of designed LNA.

Isolation of the designed LNA is below -50 dB as shown in figure 5-11. This parameter is very important to avoid interactions or positive feedbacks between the Rx and the Tx paths.

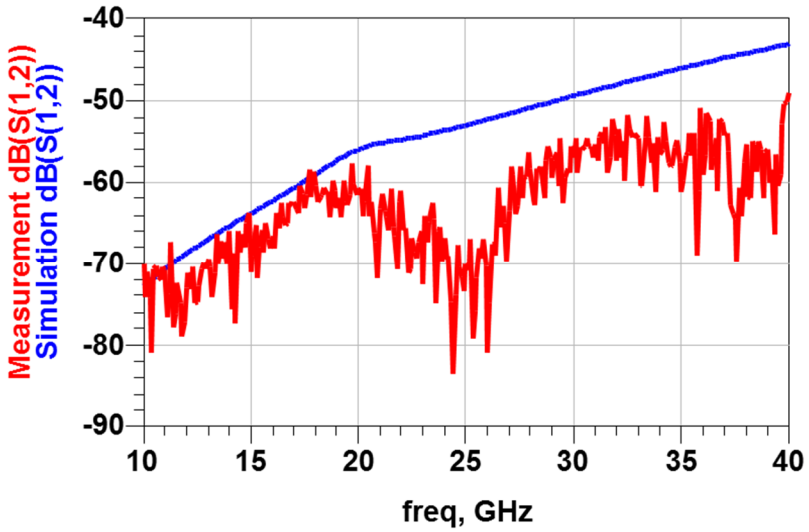

Figure 5-11: Measured and simulated isolation (S_{12}) of designed LNA.

Noise figure is below 4 as shown in figure 5-12 which is very close to the minimum achievable noise figure with this configuration.

A nonlinear analysis was also performed. The 1-dB compression point occurs for an input power equal to -20dBm as shown in figure5-13. This input power level is equal to the required input power that is mentioned in the LNA specifications.

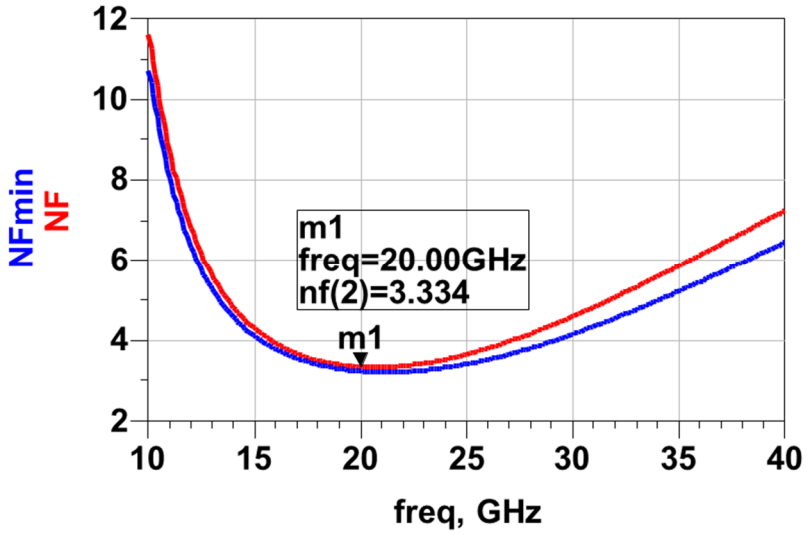

Figure 5-12: Minimum nose figure and noise figure of designed LNA.

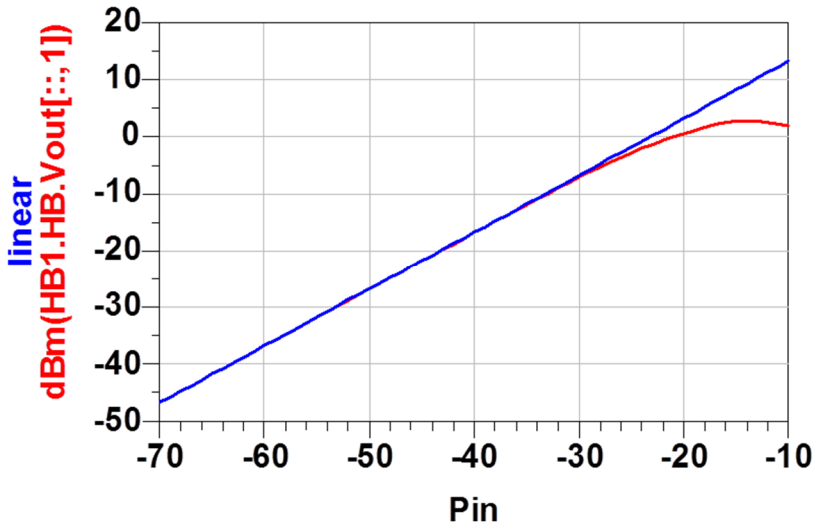

Figure 5-13: 1dB compression point of the designed LNA.

The stability factor is well above 1 over the entire operating frequency band as shown in figure 5-14 thus meaning that the designed LNA is unconditionally stable within the same band.

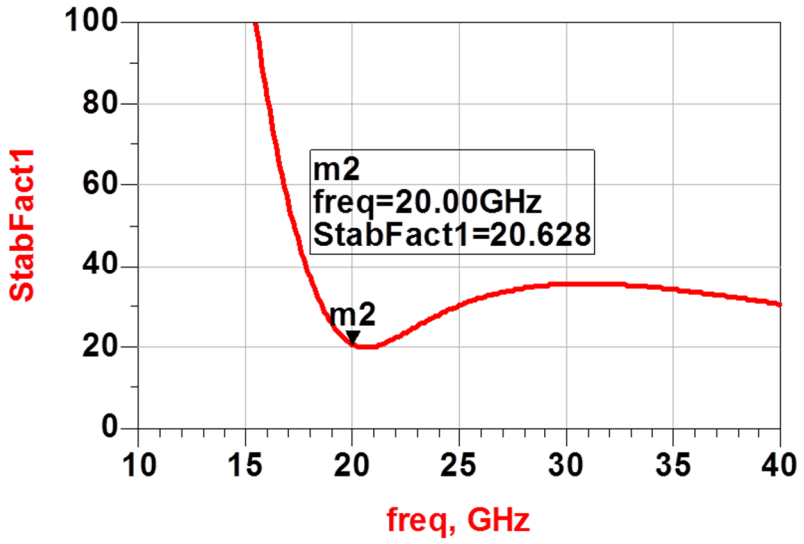

Figure 5-14: Stability factor (K) of the designed LNA.

CHAPTER 6

SWITCHING NETWORK ON CHIP

6.1 CMOS switch design

In recent years, several types of the switching devices have been developed including Radio Frequency Micro Electro Mechanical system (RF MEMS) switches, pin diodes and CMOS switches. RF MEMS switches have better isolation, low insertion loss and wide bandwidth but, due to the limited yield, the big size and the short life time, their use is not yet broadly diffused [41]. On the other hand pin diodes are reliable with very good linearity that can handle high power at higher frequency applications. However they suffer from high insertion losses, low isolation, high DC power consumption and they require an external driver needed to control the switching speed [42]. Switches based on FET transistors are typically taken into account for MMIC applications to overcome disadvantage of MEMS and pin diodes. They usually have low insertion losses, good isolation, low power consumption, small size, high switching speed and high reliability. On the other hand, their main disadvantages are related to the limited power handling capability and to the relatively complex configurations [43].

The electrical model of the NMOS transistor is shown in figure 6-1 for both on and off mode. In order to avoid signal leaking and oxide breakdown, the gate of NMOS is biased with a large resistor R_G (5 KOhm). C_s is the capacitance resulting from the capacitive effects of the source and drain with gate; R_{ch} is the on-state channel resistance which is typically low. R_{sub} is the overall substrate resistances and V_c is the bias voltage that is

equal to 0V in the ON mode or 2.5V in the OFF mode. This voltage is thus used to control the switch status.

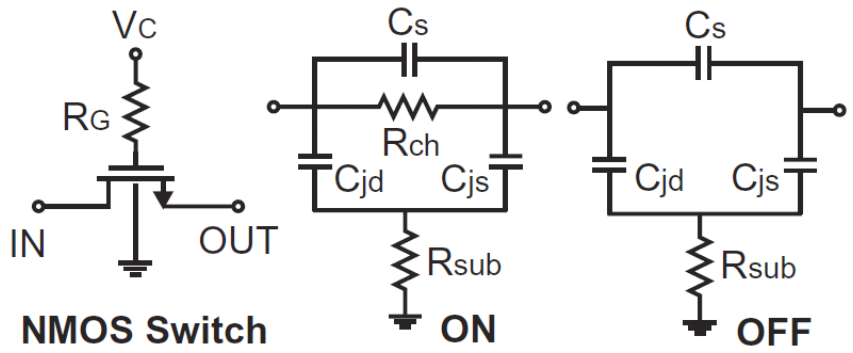

Figure 6-1: NOMS electrical model for on and off stats.

6.1.1 Single switch design

The schematic shown in Fig. 6-2 is used for both the 20 and 30 GHz switch. Indeed, the operating frequency is controlled by the series inductor, L. Therefore, by changing the inductor value (L), the switch operating frequency can be set to desired frequency band. It means that for different inductor values, different resonance and different operating frequencies band can be achieved. The single switch is designed by employing an inductor L equal to 330pH at Rx mode (SW RX) and equal to 230 pH at Tx mode (SW TX). Both inductors are realized with spiral rectangular inductors as described in Chapter 3. For the application at hand, the NOMS employed to design the single switch is the IHP_rfnmos_h3 device of the SG25H3 DK which has 15 gates.

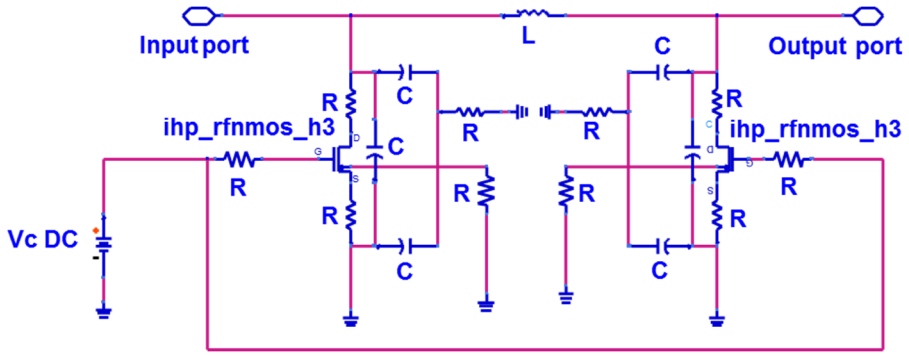

Figure 6-2: Schematic of the single switch.

The simulation results of the single switch designed for operation in Rx mode (SW RX) are shown in figure 6-3. As it can be observed, the switch provides less than -25dB isolation in OFF mode and the insertion losses are around 2dB in ON mode at 20GHz.

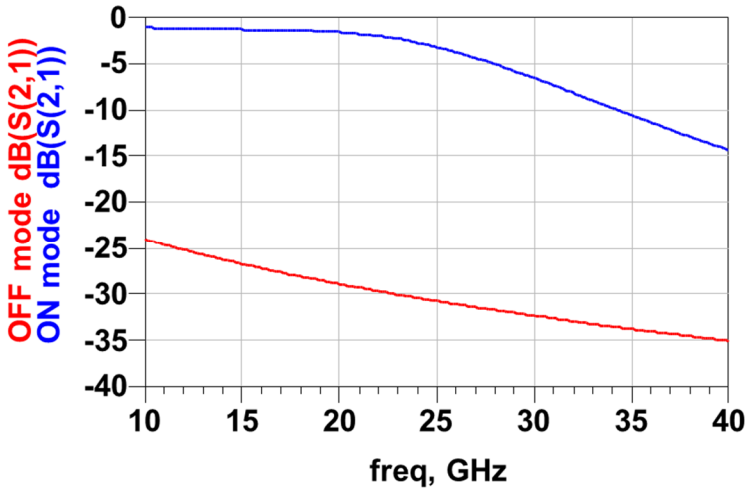

Figure 6-3: Simulation results of the single switch in Rx mode (SW RX).

The simulation results of the single switch in Tx mode (SW TX) are shown in figure 6-4. As it can be observed, the switch exhibits less than -25dB isolation in OFF mode and the insertion losses are around 2dB in ON mode at 30GHz.

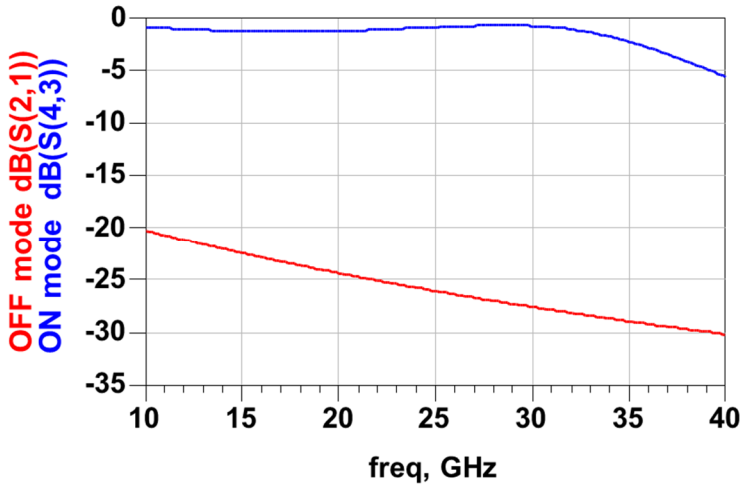

Figure 6-4: Simulation results of the single switch in Tx mode (SW TX).

6.2 CMOS switching network design

To add selectivity between the Tx and the Rx path in the Ka-band hexa core chip, a switch network is required as discussed in Chapter 4. As shown in figure6-3, the switching network should operate in Tx mode connecting the input port to the 4 Tx cores whose operating frequency is in the 30GHz band. In Rx, the signal received by the two Rx cores should be delivered to the output port in the 20GHz band. Switching network ports must be matched to 50 ohm for both states. Based on the link budget considerations, the minimum isolation required between the input/output port and the Rx port is equal to -12dB in Tx mode. A similar value of isolation is required in Tx mode between the Rx and the input/output port. The isolation between two Tx ports and the Rx ports should be at least 12dB.

In other words, when switch is in transmit mode the power flow from the distribution network is divided into two parts in a power divider to feed two different branches (upper and lower branch in figure 6-5).

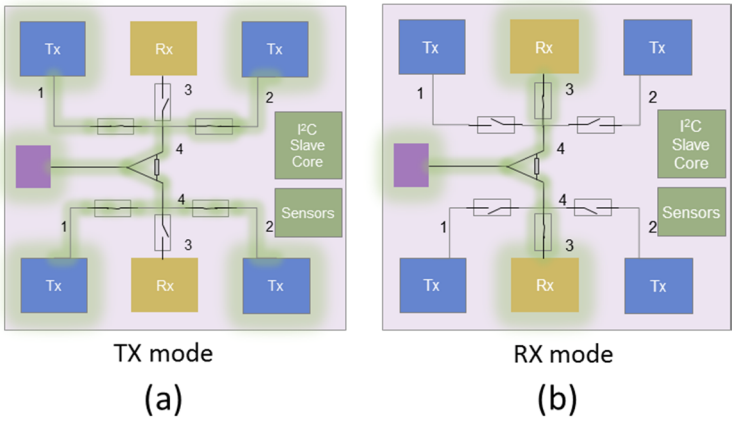

Figure 6-5: Power flow in the chip on (a) TX (b) RX mode.

The schematic of the designed switching network is shown in figure 6-6 where SW Tx and SW Rx are the single switches set to operate at 30 GHz and 20 GHz respectively, R is a resistor to provide matching when the switching network operates in Tx mode, T-lines are the transmission lines realized with lumped element components and employed to obtain better isolation. Rx, Tx and D ports show the connections to the Rx, Tx and distribution network path respectively.

The key point in the switching network design is to identify the number of the gates for each switch to have good isolation and low insertion loss at the same time. For the case at hand, 15 gates are selected for each NMOS employed in the switching network.

The π equivalent model employed to implement the T-lines with a series inductor and two parallel capacitors. Inductors are realized with rectangular spiral inductor simulated with HFSS. The lumped element power divider is also simulated with HFSS with the

exception of the 100 Ohm matching resistance. To precise design all inductors include the inductors that used in single switches, inductors from T-line model and power divider inductors are considered as a 10 port device as shown in figure 6-7 simulated with full wave HFSS simulator.

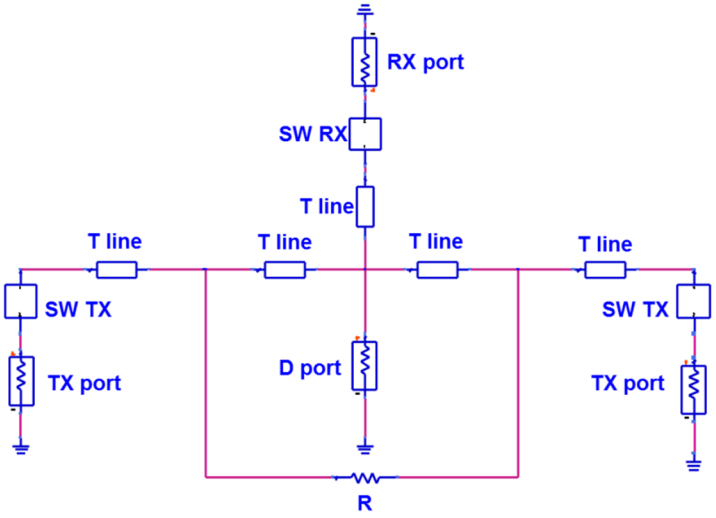

Figure 6-6: Schematic of designed switching network.

To generate a layout of the switching network, first the layout of a 10 port device where all the inductors present in the switch network were included is simulated with full wave HFSS solver and imported to Cadence layout editor where each of the 10 ports was connected to relative components as shown in schematic of the switching network and also to the remaining part of the circuit.

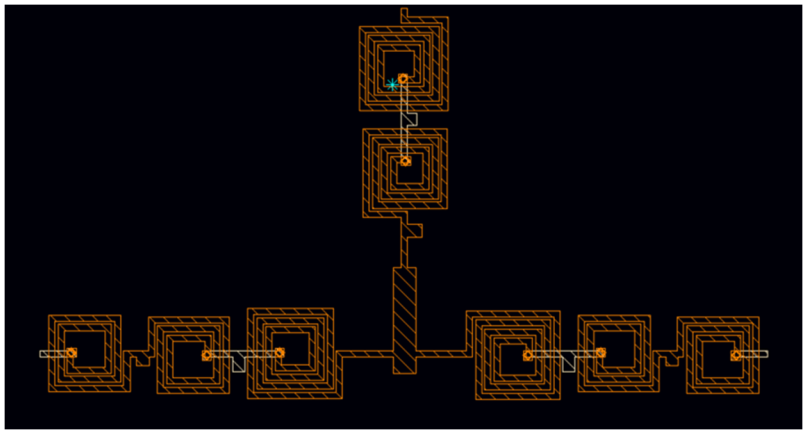

Figure 6-7: Layout of the 10 port device including all the inductors of the switching network.

The RF part of the layout for the Tx branches was designed symmetrically to avoid any phase offset between the two Tx ports. Metal 1 was considered as a solid ground plane in the area below the branches. DC bias line of the Rx single switch which used in Rx branch, connected to one DC pad and the bias lines of two Tx single switches which are used in Tx branches are connected to other DC pad. These two DC pads are employed to select the status of the switching network. The general layout generation procedure is the same as that described in Appendix A.

The layout of the designed switching networks is shown in figure 6-8. The switching network is controlled by the control voltages of the single switches. In the final prototype these voltages lines are connected together to have just one control line that can be used to enable or disable the LNA or the PA thus saving power and helping the synchronization.

The designed switching network was fabricated and measured. The prototype is shown in figure 6-9.

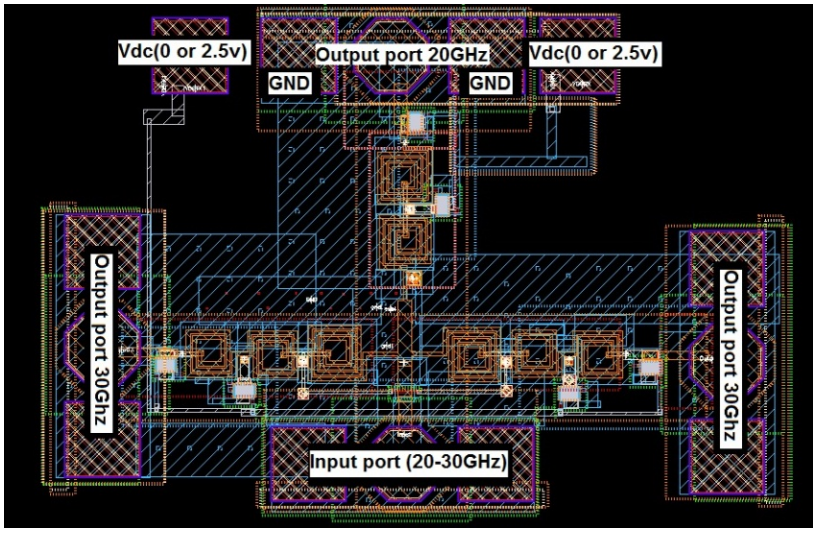

Figure 6-8: Layout of designed switching network.

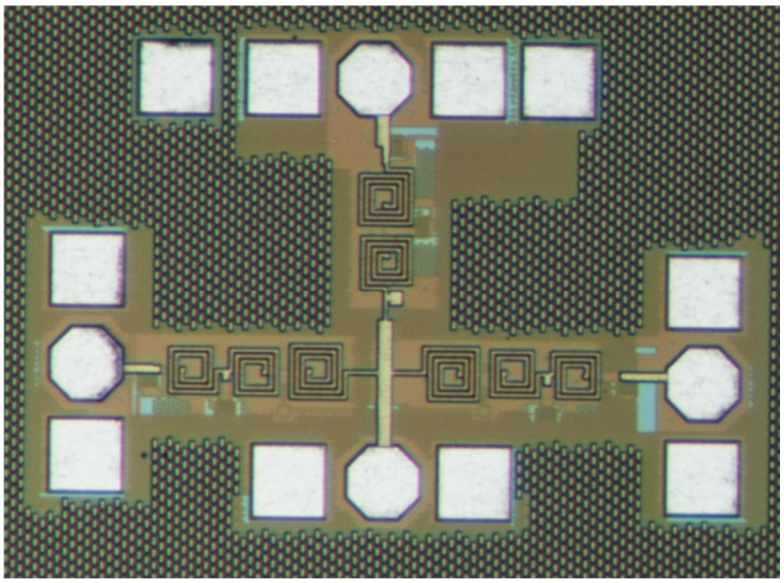

Figure 6-9: Micro photo of fabricated switching network.

6.3 Measurements and results

The numerical and experimental characterization of the switching network is done considering the two states separately. Therefore, the same layout was configured once in

Rx and once in Rx mode. The RX means that the chip operates in receive mode and the TX state means that chip operates in transmit mode.

6.3.1 RX mode results

The insertion losses of the switching network on RX mode are shown in figure 6-10.

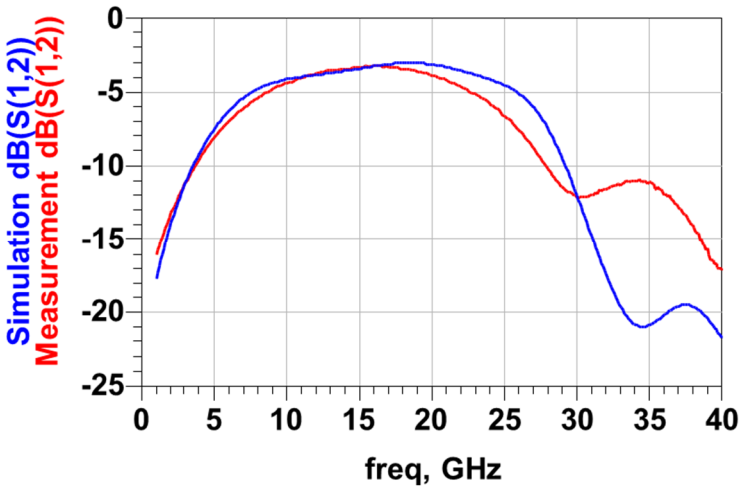

Figure 6-10: Measured and simulated results of insertion loss of the switching network in RX mode.

Measurement results are in good agreement with the simulations showing insertion losses around 3dB at 20 GHz.. The matching between the switching network in RX mode and the BFN is evaluated through the reflection coefficient shown in figure 6-11. The measurement and simulated results are coherent showing good in the whole frequency band.

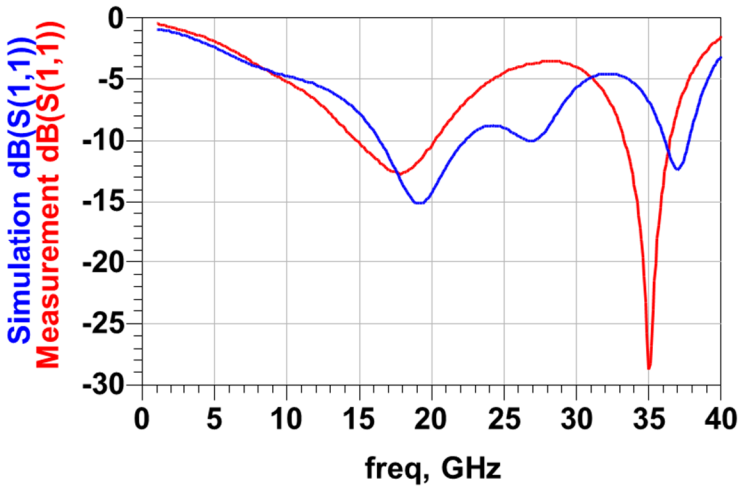

Figure 6-11: Measured and simulated results of the switching network input (D port) matching in RX mode.

Figure 6-12 show the measured and simulated matching of the switching network output port (RX port) in RX mode. Results are in good agreement showing a matching well below 10dB in the whole frequency band. Two types of isolation results are shown in figure 6-13 and figure 6-14. Figure 6-13 illustrates the measured and simulated isolation results between the RX port and the D port while the switching network is in TX mode. Figure6-14 shows the measured and simulated results of isolation between D port and TX port while the switching network is in RX mode. In both cases the isolation is below 20dB thus meaning that the switching network is providing good isolation performance.

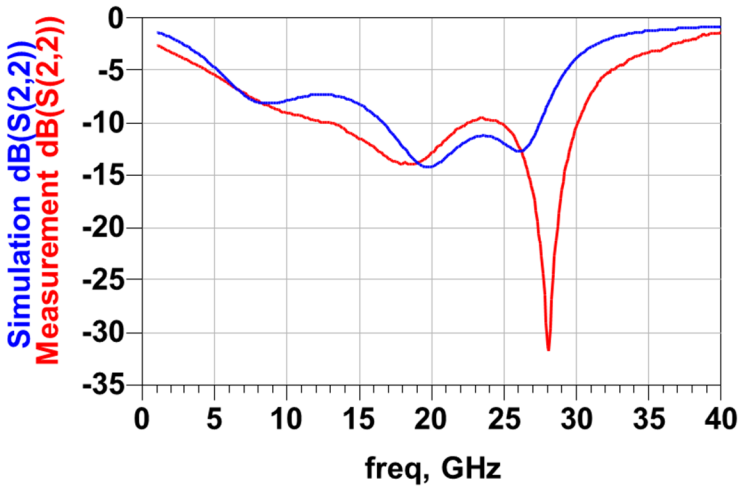

Figure 6-12: Measurement and simulation results of the switching network output matching (RX port) in RX mode.

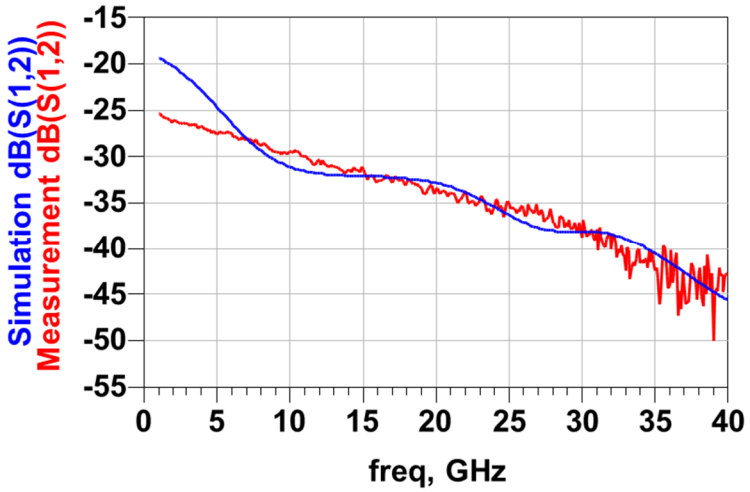

Figure 6-13: Measurement and simulation results of isolation between the switching network D port and RX port in TX mode.

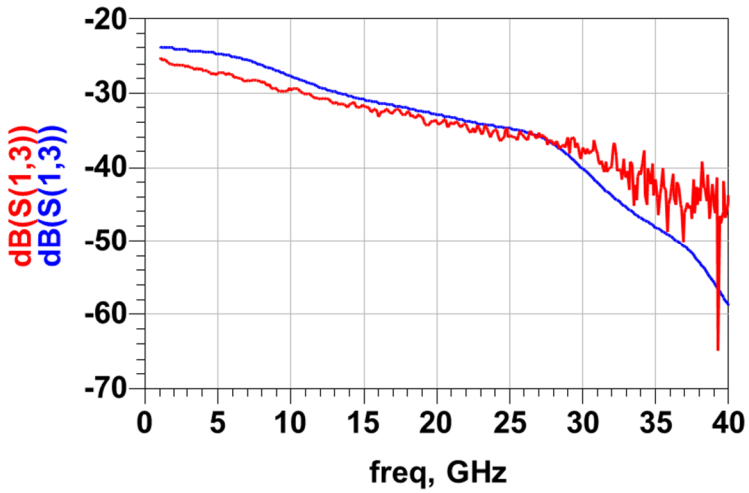

Figure 6-14: Measurement and simulation results of isolation between the switching network D port and TX port in RX mode.

6.3.2 TX mode results

Measured and simulated insertion losses are shown in figure 6-15. The proposed result includes the dividing effect of the switching network in TX mode where two 30 GHz branches are present. Therefore, the effective losses should be evaluated by adding 3dB. Measured and simulated results of the D port matching in TX mode are shown in figure 6-16.

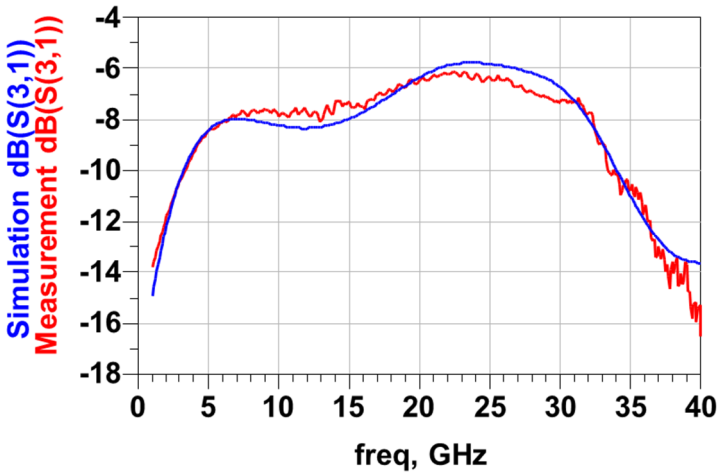

Figure 6-15: Measured and simulated results of the switching network insertion loss in TX mode.

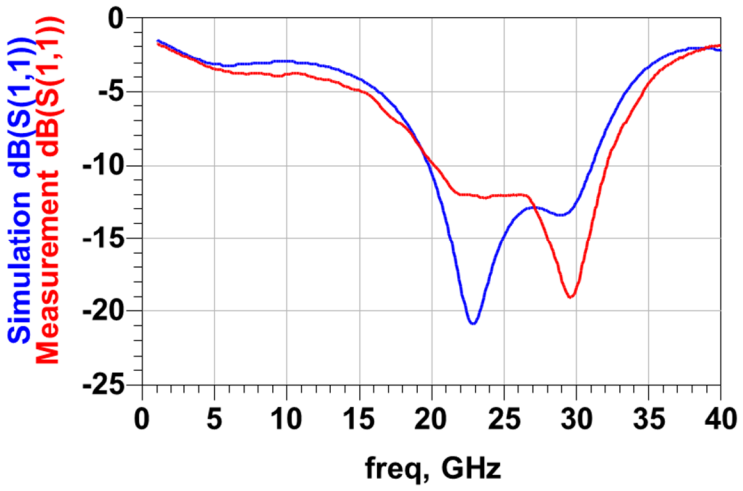

Figure 6-16: Measured and simulated results of switching network input (D port) matching in TX mode.

The measured results are in good agreement with the simulation ones showing both good matching conditions in the operating bandwidth. Measured and simulated results for the output matching network at the TX port in TX mode are shown in figure 6-17 where it can be observed also a good matching performance. The isolation performance between the D port and the TX port in RX mode, and between the TX port and the RX port in TX mode are shown in figure 6-18 and 6-19 respectively.

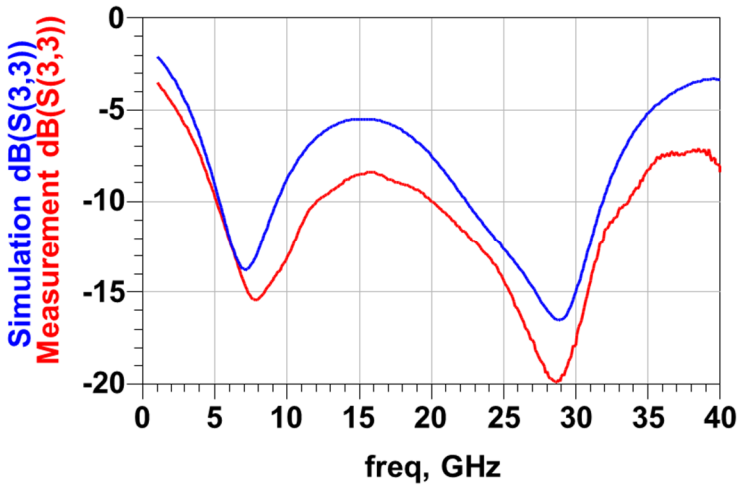

Figure 6-17: Measurement and simulation results of switching network output matching (TX port) in TX mode.

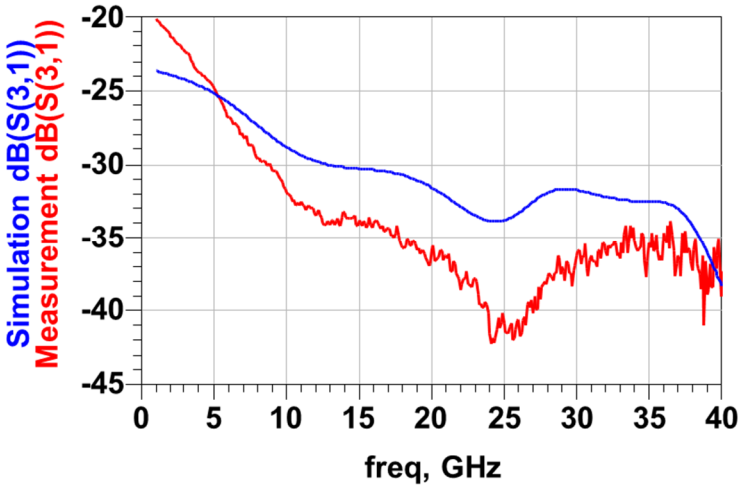

Figure 6-18: Measurement and simulation results of isolation between switching network D port and TX port in RX mode.

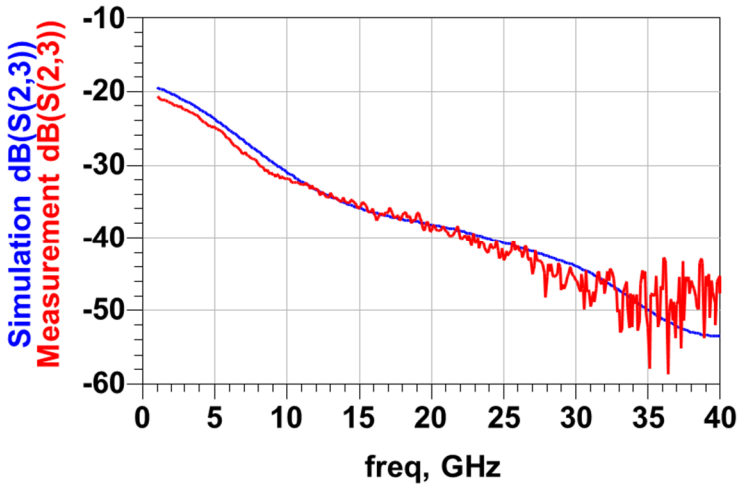

Figure 6-19: Measurement and simulation results of isolation between switching network RX port and TX port in TX mode.

The Isolation below -20dB achieved for both RX and TX mode that also can be helpful to avoid greeting loops on transmit and receive chain.

CHAPTER 7

VECTOR MODULATOR ON CHIP

7.1 Vector modulator concept

The vector modulator is a microwave device which can control the amplitude and the phase of a microwave signal. Typically, the amplitude and phase are controlled using two voltages which are tuned by an I^2C interface. Different configurations can be employed to implement a vector modulator such as the push-pull vector modulator [44], the bi-phase vector modulator [45], the variable gain amplifier combined with switched phase shifters [46]. In this chapter, will be described the Vector Modulator employed in the receiver front ends of the hexa-chip Ka-band chip. The configuration adopted in this project is based on a 90 degrees transformer combined with variable impedance loads.

7.2 Design of the 90^o transformer hybrid

The ideal 90 degree hybrid is a four port microwave component that provides equal 3dB of power division in the coupled and in the through ports while the other port is isolated form input port. Furthermore, 90 degrees of phase difference should be ideally set between the through and the coupled port. This phase difference is usually employed to design phase shifters, vector modulators, double balanced mixers and impedance matching networks [47]. A typical implementation of the 90 degree hybrid is achieved using a transformer such as the one shown in figure 7-1. The major challenges in the design and realization of the transformer are the correct evaluation of the parasitic effects, of the series resistance and of the insertion losses.

The 90 degree hybrid circuit model is shown in figure 7-2. The ideal hybrid must be able to provide 90 degrees phase difference between thru and the coupled port while the amplitude must be equal to 3 dB on both ports. The 90degree hybrid transformer can be realized with parallel winding inductors on a silicon substrate. With this method, the magnetic coupling between the parallel inductors is used to realize a 90 degree hybrid. This type of structure was optimized to operate at 20 GHz by using a FEM based full-wave simulator. The terminals of the 90 degree hybrid are located opposite each other as shown in figure 7-1 thus simplifying the circuit inter-connections.

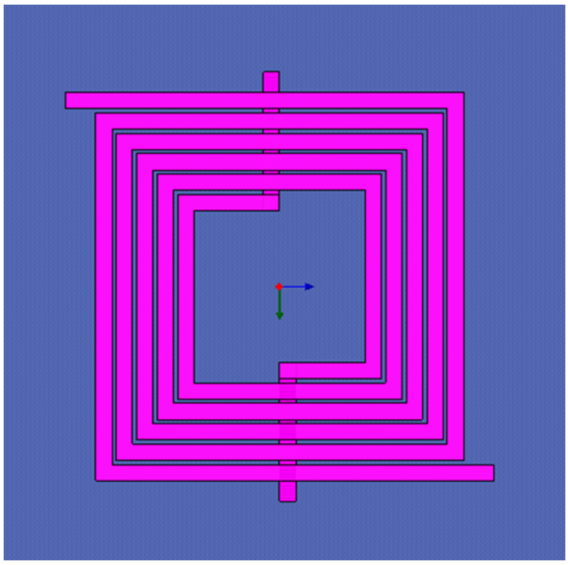

Figure 7-1: HFSS model of designed 90 degree hybrid transformer.

The geometrical parameters of the hybrid are shown in table 7-1. The equivalent circuit model of the hybrid is shown in figure 7-2. Ports 1, 2, 3 and 4 are input, trough, coupled and isolated ports respectively. The spirals provide the main inductance contributions, L_1 and L_2 which are connected between ports 1-2 and 3-4 of the coupler. Capacitive effects

between the two inductors and between the inductors and the ground plane are modeled with the capacitors C_1 and C_2.

Table 7-1: Geometrical parameters of the 90 degree hybrid coupler

Parameter	Value
Number of turns	3
Conductor width	4um
Conductor spacing	2um
Transformer total dimension	105um×105um

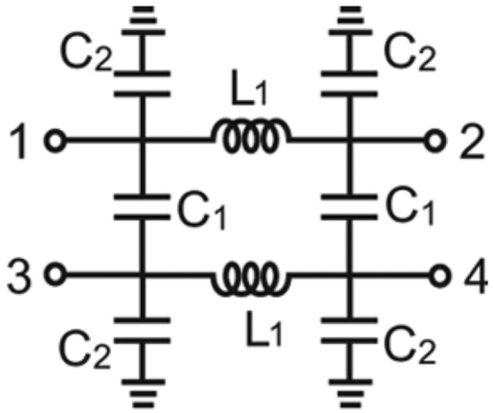

Figure 7-2: Circuit model of 90 degree hybrid transformer.

Coupling, trough, isolation and matching simulation results for the designed hybrid transformer are shown in figure 7-3. As it can be observed, the results show around 3dB of power division between the trough and the coupled port while the matching and isolation are below -15dB at 20 GHz. The simulated phase behavior of the designed

hybrid transformer is shown in figure 7-4. As it can be observed, the phase difference between port 2 and port 3 is around 90 degree at 20 GHz, as expected.

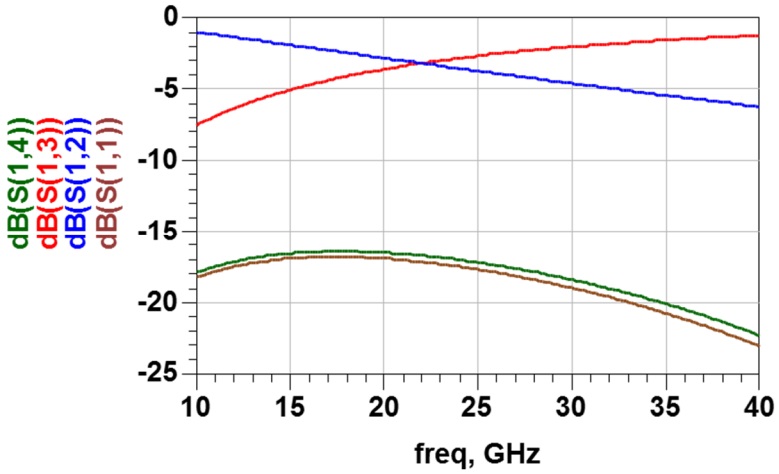

Figure 7-3: Simulated module of the S parameters of designed hybrid transformer.

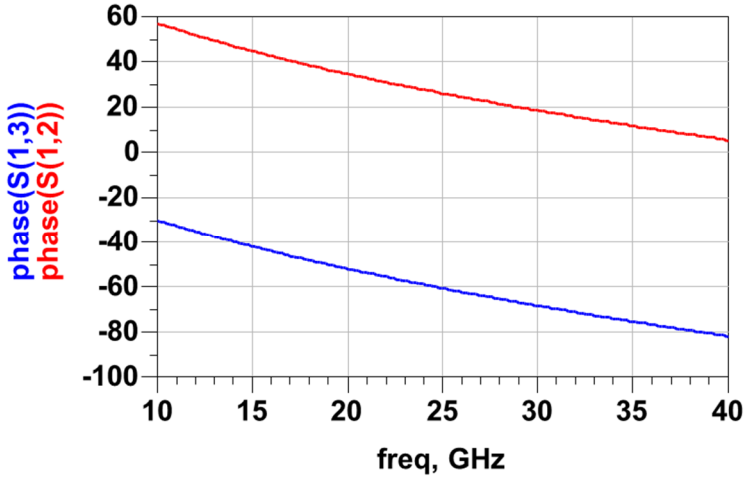

Figure 7-4: Phase response of trough port and coupled port.

7.3 Vector modulator design

The variation of the gate capacitance due to the variation of the gate bias voltages is used to create a variable impedance load as shown in Fig. 7-5. The 90 degree hybrid described in the previous section was employed to provide a wide range of output phase. On the output, a Wilkinson power divider-combiner was employed.

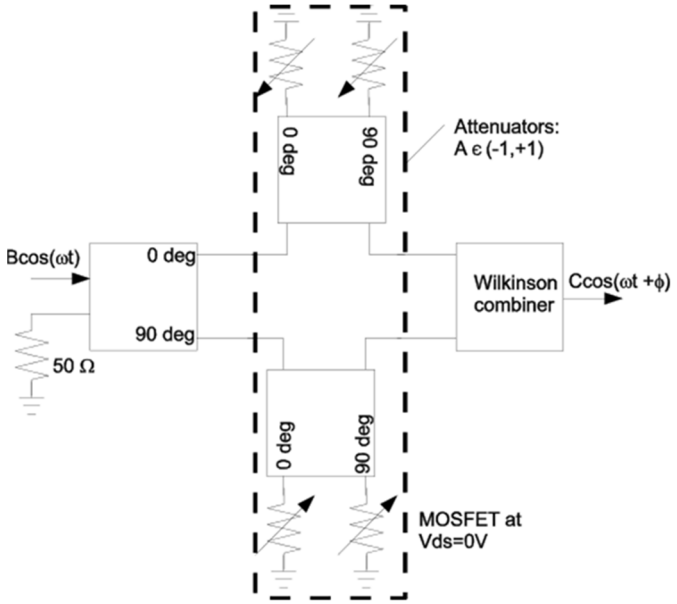

Figure 7-5: Block diagram of the vector modulator.

The variable impedance is realized by NMOS variable capacitor with series spiral inductor while NMOS bias with variable DC bias voltage. The values of the components which are used in the design of the variable impedance loads are listed in table 7-2 while their schematics are shown in figure. 7-6

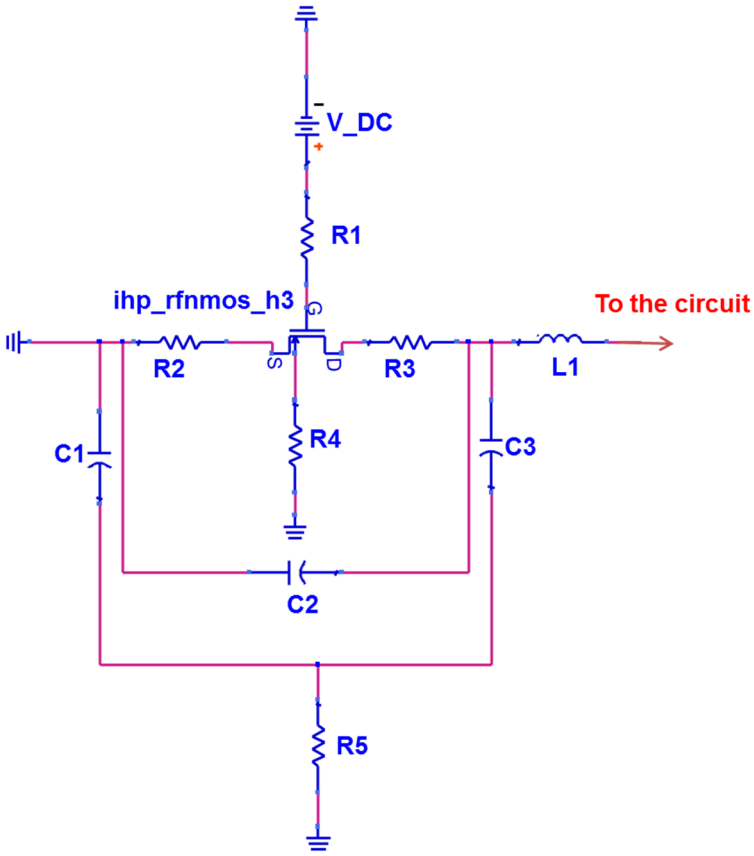

Figure 7-6: Schematic of variable impedance that is shown in figure7-5.

Table 7-2: Values of the components used in the variable impedance loads.

Parameter	Value	Parameter	Value
R1	5k Ohm	C1	77 fF
R2	1 Ohm	C2	35 fF
R3	1 Ohm	C3	77 fF
R4	5k Ohm	L1	390 pH
R5	370 Ohm	V_DC	0V – 2.5V

Two variable impedances are biased with one common DC voltage that is controlled by the I^2C data line. L1 is used to provide the variable impedance by changing the channel capacitor of the RF NMOS. R_1 is the resistor used to bias the gate and it avoids signal leaking through the gate. R_2, R_3, R_5, C_1, C_2 and C_3 are used to improve the RFNOMS model accuracy provided by design kit while R_4 is the bulk resistance of RFNMOS. The Wilkinson power divider-combiner is realized by employing a lumped element model as shown in figure 7-7. The values of designed power divider-combiner are reported in table 7-3. The inductors which were used in the power divider-combiner network were realized using rectangular spiral inductors and are simulated with HFSS. . The most critical aspects in the design of the vector modulator are the selection of the right gate number and FET transistor size and the accuracy of the hybrid model in terms of operating frequency, input and output matching. After several schematic simulations with Agilent ADS, the RF NMOS with 14 gates and with a channel size of 0.25um was selected because this value is big enough to provide a wider range of impedances while the input and output matching are satisfactory at 20 GHz.

The layout of the vector modulator, generated in Cadence following the procedure shown in Appendix A, is shown in figure 7-8. The overall size of the designed 20 GHz vector modulator is 720um×680um including the RF pads. A prototype was fabricated and measured and it is shown in figure7-9.

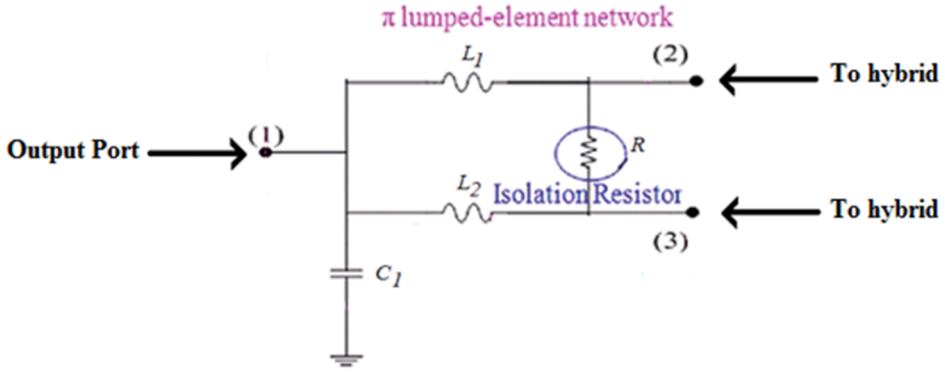

Figure 7-7: Schematic of the power divider-combiner used in the 20 GHz vector modulator.

Table 7-3: Components' values of the power divider-combiner shown in figure 7-7.

Parameter	Value
L1	230 pH
L2	230 pH
C1	155 fF
R	100 Ohm

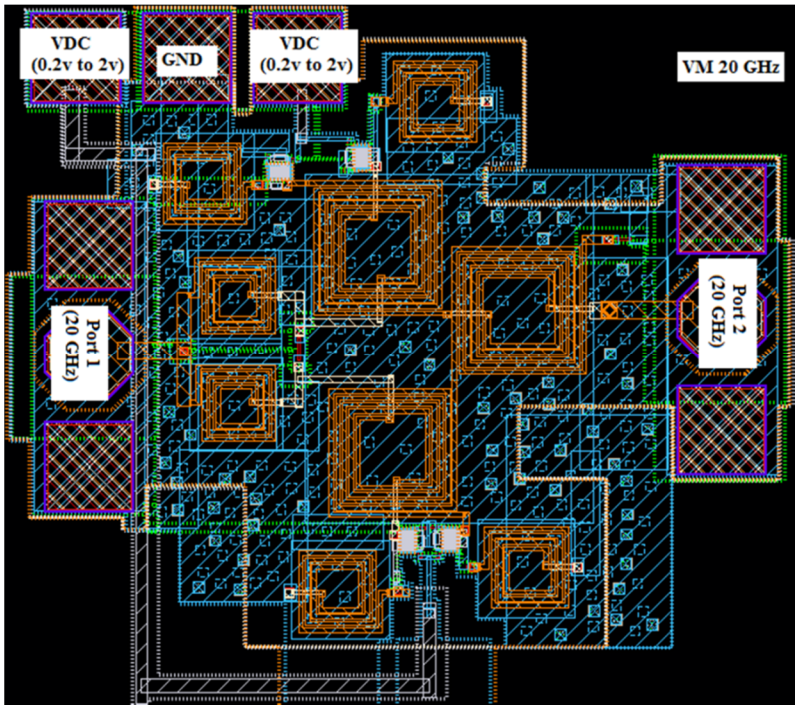

Figure 7-8: Layout of the designed 20 GHz vector modulator.

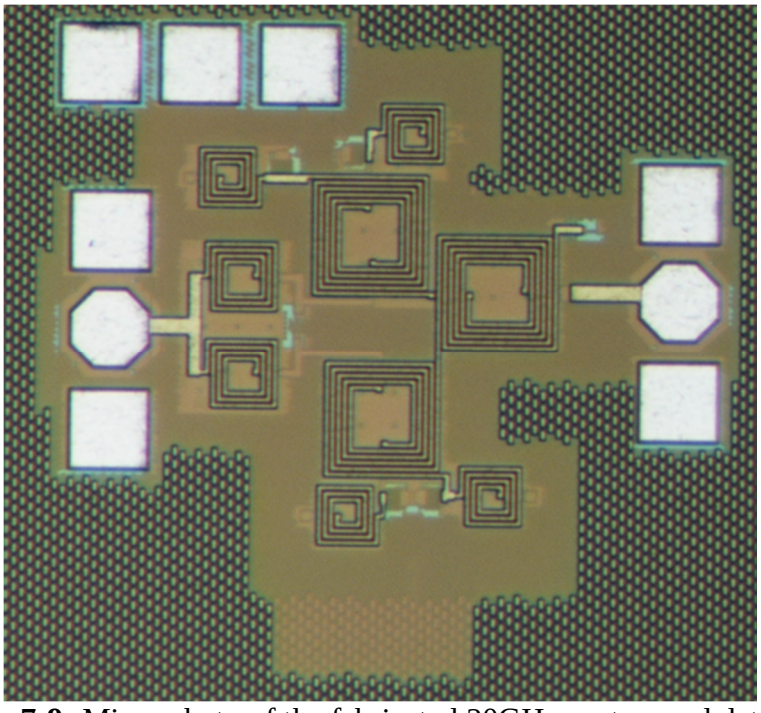

Figure 7-9: Micro photo of the fabricated 20GHz vector modulator prototype.

7.4 Measured and simulated results

To measure the designed 20 GHz vector modulator the two bias voltages are varied within the range from 0V to 2.5 V with steps of 0.2V. For each bias voltage combination, the output amplitude and phase is measured. The results of this process, casted in terms of the transmission coefficient S_{21}, are shown in figure 7-10.

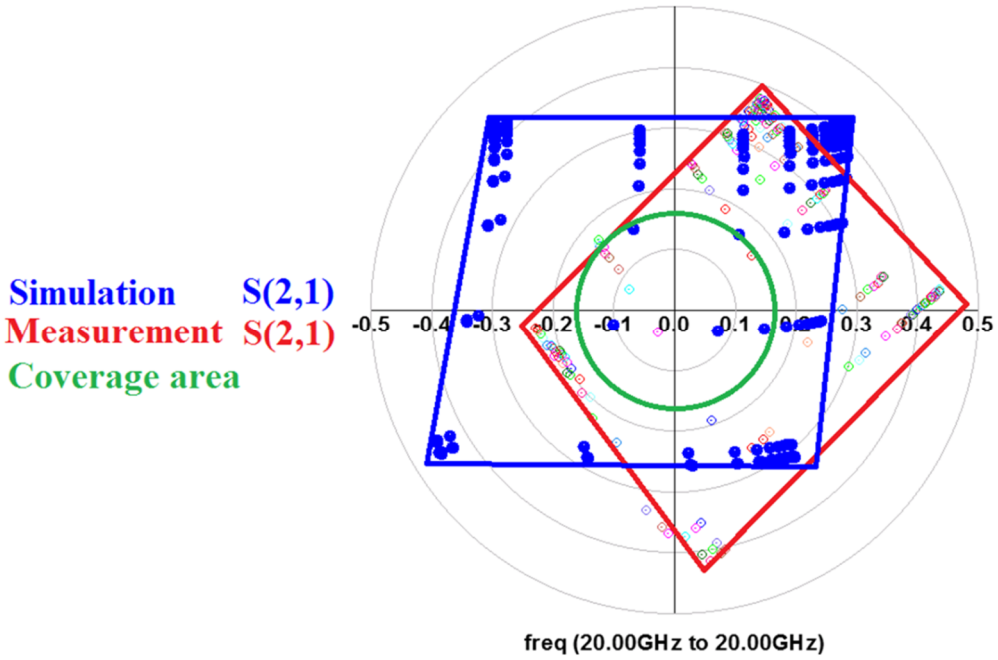

Figure 7-10: Measured and simulated results of the 20 GHz vector modulator and the relative coverage area.

Both simulated and measured results show a full coverage of the four quadrants thus proving a full control of both amplitude and phase. The different rotation of the coverage area is not significant and it is due to uncompensated or un-calibrated phase differences. Input matching at four critical voltages (0V and 2.5V) states is shown in figure 7-11. As it can be observed, the input matching is below 10 dB for all states. The output reflection coefficient at the same voltages is reported in figure7-12 showing an amplitude lower than -10dB.

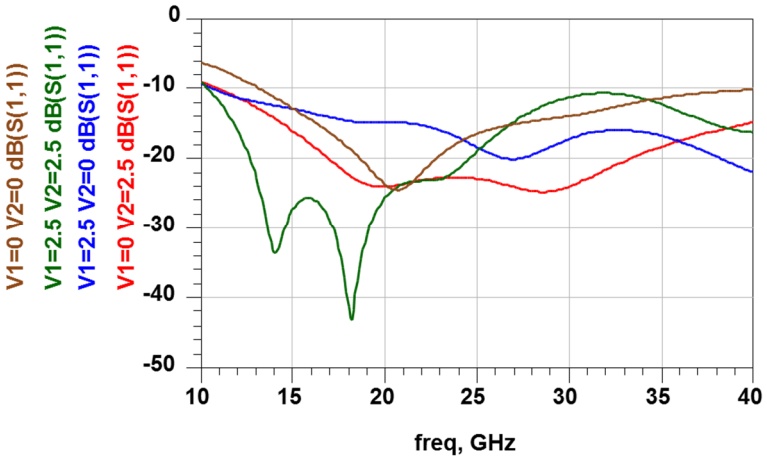

Figure 7-11: Measured input matching of the vector modulator at four different bias conditions.

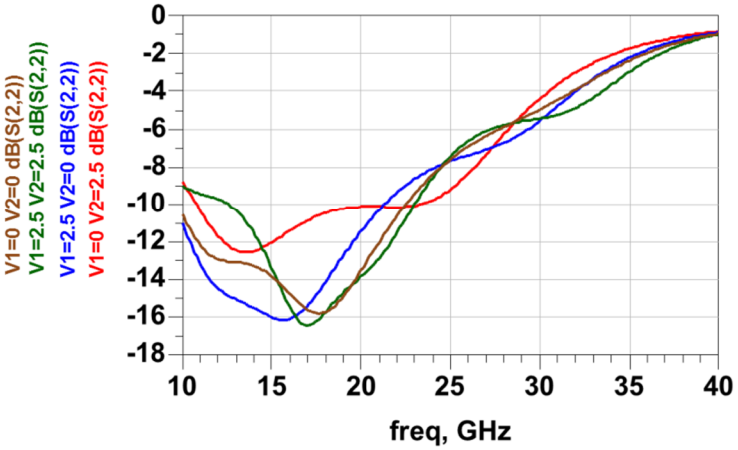

Figure 7-12: Measured output matching of the vector modulator at four different bias conditions.

CHAPTER 8

BROADBAND POWER DIVIDER-COMBINER ON CHIP

8.1 Wilkinson power divider-combiner on chip

On-chip power division is required to implement dual-band multicore chips including both Rx and TX elements as discussed in Chapter 3. As was mentioned in Chapter 2, in Ka multimedia services the Rx and Tx bandwidth are 19.7 – 21.0 GHz and 29.5 – 30.8 GHz respectively. Therefore, to cover both channels the operating bandwidth of the on-chip power combiner/divider should be greater than 40% thus making this design particularly complex. The isolation between output ports is also a crucial design consideration as it reduces the spurious coupling among active components and actually decreases the out-of-band oscillations and positive feedback. To fulfill these two important requirements, it is proposed a design approach based on the optimization of the equivalent lumped element model of the Wilkinson power divider using the Method of Least Squares (MLS). First, a simple lumped component equivalent model of power divider is defined and the expression of its S matrix is obtained. An error function is constructed in terms of the required transmission and reflection characteristics. The input and output impedances of the power divider can be selected arbitrarily. The minimization of the error function is then performed by a combination of genetic algorithm and conjugate gradient methods, which are used to define the values for the lumped components. In a second phase, the lumped elements are used as a starting point to design the on chip components. The proposed technique was applied to design wideband MMIC power divider. A prototype of the wide band power divider was also fabricated and

measured. The comparison of results of MLS design, full-wave simulation and measurements are presented to show that the proposed circuit configuration and the optimum design procedure are effective and could have potential practical application.

8.2 Broadband power divider-combiner design

The Wilkinson power divider shown in figure 8-1a is taken as reference. Its equivalent model based on lumped components is presented in figure 8-1 b. Ports 1, 2 and 3 are designated as input and outputs ports.

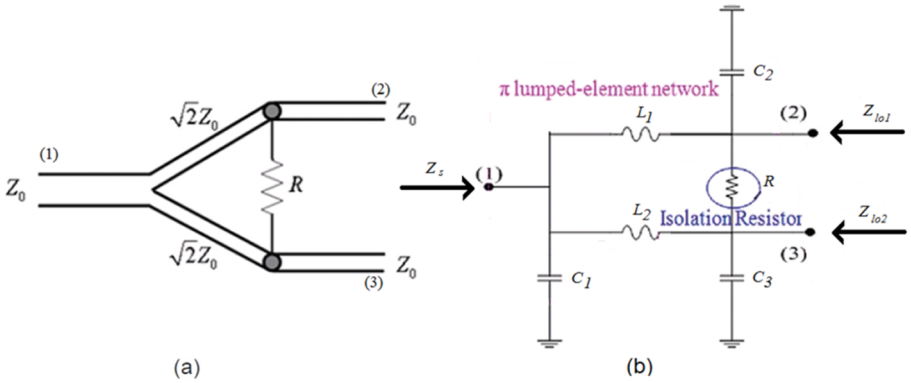

Figure 8-1: A power divider based on: (a) distributed elements; (b) lumped components.

The equivalent circuit can be used to derive the scattering matrix of the Wilkinson divider from the impedance matrix [48]. The equivalent impedances Z_s, Z_{lo1} and Z_{lo2} are defined at the input and output ports of the divider respectively. Their value can be easily obtained in terms of the equivalent inductances L_1 and L_2, capacitances C_1, C_2 and C_3 and resistance R. Once the scattering parameters are obtained from the ABCD matrix, the error function can be written in terms of the reflection coefficients at the three ports, namely S_{11g}, S_{22g} and S_{33g} while the goal function is expressed as S_{11f}, S_{22f} and S_{33f}. If the

operating bandwidth of the power-divider is comprised between f_1 to f_2, the error function e_{PD} can be written as **Eq. 8-1.**

$$e_{PD} = W_1 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{21\,f_k} - S_{21g} \right| + W_2 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{31\,f_k} - S_{31g} \right| + W_3 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{11\,f_k} - S_{11g} \right| + W_4 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{22\,f_k} - S_{22g} \right| + W_5 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{33\,f_k} - S_{33g} \right| + W_6 \sum_{k=k_{f1}}^{k_{f2}} \left| S_{23\,f_k} - S_{23g} \right| \quad \textbf{Eq. 8-1}$$

Where W_i are weighting factors and the index k is used take K samples within the power divider frequency range. The error function can be then minimized using a customized version of the MLS algorithm as shown in [49]. For the case at hand, the MLS procedure was employed in Advanced Design System (ADS) and it was used to optimize the values of the power divider lumped elements, namely L_1, L_2, C_1, C_2, C_3, R, Z_s, Z_{lo1}, Z_{lo2}. Once the optimal values were obtained, they were turned into the corresponding components.

On the SG25H3 technology the maximum and minimum values of the inductors, capacitors and resistor in the circuit model have been fixed as 100pH<L<1nH, 25fF<C<2pF, 30Ω<R<25kΩ. The specifications of this second example reflect the Ka SatCom requirements and they can be explicated defining the following goal function: S_{31g}= S_{21g}=-3dB, f_1=17GHz, f_2=33GHz, K=1601, S_{11g}=-10dB, S_{22g}=-10dB, S_{33g}=-10dB, S_{23g}=-10dB, Z_s=50Ω and Z_l=50Ω and W_i= 1.

Table 8-1: Initial and Optimized values of designed power divider-combiner components.

	L (pH)	C (fF)	R(Ohm)
Initial values	140	40	20
Optimized values	310	80	100

A prototype of the on-chip power divider shown in figure 8-2 was fabricated and tested.

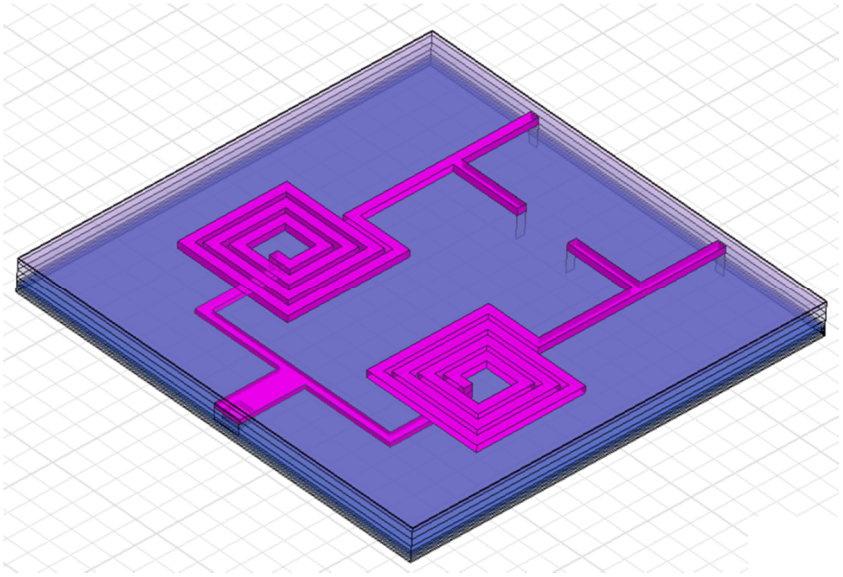

Figure 8-2: Full wave model of the designed power divider-combiner.

The layout and the micrograph are shown in figure 8-3 and figure 8-4 respectively. The overall chip size is equal to 195 µm × 200 µm excluding the three pads.

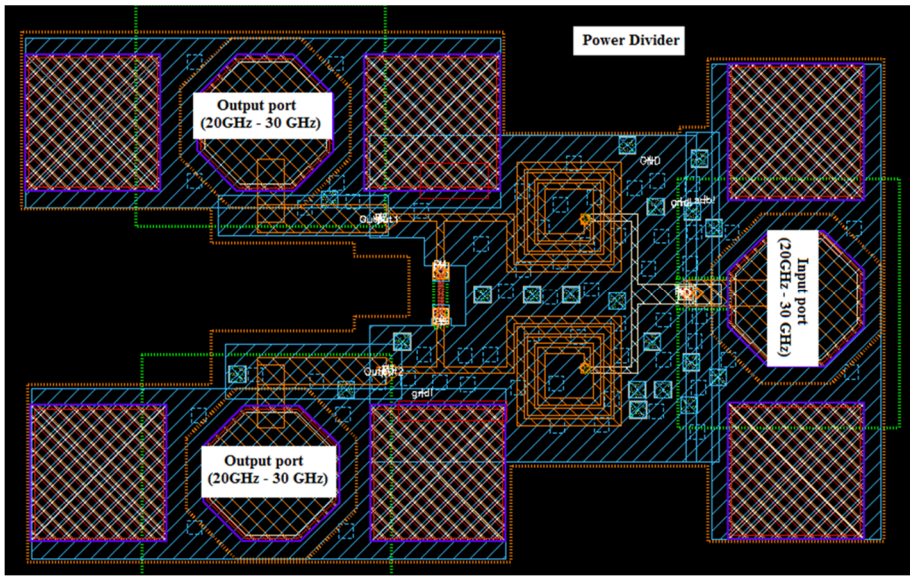

Figure 8-3: Layout of the designed power divider-combiner.

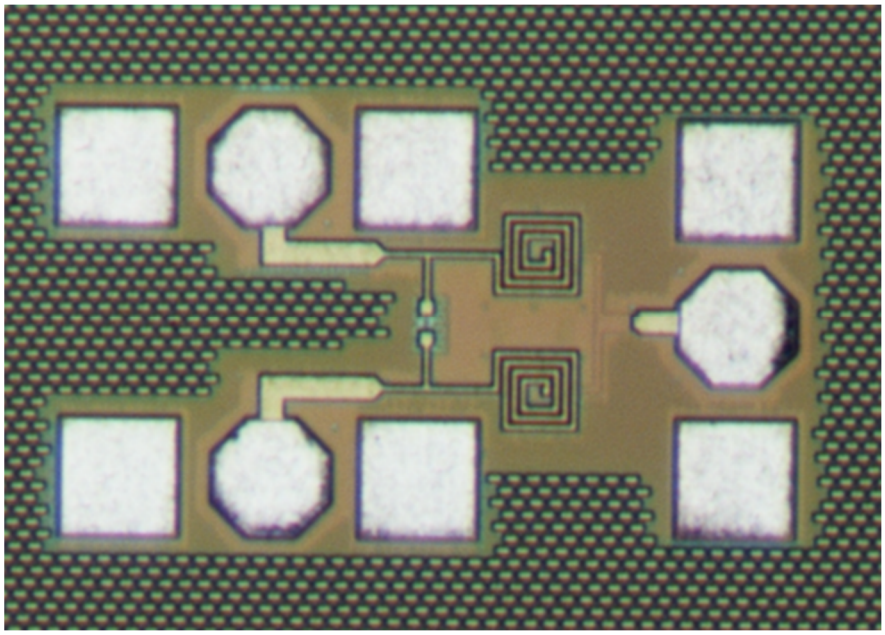

Figure 8-4: Micro photo of the designed power divider-combiner.

8.3 Measurement and results

As it can be seen from the schematic simulation results shown in figure 8-5, figure 8-6, figure 8-7 and figure 8-8 all scattering parameters of the optimized circuit satisfy the goal function. The full wave simulation was done taking into account the actual geometry of the MMIC power divider as shown in figure 8-2. In this case, the full layout is included into the full-wave analysis with the exclusion of the lumped resistor. The FEM based simulation results are casted in terms of S-parameters and imported into a circuital simulator where the resistor design kit model is included. Simulation results are superposed to MLS results in figure 8-5, figure 8-6, figure 8-7 and figure 8-8. As it can be observed, the two simulations are in good agreement and only a limited discrepancy between the simulated results and the goal function can be noticed in case of the FEM based results.

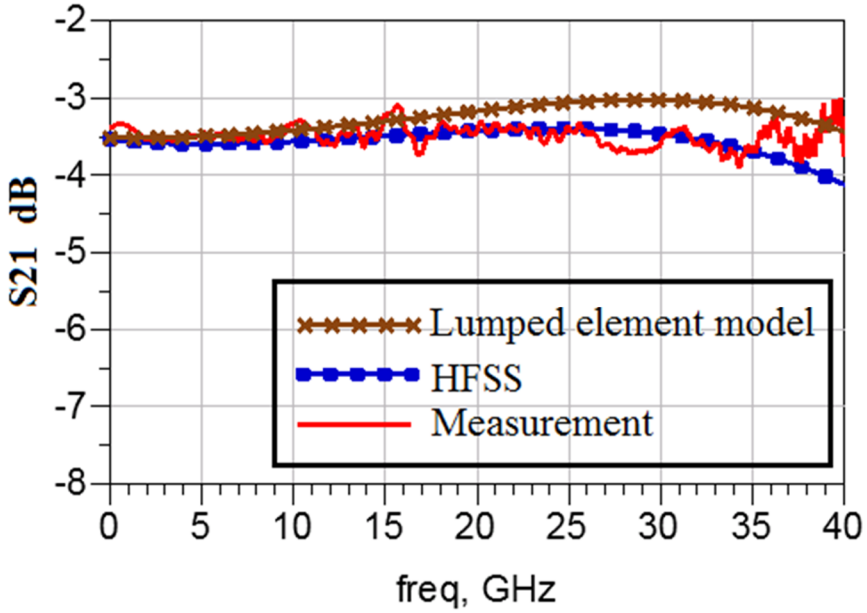

Figure 8-5: Power division coefficient of designed power divider-combiner.

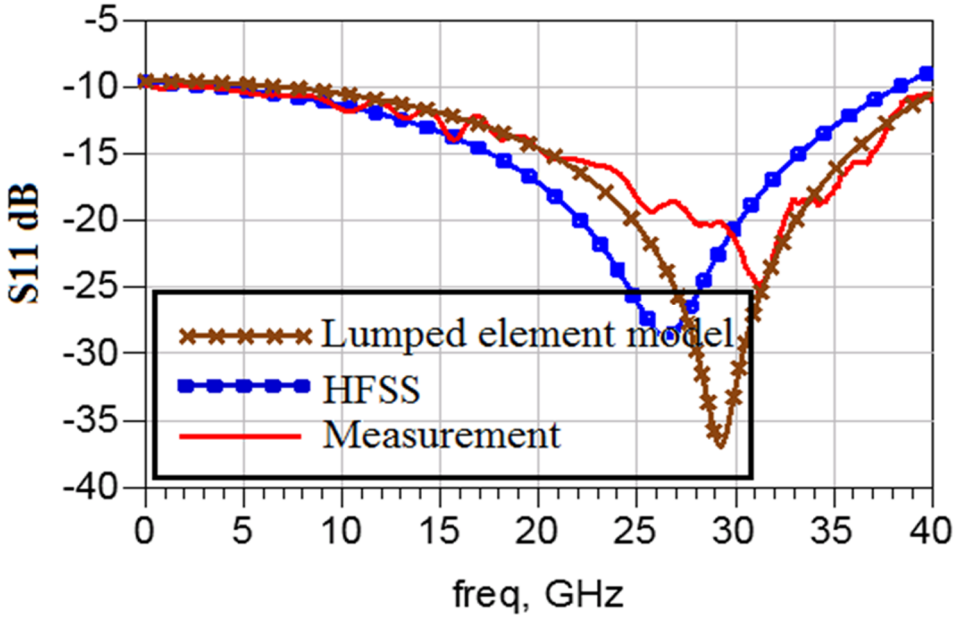

Figure 8-6: Input matching of designed power divider-combiner.

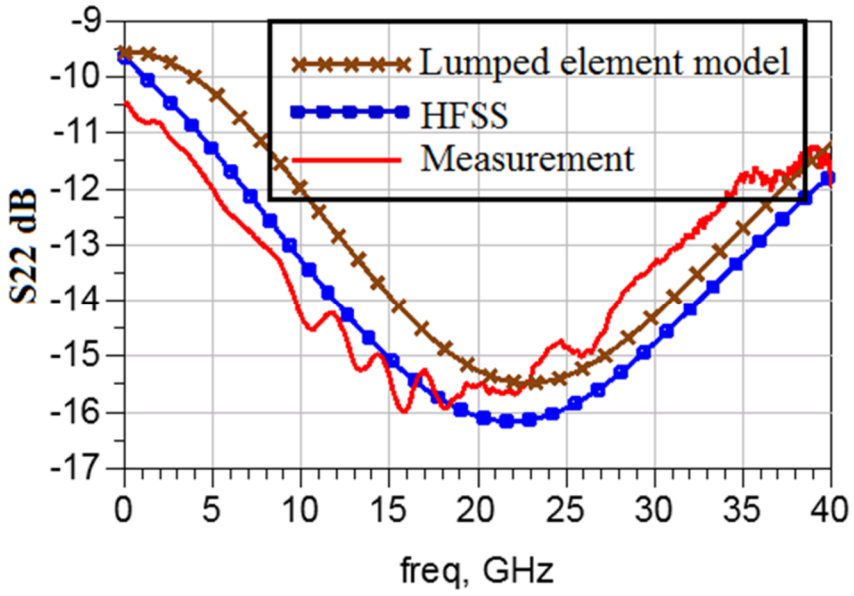

Figure 8-7: Output matching of designed power divider-combiner.

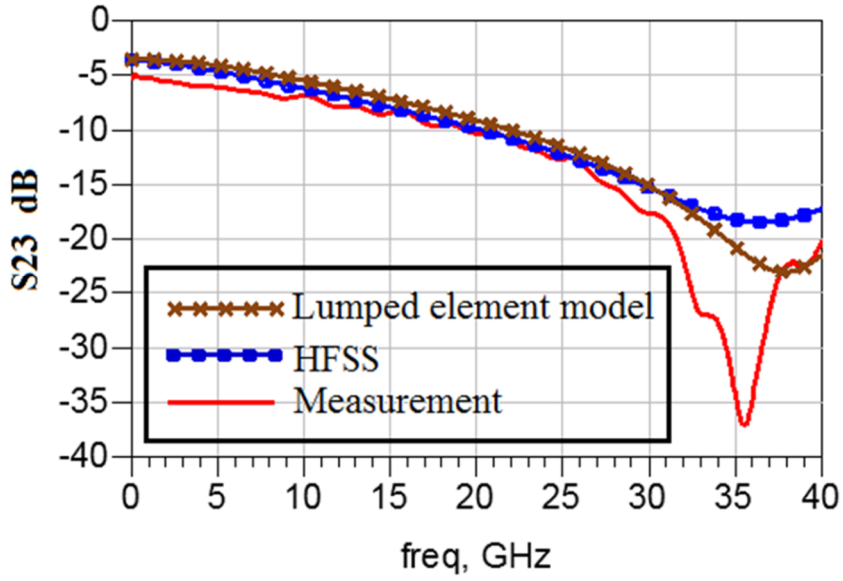

Figure 8-8: Isolation of designed power divider-combiner.

Measurements have been taken and results are shown in figure 8-5, figure 8-6, figure 8-7 and figure 8-8. Comparison with MLS and full wave simulations shows that the prototype

behavior well matches the numerical results. The reflection coefficient at the input port is well below 10dB between 5 and 40 GHz but the isolation between the two output ports remains below 10dB only between 18 and 40GHz.

CHAPTER 9

DIPLEXER NETWORK ON CHIP

9.1 Diplexer design

In this chapter the design and experimental characterization of a four-port diplexer will be presented. The proposed on-chip diplexer network is conceived as an alternative solution to the switching network described on Chapter 6. Its requirements, derived from the link budget analysis, are similar to those of the switching network both in terms of performance and size. A summary of its functional description is given in figure 9-1.

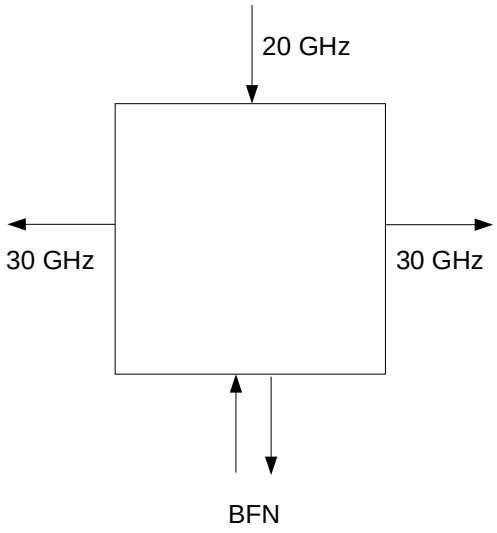

Figure 9-1: Functional description of the diplexer network.

The proposed network splits the received/transmitted signal into two paths. One path connects receiver front end operating at 20 GHz to the BFN while the transmitted signal at 30 GHz is delivered to two transmitting antenna elements. The two channels have a significant bandwidth separation and the isolation requirements are not critical.

Indeed, the real isolation between the transmitter and the receiver cores are enhanced by the LNA and PA unilateral behavior.

The diplexer network is realized using as a starting point three band-pass filters, one for each channel. The filter order was chosen making a trade-off between the out of band response and the size. The best compromise is achieved by employing filters of the third order. Each filter was first designed using classical filter synthesis methods [50]. The schematics of the two filters are shown in figure. 9-2 and 9.3 where are reported also the values of inductances and capacitances.

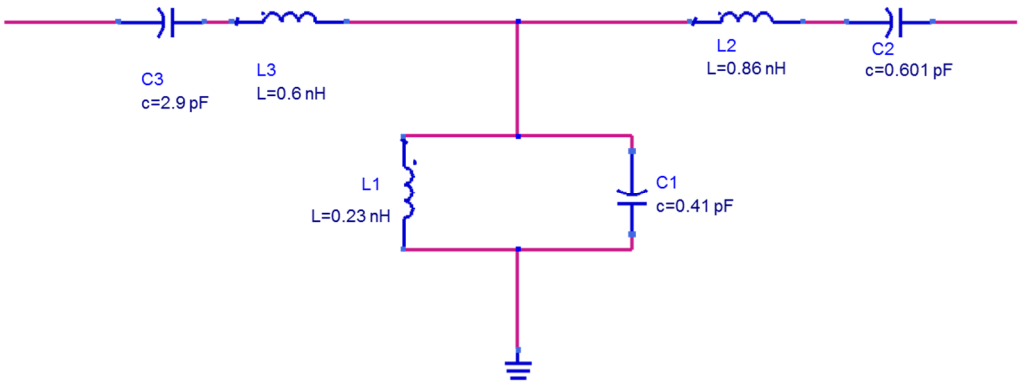

Figure 9-2: Band-pass filter schematic for the two 20 GHz branch.

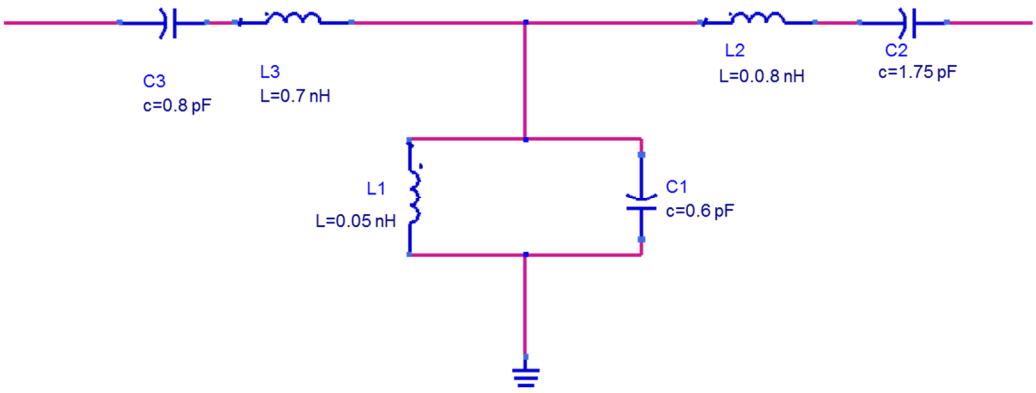

Figure 9-3: Band-pass filter schematic for the 30 GHz branches.

The responses of the 20 GHz and 30 GHz filters are reported on Fig. 9-4 and 9-5 respectively.

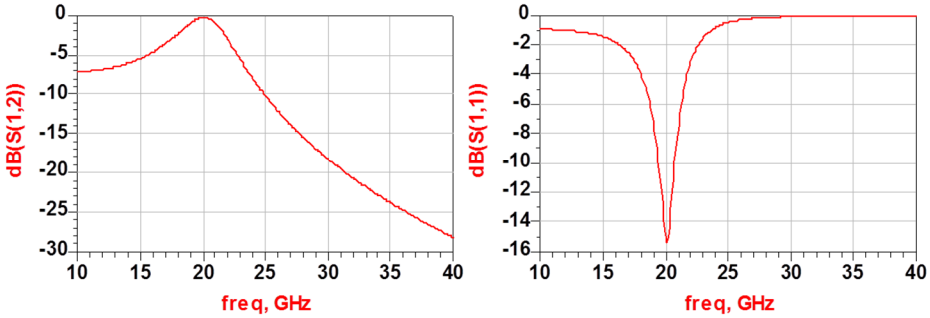

Figure 9-4: Response of the 20 GHz lumped element band-pass filter.

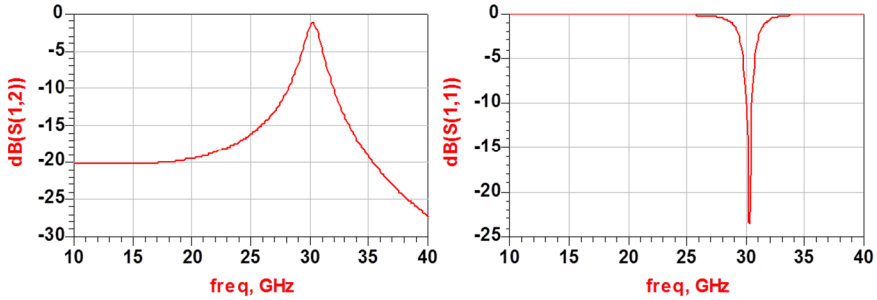

Figure 9-5: Response of the 30 GHz lumped element band-pass filter.

9.2 Layout generation

Before generating the layout, the three ideal filter branches were integrated into a single schematic and the performance optimization of the circuit was performed obtaining the result shown in figure 9-6.

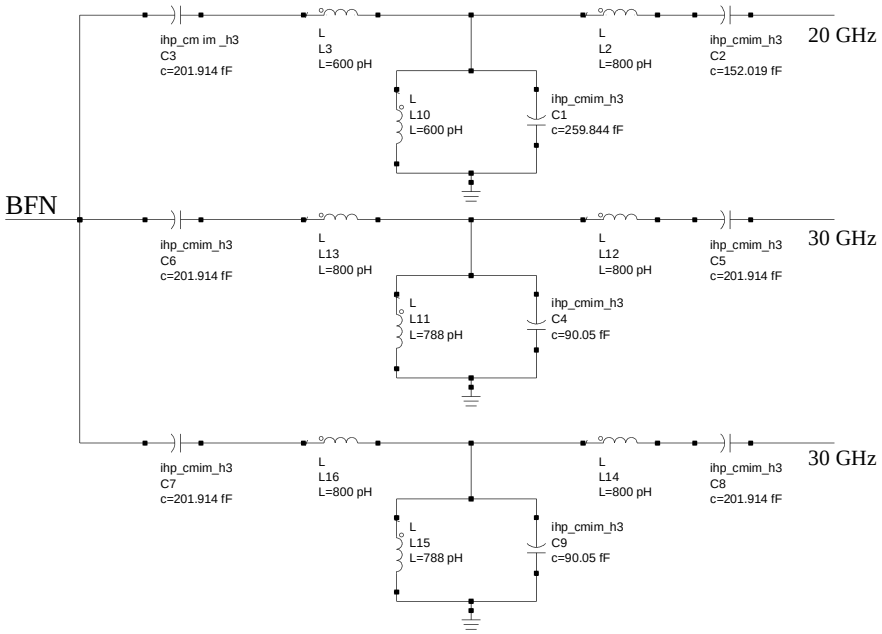

Figure 9-6: Optimized schematic of the lumped element model of the diplexer.

Using the schematic shown in Fig. 9-6 as a starting point, the layout was generated in two steps. In a first phase, the lumped elements present in the circuit were individually implemented in the SiGe BiCMOS stack up. Thus MIM capacitors and rectangular spiral inductors were used in place of the ideal capacitors and inductors respectively. MIM capacitors were imported from the SG25H3 DK whereas spiral inductors were customized and optimized using HFSS. The simulation results, achieved importing the s2p files of each spiral inductor, are shown in figure 9-7 and 9-8 for 20 GHz and 30 GHz branches respectively. As it can be seen, the filters' response is very similar to the one obtained with the lumped element model.

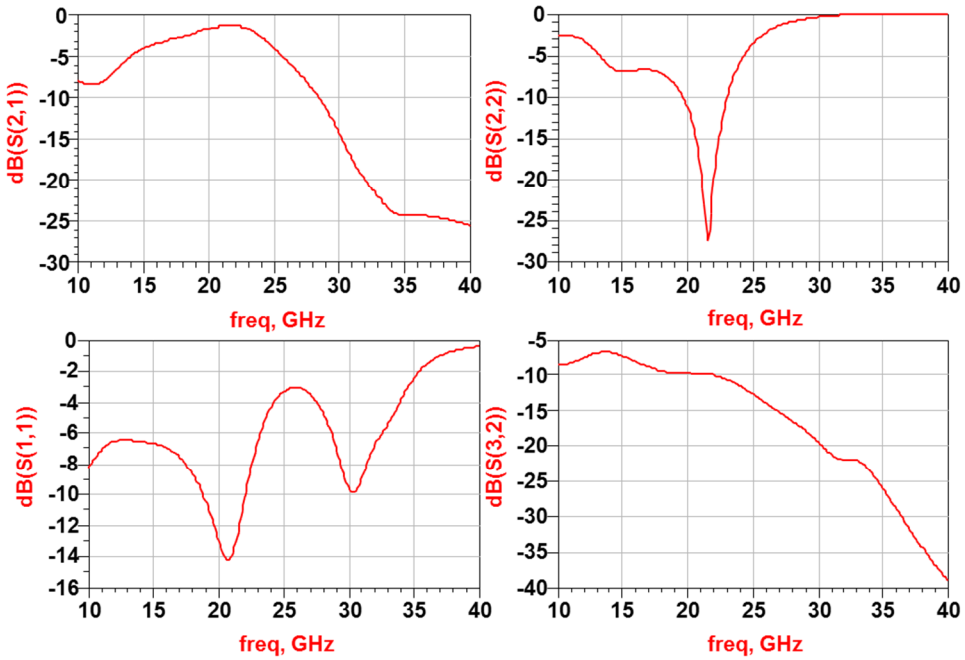

Figure 9-7: Simulated results of the diplexer schematic shown in Fig. 9-6 for the 20GHz branch

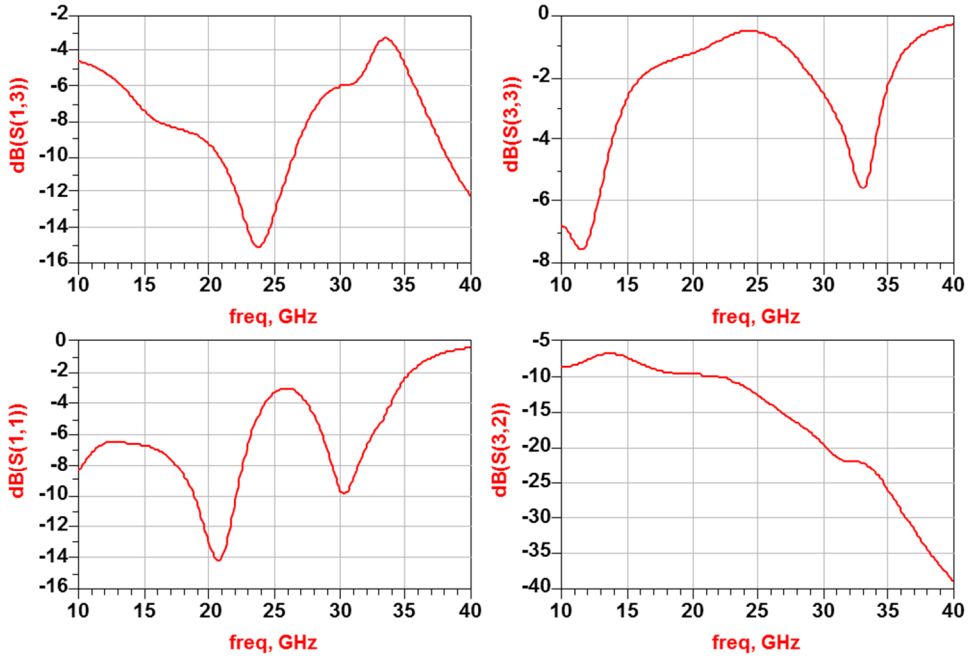

Figure 9-8: Simulated results of the diplexer schematic shown in Fig. 9-6 for the 30GHz branch

In a second phase, the layout of the whole diplexer was generated in HFSS as shown in figure 9-8 and 9-9. Simulations were performed to further improve the insertion loss performance. From the results shown in figure 9-12, 9-13, 9-14 and 9-15 it can be observed that the insertion losses are about -3dB and -5dB at 20 GHz and at the two 30 GHz ports respectively. The isolation between the two channels is approximately equal to -13 and -30 dB at 20 and 30 GHz respectively.

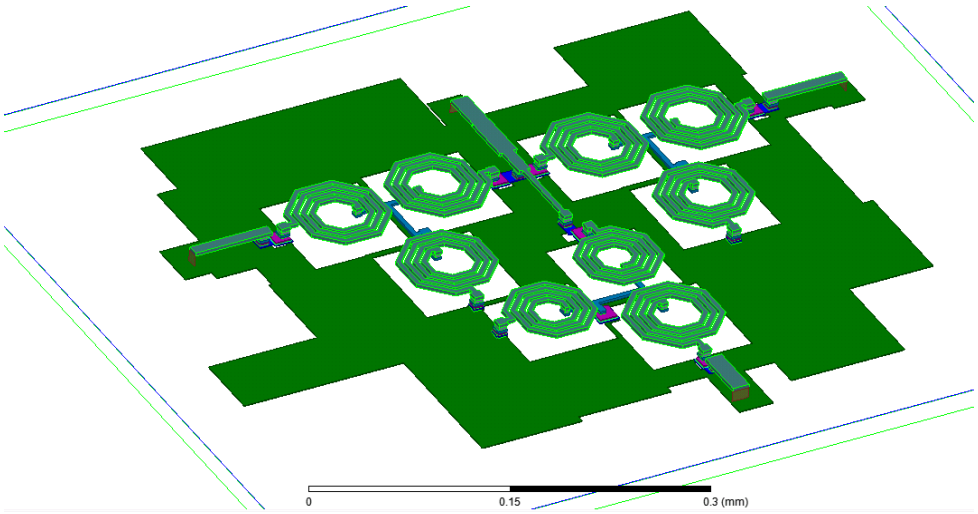

Figure 9-9: Diplexer layout as it was simulated in HFSS: 3-D view.

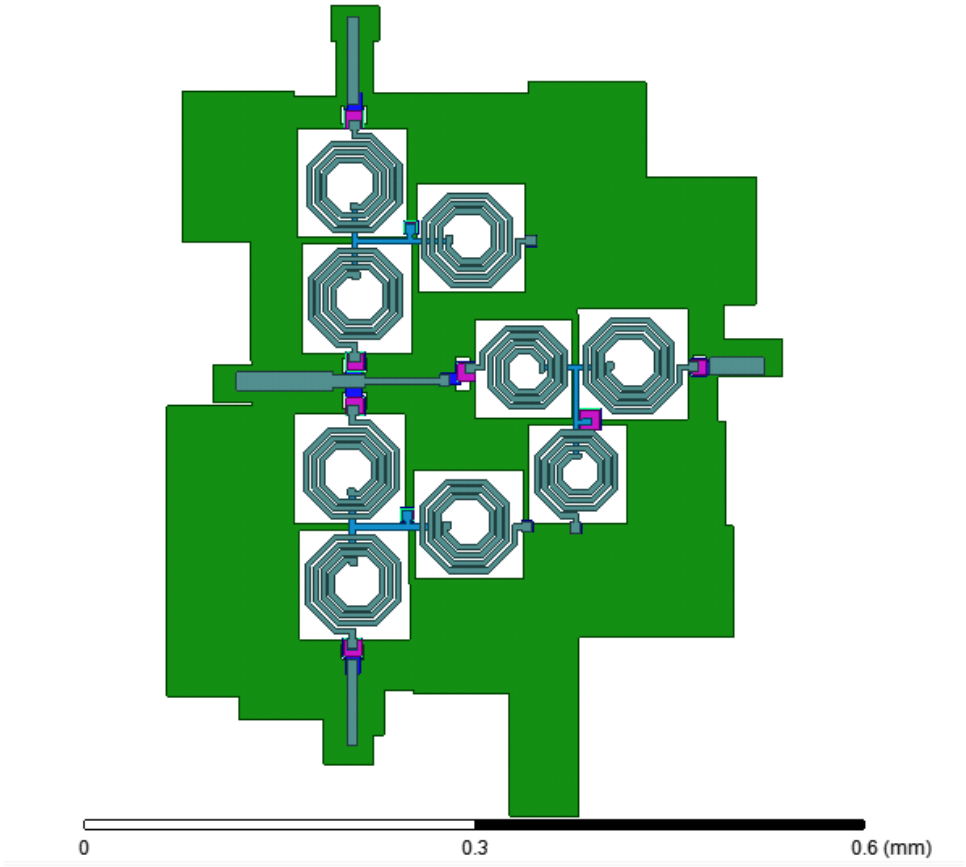

Figure 9-10: Diplexer layout as it was simulated in HFSS: 2-D view.

9.3 Measurement and results

The layout of the diplexer was generated in Cadence™ following the procedure described on Appendix A. The final layout is shown in figure 9-10. The overall size of the diplexer network is 570um×400um which is very close to that of the switching network. Five samples of the diplexer were diced and measured. A micro-photo of the fabricated diplexer is shown on figure 9-11.

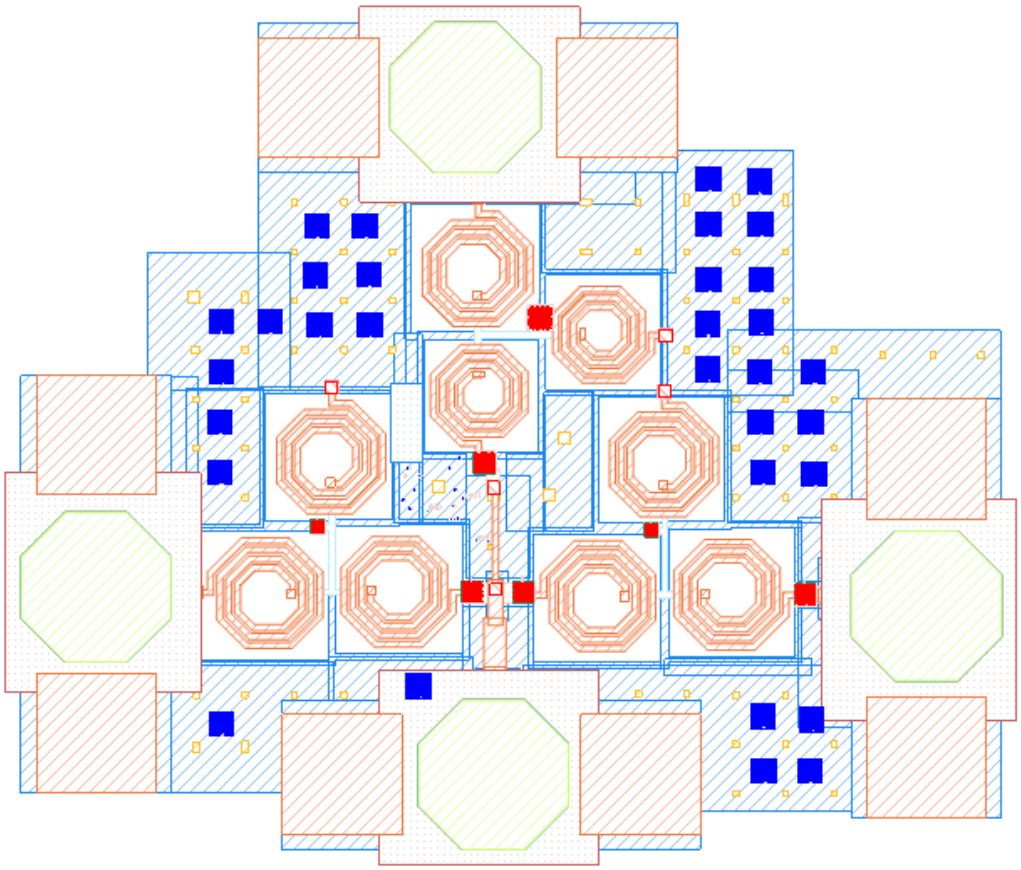

Figure 9-11: Layout of the diplexer.

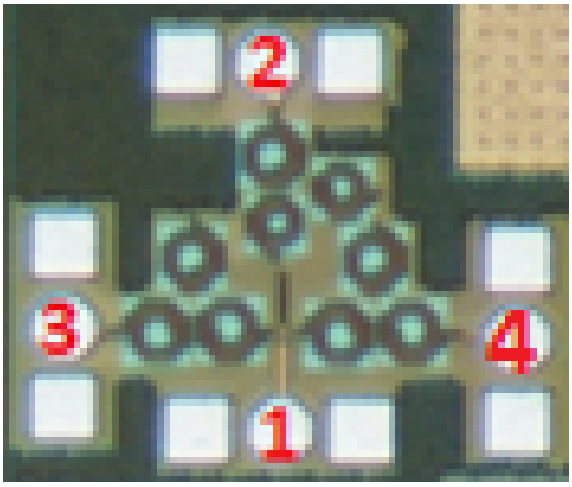

Figure 9-12: Micro-photo of the diplexer prototype.

Measurements of the diplexer were performed feeding the three ports with GSG Probes Pico 40A-GSG-100-C-N. The remaining probe was connected to a 50Ohm loaded probe. The scattering parameters were measured in the range from 10 to 40 GHz. Results are shown in figure 9-12, 9-13 and 9-14 where they are superposed to the simulated ones. As it can be observed, there is an excellent agreement between the experimental and the numerical data at all branches. Measurements show some fluctuations which are mainly due to unfiltered reflections generated at the probe termination. Both insertion losses and isolation between the two channels are coherent with the simulations. Therefore, the designed diplexer is a valid alternative for the implementation of the hexa-core Ka-band chip. With respect to the switching network presented on Chapter 9, the main advantage of this solution is to be fully passive and to have limited insertion losses. However, the diplexer isolation is less than that of the switching network.

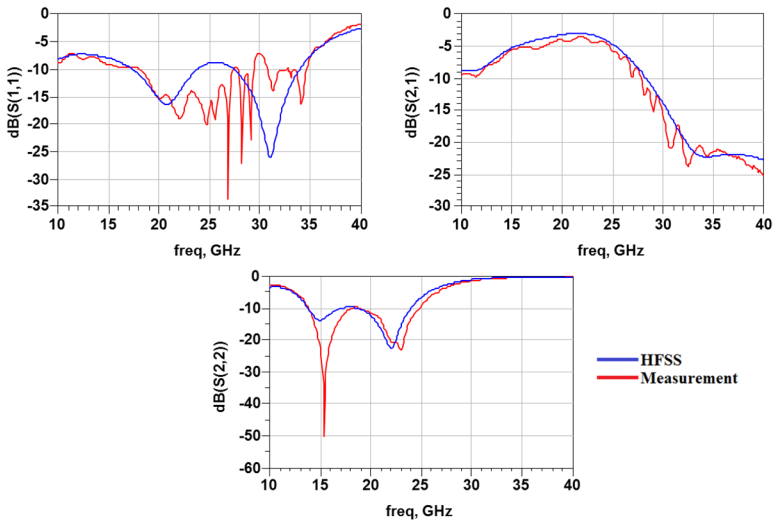

Figure 9-13: Simulated and measured results of the diplexer network: 20 GHz branch.

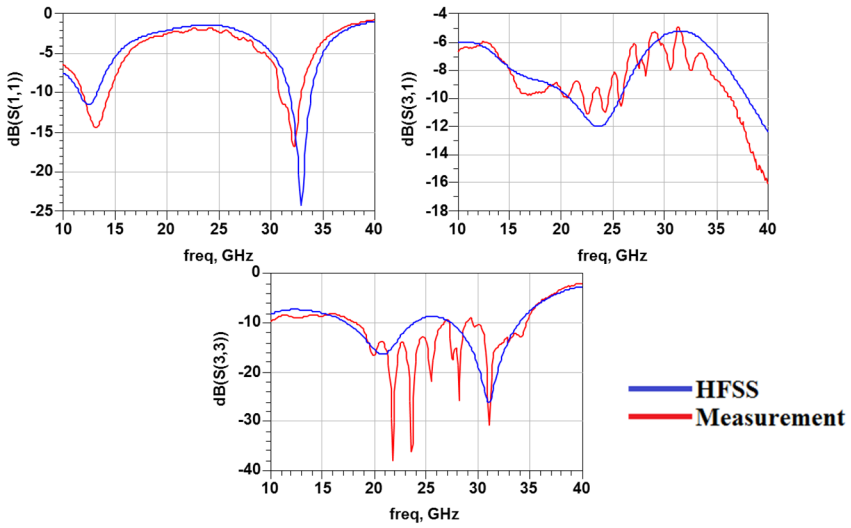

Figure 9-14: Simulated and measured results of the diplexer network: 30 GHz branches.

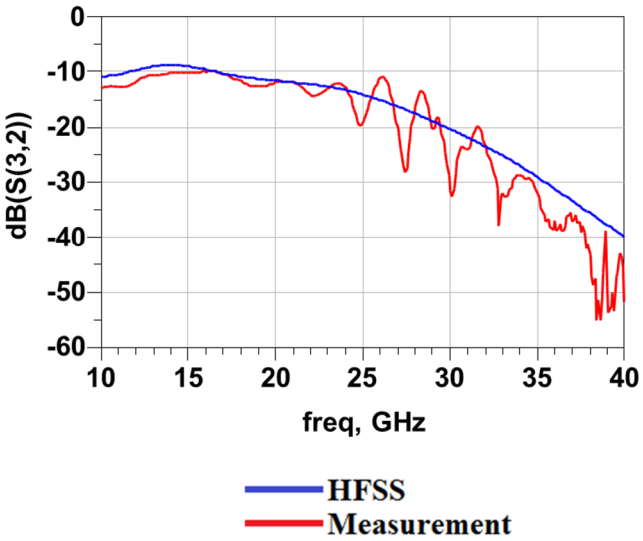

Figure 9-15: Simulated and measured results of the diplexer network: isolation.

CHAPTER 10

TEST BOARD DESIGN FOR EXPERIMENTAL CHARACTERIZATION

10.1 Test board design

To measure the designed multi core SiGe chip with full RF ports, DC controls and bias lines, designing a test board is essential. To design the test port several points must be considered as listed below:

- Dimensions
- Frequency behavior
- Wire bonding
- RF port type
- I2C connections
- DC pin grounding capacitor

Test board is designed to include the cavity which hosts the chip .The multicore chip is connected to the board pins via wire bonding. These pins are divided into four main types, namely: RF pins, DC bias pins, DC control (data) pins and ground pins and all of them must be connected to a suitable connector.

The stack up of the board is shown in figure 10-1 which shows vias and trough holes to be processed. A back etching area is used to solder the dc pins to the DC connectors from below. Layers and thickness of the board are reported in table10-1. Layers and thicknesses are selected to reduce the length of wire bonding as possible dimensions of vias and drilling holes are listed in table 10-2.

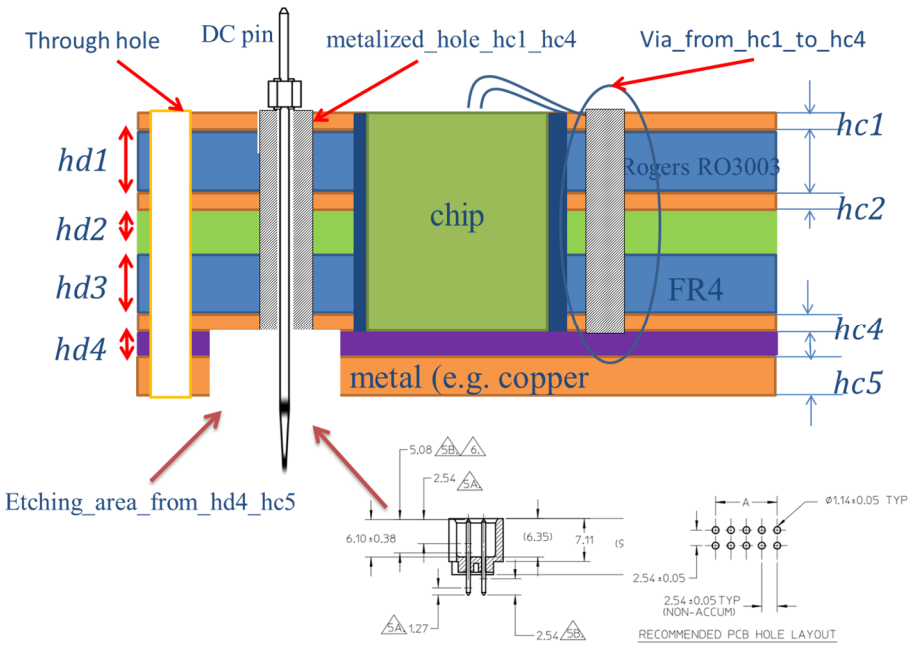

Figure 10-1: Stack up of the test board.

Table 10-1: Stack up layers information of designed test board.

Thickness	Material	Value	Type
hc1	Cu	0.035 mm	Conductor
hc2	Cu	0.018 mm	Conductor
hc4	Cu	0.035 mm	Conductor
hc5	Cu	1 mm	Conductor
hd1	Ro3003	0.127 mm	Dielectric
hd2	Glue	0.066 mm	Dielectric
hd3	FR4	0.2 mm	Dielectric
hd4	Glue	0.066 mm	Dielectric

Table 10-2: Vias and drilling information of test board

Name	Diameter-Dimension	Depth	Starting	Finishing
Via_hc1_hc4_GCPM_gnd	0.3048mm	0.481mm	hc1	hc4
Via_hc1_hc4_gnd	0.3mm	0.481mm	hc1	hc4
through_hole_rf_connector	2.0574mm	1.547mm	hc1	-
Chip_cavity	3.7mm*3.5mm	0.547mm	hc1	hc5
Chip_cavity_tool	0.6mm	0.547mm	hc1	hc5
metalized_hole_hc1_hc4	1.14mm	0.481mm	hc1	hc4
metalized_hole_hc1_hc4_pin	1.02mm	0.481mm	hc1	hc4
etching area from hd4 to hc5	18*8.5 mm& 8.69*5.32mm & 15*8 mm	1.066mm	hd4	-

By considering the thickness of RF substrate between the two metallization hc1 and hc2, a 50 Ohm with width 7.12um is printed on hc1 while the ground plane is located on layer hc2. The designed test board model is shown in figure 10-2 with RF ports named port1-7. All 7 RF ports are connected to microstrip RF end launchers that can operate up to 40 GHz. Wire bonding and chip pins accesses are shown in figure 10-3. Capacitors with 470 pF capacitance are used to ground the DC pins at RF frequencies. The fabricated prototype of the test board with the wire bonded chip is shown in figure 10-4.

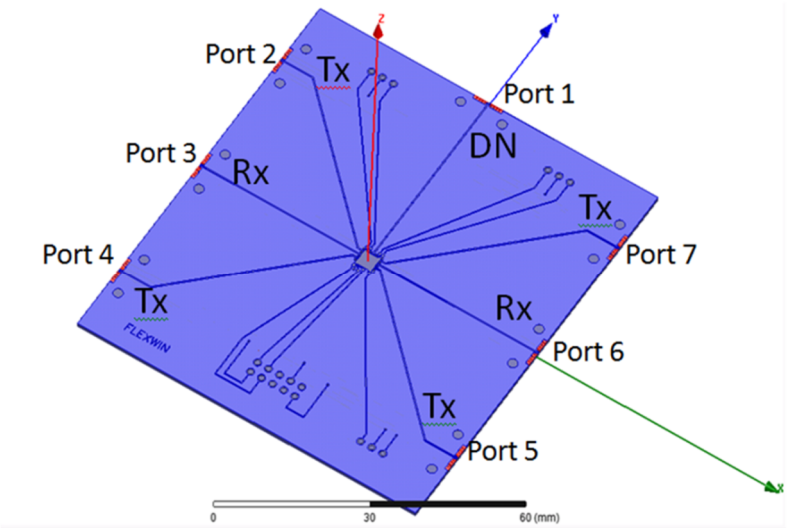

Figure 10-2: The chip test board model.

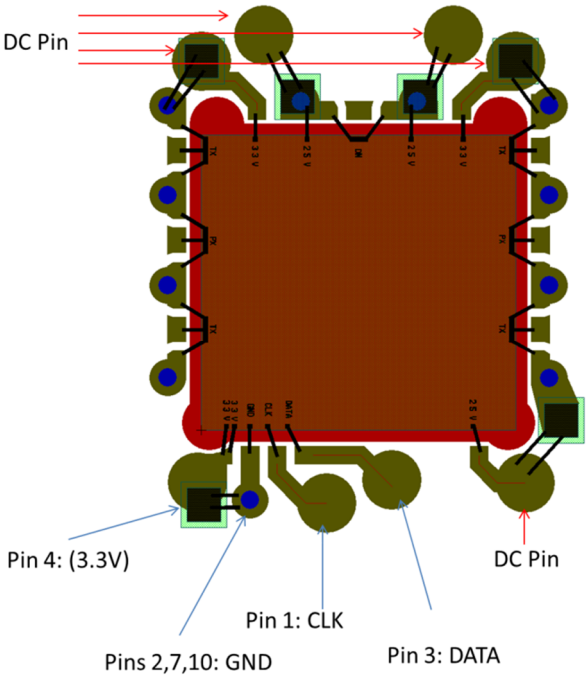

Figure 10-3: Wire bonding and chip pins on the designed test board.

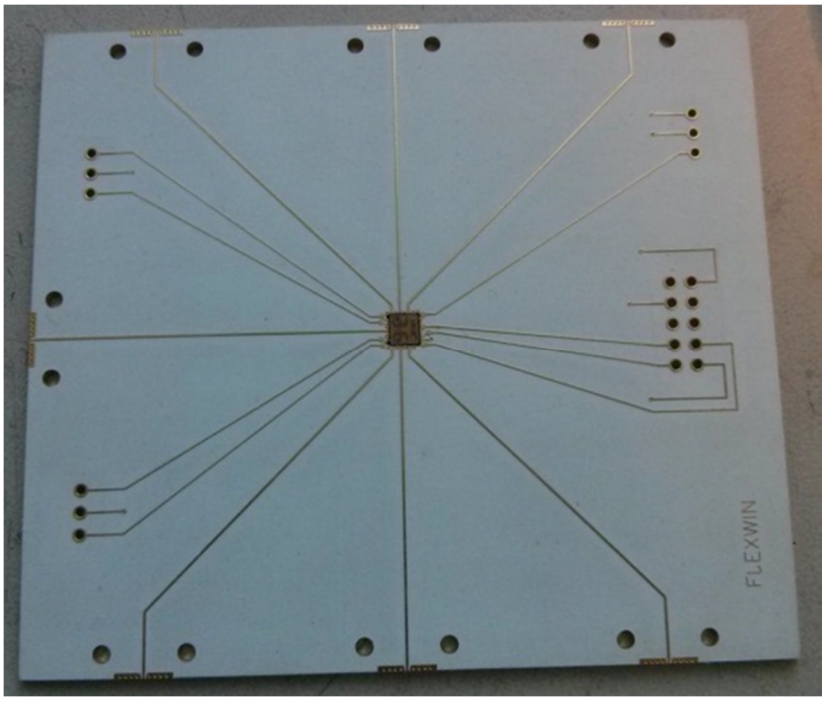

Figure 10-4: Fabricated test board prototype with multi core chip mounted.

As it can be seen on the test board there are long microstrip connections from the chip to the end launchers. Due to their length a de-embedding procedure is necessary to obtain a meaningful measurement of the performance of the chip. De-embedding may be applied following several methods, such as through reflect match (TRM) [51], line reflect match (LRM) [52], line reflect line (LRL) [53] and through reflect line (TRL) [54]. The TRL method was selected to use because the realization of thru line and of high impedance reflect load is easy to implement in printed technology. As three measurement modes are needed to characterize the chip (TX mode at 30GHz, RX mode at 20GHz and isolation between RX and T), through, line and reflect (de-embedding materials) for each measurement mode have been fabricated, as shown in fig. 10.5.

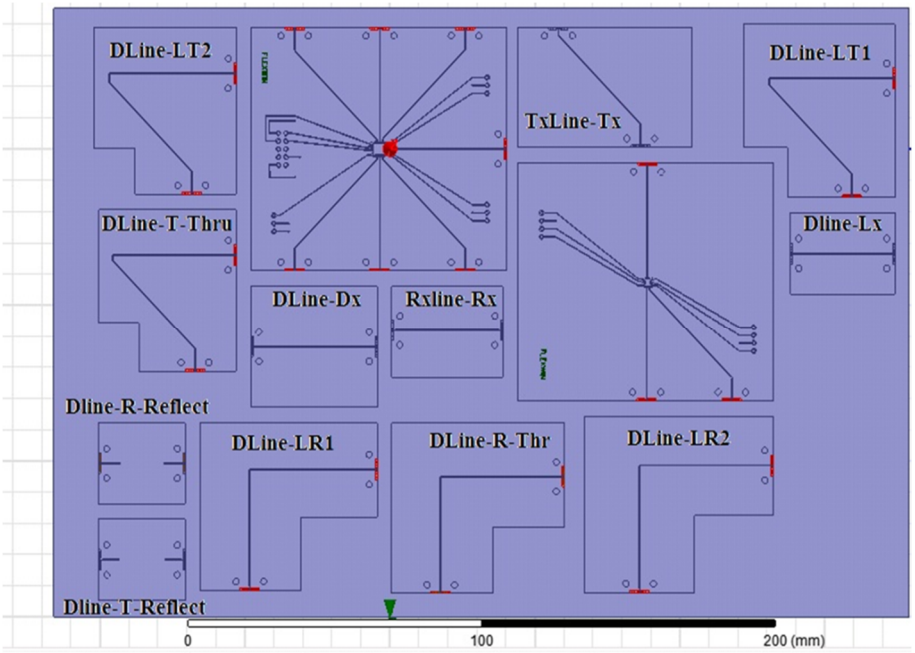

Figure 10-5: Sub circuits for de-embedding of the chip test board.

Table 10-3: Correspondences between measurement modes and de-embedding kits .

Measurement mode	Through	Line	Reflect	Line width
TX mode (30GHz)	Dline-T-Thr	Dline-LT1 or 2	Dline-T-Reflect	7.12um
RX mode (30GHz)	Dline-R-Thr	Dline-LR1 or 2	Dline-R-Reflect	7.12um
Isolation between RX and TX	Dline-T-Thr	Dline-LT1 or 2	Dline-R-Reflect	7.12um

10.2 Measurement and results

The multi core chip layout is shown in figure 10-6, sub circuits and components are also indicated by the yellow squares. A micro photo of the fabricated prototype is shown in figure 10-7.

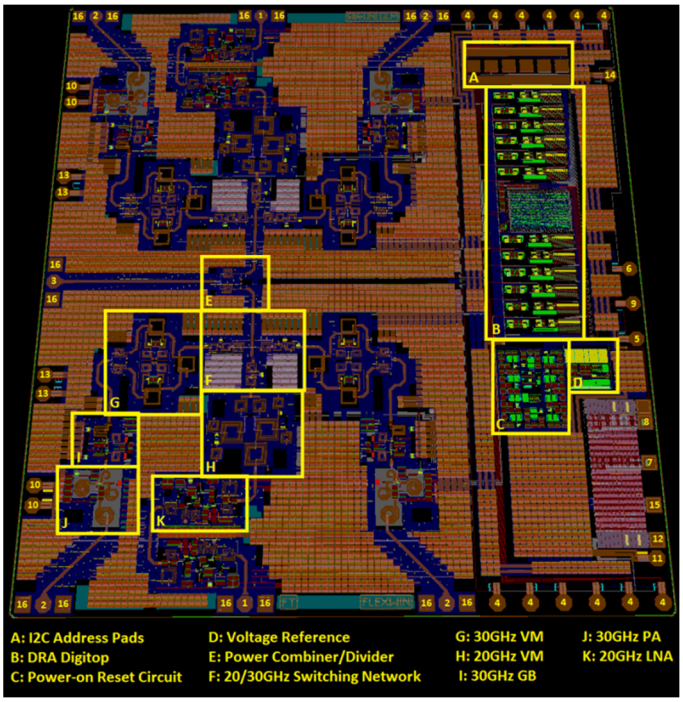

Figure 10-6: Layout of multi core chip.

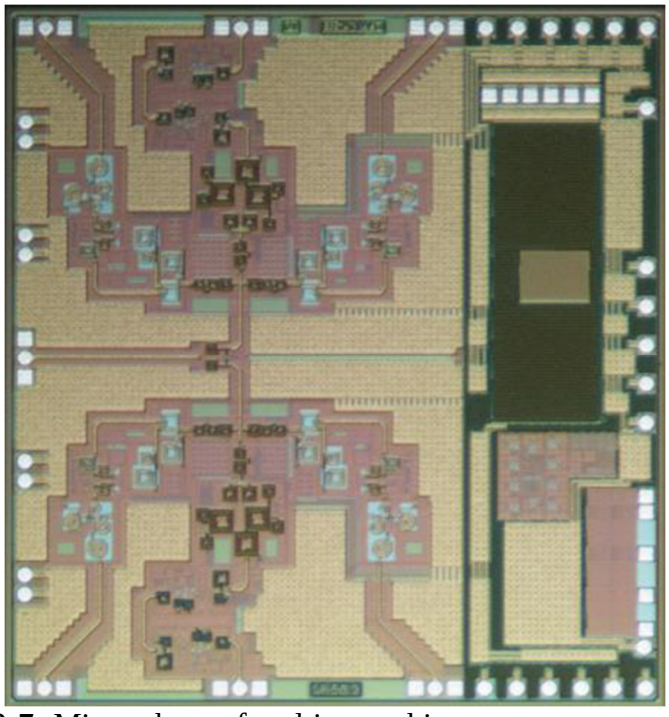

Figure 10-7: Micro photo of multi core chip.

RX measurements were done at 20 GHz while the chip is on receiving mode due the status of the switching network. In this measurement the performance of the multi core

chip is measured while power divider-combiner, switching network, 20 GHz RX vector modulator and 20 GHz RX LNA operating. The measurement was run from 15 GHz to 25 GHz covering the RX bandwidth.

The RX mode measurement is done between DN port and RX ports, indicated in figure 10.2 as port 1, 3 and 6, respectively. The other ports are terminated with 50 Ohm loads. The switching network is switched on the RX mode and different states of 20GHz RX vector modulator are considered. In figures 10.8-.10.15 are presented the chip scattering parameters. Even if the receiving bandwidth ranges from 19.7 GHz to 21 GHz a considerably larger set of frequency is shown.

In fig. 10.8 the measured return loss at port 1 (input matching) (S_{11}) is presented. As it can be seen a good matching, better than 10dB, is shown at frequency larger than required band. From 19 GHz to 20 GHz, matching is close to 10 dB so fulfilling the requirements on the bandwidth to cover.

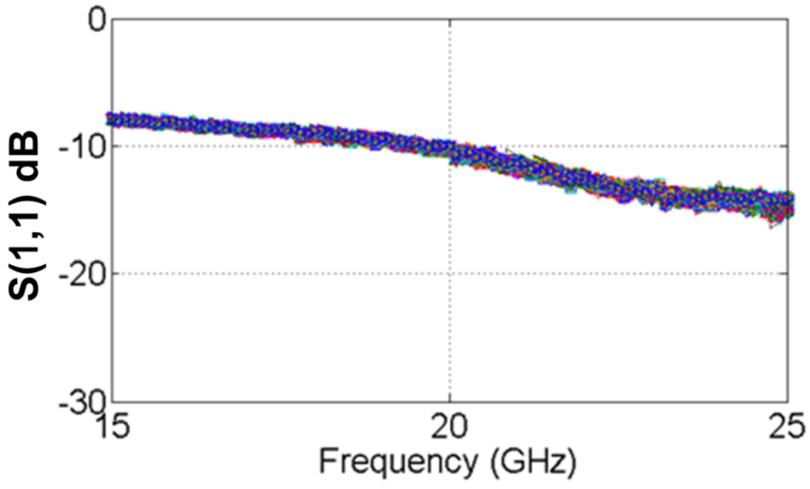

Figure 10-8: Measured input matching (S_{11}) of the chip in RX mode.

Output matching at port 3 (S_{33}), shown in figure 10.9, is better than 10 dB on the entire band considered. Port 6 has not been measured but, due to the symmetry of the chip and of the test board it is expected to present the same result.

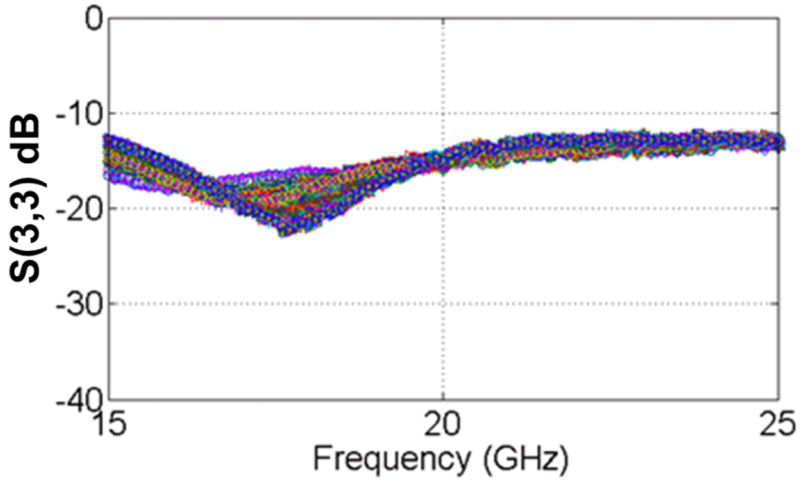

Figure 10-9: Measured output matching (S_{22}) of the chip in RX mode.

The measured gain of the chip (S_{13}) is shown in figure10-10 for different states of 20GHz RX vector modulator. As observed from figure 10-10 the maximum gain ranges from 10dB up to 20dB.

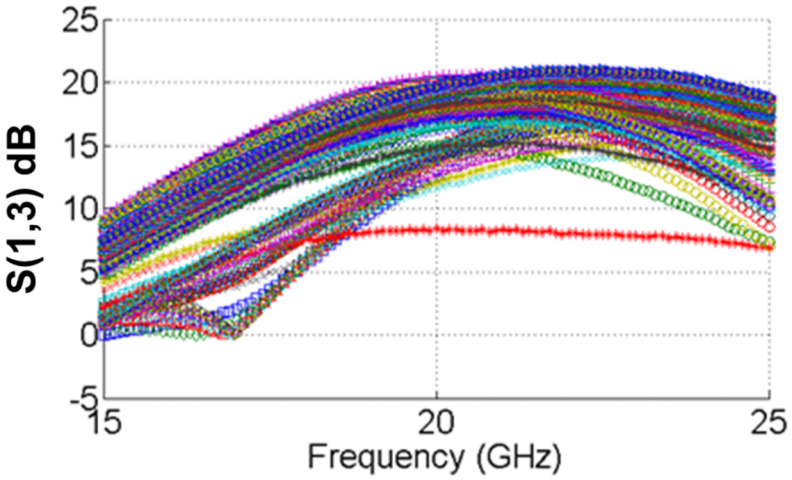

Figure 10-10: Measured gain (S_{13}) of the chip in RX mode.

In figure 10-11 the measured isolation (S_{31}) in RX mode is shiown to be better than 35dB at 20GHz as shown in figure10-11.

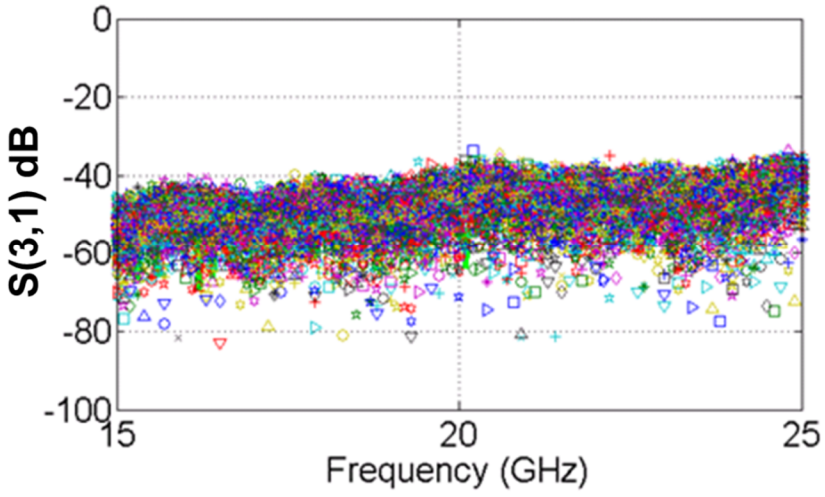

Figure 10-11: Measured isolation (S_{31}) of the chip in RX mode.

TX measurements were done at 30 GHz while the chip is on transmitting mode due the status of the switching network. In this measurement the performance of the multi core chip is measured while power divider-combiner, switching network, 30 GHz TX vector modulator and 30 GHz TX power amplifier operating. The measurement was run from 25 GHz to 35 GHz covering the TX bandwidth.

The switching network and the power divider, presented in chapters 6 and 8, are parts of both the RX and the TX chains. For this reason measurements on the TX side of the chip are also presented. Notice that, other than the switch and the power divider, no others components operating in the TX band have been the subject of the work presented in the present thesis. TX amplifier and vector modulator have been designed at the Univesrity of Ulm (D). The TX mode measurement is done between DN port and TX port; indicate in Figure 10.2 as port 1 and ports 2,4,5,7. . As in the RX case the other ports are

terminated with 50 Ohm loads. Measurements refer to the condition in which the switching network is on TX mode and to different states of the 30 GHz TX vector modulator. In fig. 10.12 are shown the measured return loss at port 1, which account for the input matching (S_{11}), which is below 10dB at 30 GHz in almost all the band considered and in particular within the range 29.5 GHz -30.8 GHz

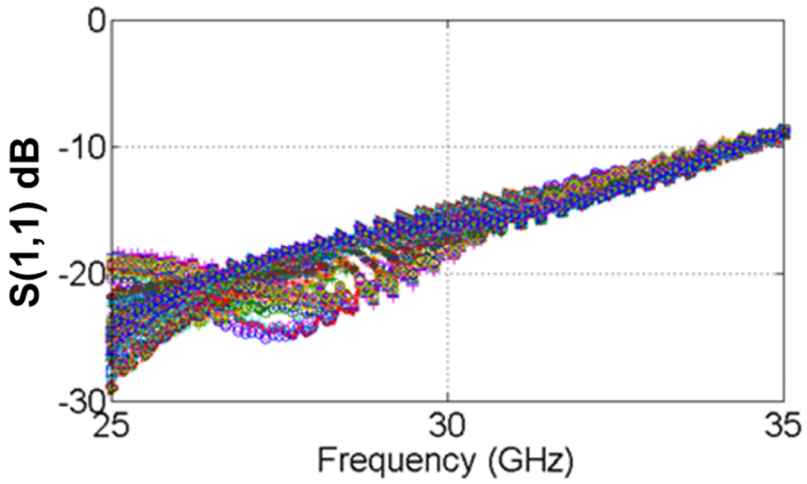

Figure 10-12: Measured input matching (S_{11}) of the chip in TX mode.

Output matching (S_{22}) is presented in figure 10.13. Strong mismatch is observed out of the band of interest, while in the range considered for the Ka band TX operations S22 stays close to or better than 10dB.

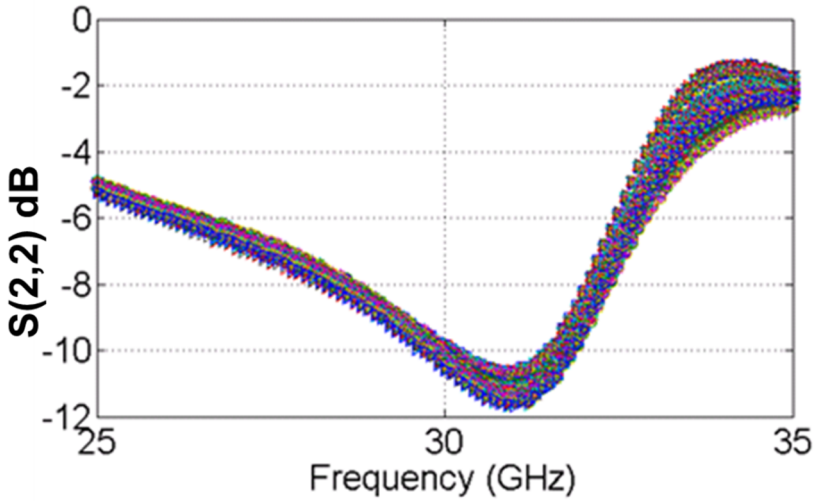

Figure 10-13: Measured output matching (S_{22}) of the chip in TX mode.

The measured gain of the chip (S_{21}) is shown in figure10-14 for different states of 30GHz TX vector modulator. As observed from figure 10-14 the maximum gain ranges from 5 dB up to 14 dB.

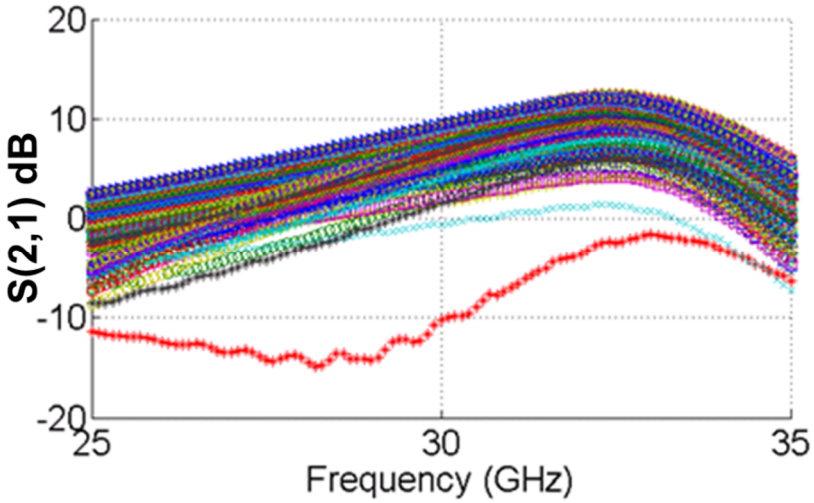

Figure 10-14: Measured gain (S_{21}) of the chip in TX mode.

As last results, the isolation (S_{12}) in TX mode is reported in figure10-15, and it stays below -50 dB in all the band considered

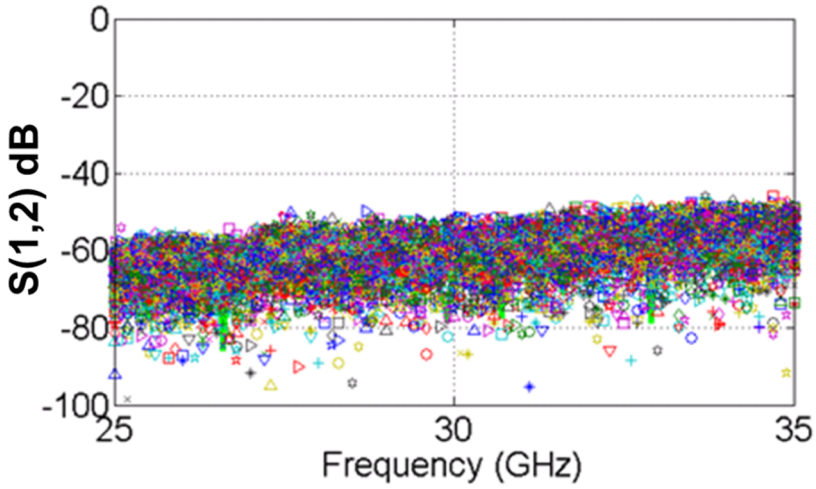

Figure 10-15: Measured isolation (S12) of the chip in TX mode.

CHAPTER 11

CONCLUSIONS AND FUTURE WORK

11.1 Conclusions

The work presented in this thesis was carried out in the framework of a project funded by the European Community aiming at designing and realizing a highly integrated chip to be used in a phased array antenna. The chip was designed using SiGe (Silicon-Germanium) technology because it permits to integrate many T/R modules in the same IC so making easier their integration with the radiating elements. Furthermore, for large scale production, SiGe is cheaper than GaAs and it is promising to be the technology of choice to bring phased arrays from military to consumer applications.

The requirements followed during the design phase were the one of a Ka-band SatCom on the move user terminal

The work presented in the previous chapters mainly focused on the RX chain of the chip for which a LNA and a vector modulator were designed. Furthermore, the design of a network to switch between the TX and the RX chains and of a wide band power divider was also carried out. As an alternative to the switch the design of a diplexer has been considered and a compact design has been produced. Measured results of single components have shown performances in most of the cases within the requirements or, in

very few instances, at the limit. The components have been integrated in a multi core TX/RX SiGe chip with four TX chains and two RX chains including the switch and the power divider. A test board has been designed to test and characterize the entire chip. Measured results were within specifications and in line with the ones measured for single components.

11.2 Future Work

The designs presented in this thesis may be improved in many ways:

- ✓ Performances of the LNA can be improved by correcting the bipolar transistor model provided by the design kit. The accurate simulation of dc block capacitors and interconnection transmission lines will be also helpful
- ✓ A buffer stage should be added to LNA input and output ports to provide more stability and to improve impedance matching. Even if this would increase LNA size.
- ✓ Performances of the vector modulator could be improved designing hybrid transformer of different types, such as up down coupling hybrid or lumped model hybrid. Also, the bandwidth of vector modulator would improve by using wide band hybrids. Size reduction of vector modulator could be achieved by reducing the size of the hybrids and of the inductors.

- ✓ Better isolation and lower insertion loss could be obtained for the switching network, adopting FET transistors with smaller size of the gate. . To increase isolation, series single switches could be added to each required branch even if at the expenses of the insertion loss and of the overall size of switching network.
- ✓ Isolation of the power divider-combiner could be improved by adding an isolator stage between the two branches or by adding an inductor and an extra capacitor to each branch. Size of power divider and combiner must remain small and this is challenging for future designs.

Other than improving the current designs future development may be devised. As an example a chip which integrates polarization controls would be a challenging and a useful development. In fact, the availability of dual linear polarization or dual circular polarization circuitry on chip would be extremely useful for the future Ka band satcom applications.

APPENDIX A

LAYOUT GENERATION

A.1 Cadence schematic

In this appendix the layout generation procedure is described. The schematic of the LNA reported in Chapter 5 is taken as a reference case.

Starting from the schematic, the layout generation requires the following steps:

- Creating a new library (i.e. project) in Cadence;
- Creating a new cell view from file in main Cadence window;
- 2 cells should be created. One called "LNA core" and the other "LNA total";
- For the "LNA core" 3 views must be created (Layout-Schematic-Symbol)
- For the "LNA total" only one view must be created (Schematic)
- Starting from "LNA core" –Schematic view to create a schematic (similar to ADS)

The schematic of the designed LNA is shown in figure A-1. In The "LNA core" cell, ports are created to define the RF input and output ports and for the DC bias. The same ports are then used in the symbol of the "LNA core" and, in turn, embedded into the "LNA total" schematic. Simulation of the "LNA core" schematic is done in the schematic window calling the "ADE L" tool as shown in figure A-3. After setting the analysis, the

simulation can be launched and the results can be viewed directly into the Cadence window.

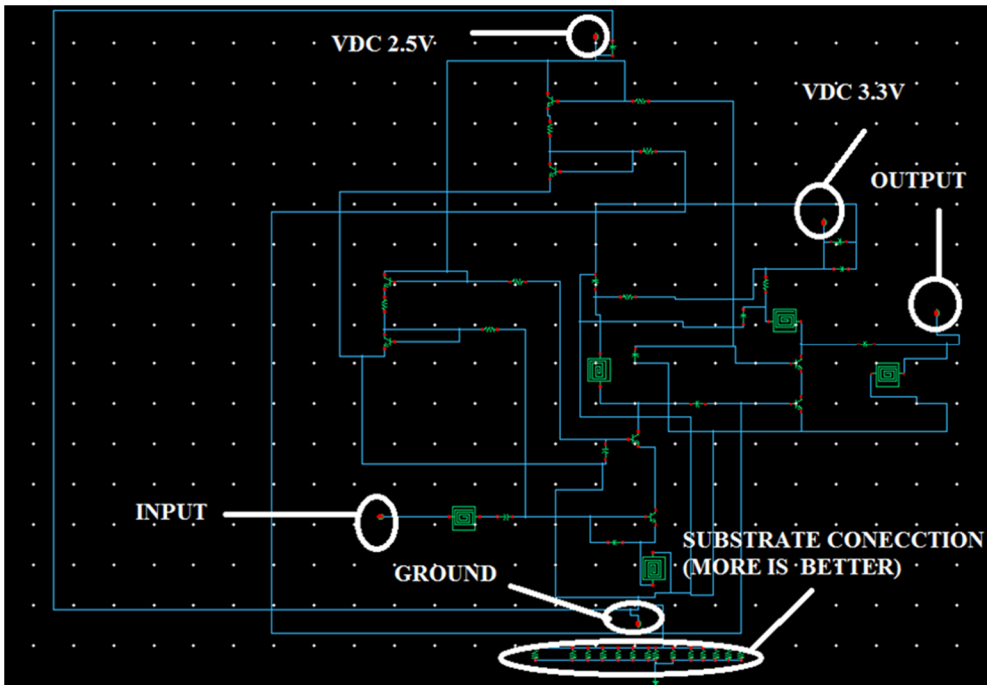

Figure A-1: "LNA core" schematic created in Cadence.

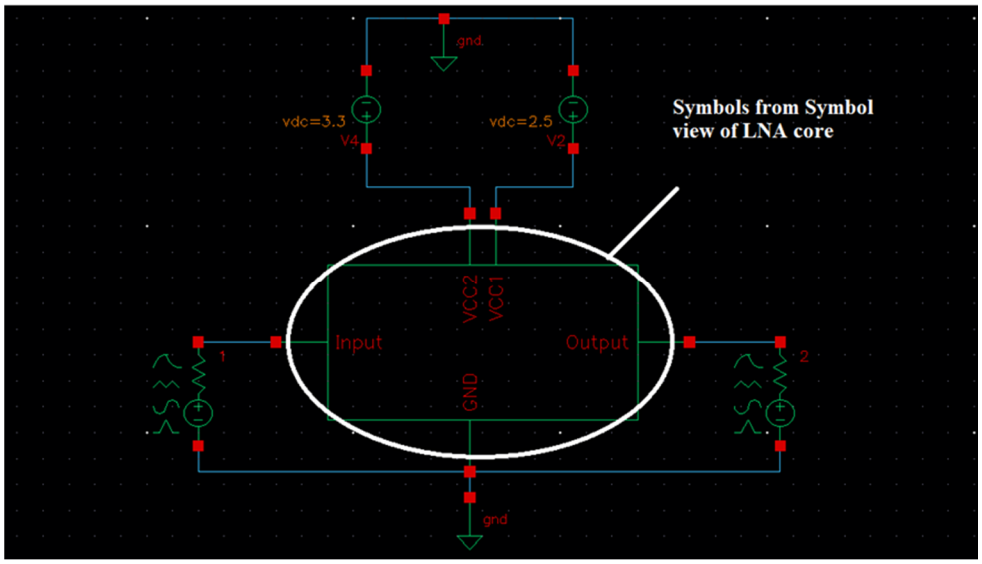

Figure A-2: "LNA total" schematic. In the center of the schematic is located the symbol of the "LNA core" with RF ports and bias voltages.

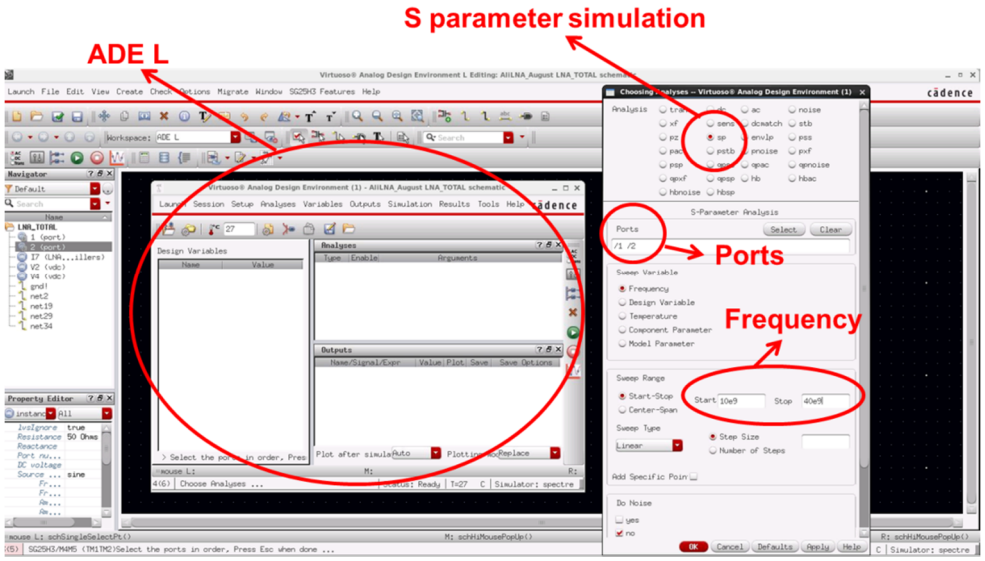

Figure A-3: "ADE L" tool and options in Cadence.

A.2 Layout generation

Layout generation in Cadence can be done automatically. However connecting the components, checking the design rules and the layout verification requires a manual interaction. To generate the layout, the following steps should be followed:

- Adding ports to designed LNA (Input-Output-V DC-Ground) in schematic window
- Adding parallel substrate connections to ground in the schematic window (the more the better to reduce the total impedance of ground)
- Lunch "Layout XL" from schematic window to create a new layout view which is created automatically. This first layout needs to be drastically changed before it can be ready for the final steps;
- Set the grid of layout to the smallest dimension as it is indicated in the design kit. This step is very important to prevent off-grid errors;

- Start to locate and to position the transistors, the inductors and the capacitors in the layout. The interconnections should be done trying to minimize the RF pass length;
- While locating single components or interconnection lines consider the design rules related to maximum current handling capability (this parameters affects the line width) or minimum distance between adjacent elements;
- The layout should be created sketching before the location of the different components and trying to identify at the earliest stages the optimal location of the DC and RF pads;
- Interconnection between different layers should be done using array of vias. The higher the size the better it is to reduce the inductance to ground and the resistance. A typical minimum value is 4x4;
- All all connections should be checked before to start the layout of the ground layer;
- Perform layout versus schematic analysis to check if there is any missing component. This can be done from Layout window>verify>LVS ;
- placing both signal and bias pads in the layout window namely ground signal ground (GSG) pad and power ground power (PGP) pad respectively. Typically, these components are not included in the schematic. These pads will be fundamental for the measurements and their location should be carefully evaluated in relation to the test set-up.

- Drawing ground plates on Metal 1 and removing unnecessary metal 1 space from ground plates in the layout window
- Placing slits as mentioned in design rules to reach the 0 error on the DRC primary verification in the layout window (shape, size and distance between slits must be compliant with the design rules)
- Placing P-tabs in the design everywhere that is possible in layout window (using more P-tabs will reduce total substrate resistance)
- Drawing polygons on each layer (e.g. “no filler” layer on M1, M2, M3, TM1 and TM2 for spiral inductors) around the RF pass and everywhere it is not necessary to have filler as no filler layer;

Now the layout is ready without fillers and the final design rule checks (DRC). The fillers creation can be done automatically. Fill rule check is a separate rule check, which has to be loaded separately from the Assura DRC UI. In “Rules File” text area replace drc.rul with fill.rul. Copy content of the “Rules File” in “RSF Include” and replace fill.rul with fill.rsf as shown in figure A-4.

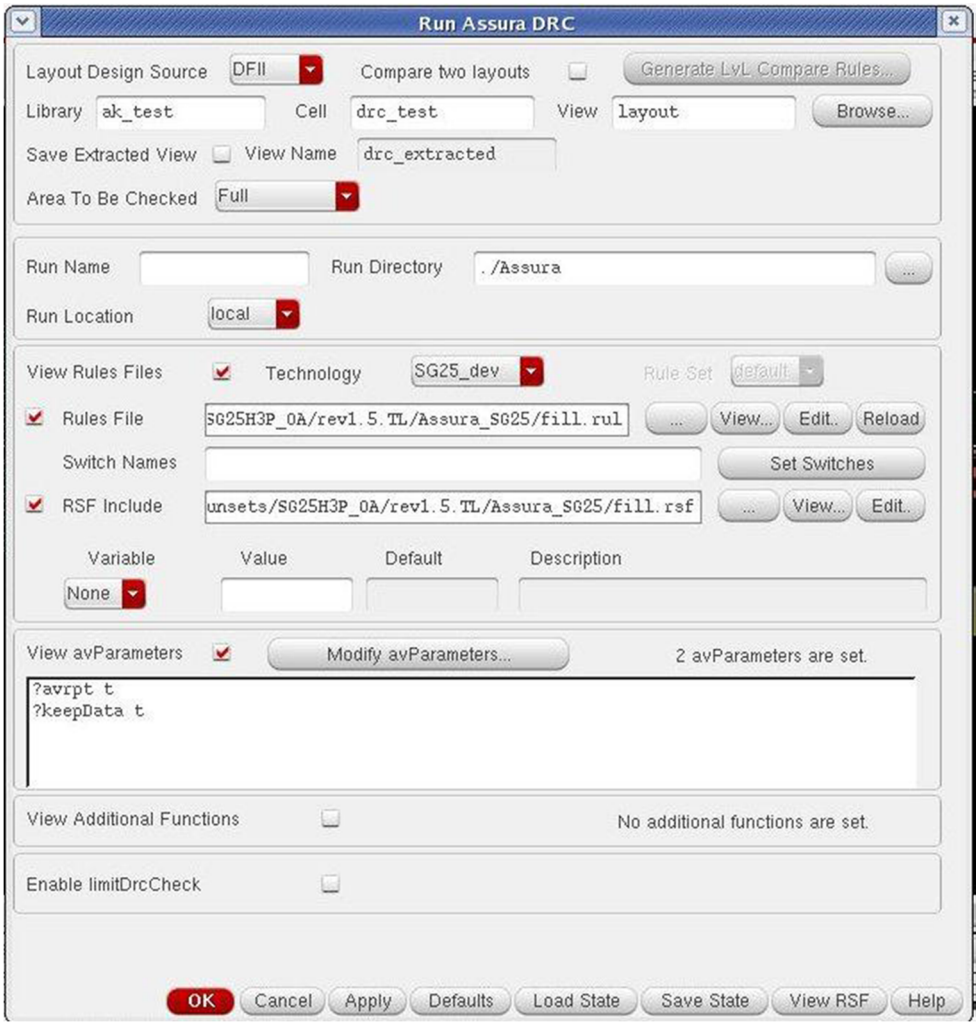

Figure A-4: Assura DRC check.

Then click on “Set Switches” button and choose the layers which have to be filled. In LNA layout generation all 5 metalized layers and active layer have to be filled. The Assura set-up for proper filler generation shown in figure A-5 is replicated here below:

- Fillergenerationmode
- FillerGenerationActive
- FillerGenerationMetal 1

- FillerGenerationMetal 2
- FillerGenerationMetal 3
- FillerGenerationTopMetal 1
- FillerGenerationTopMetal 2

Figure A-5: Filler generation settings set-up.

It is possible to fill several layers at once. Select all layers which have to be filled by pressing “Ctrl” button and select multiple layers. Press “OK” button to start the DRC fill run. After running the DRC, a new library is created: “AssuraOutLib” as shown in figure A-6. This library contains a cell which has the same name of the designwhich was filled. Due to an error in the design kit, to generate the active fillers, the switches of

Fillergenerationmode and FillerGenerationActive must be selected twice and some corrections in the filler distance in some cases must be done manually (if is necessary). According to the IHP DK, in the case of the LNA minimum and maximum distances for the active layer are 1.5 um and 8 um respectively.

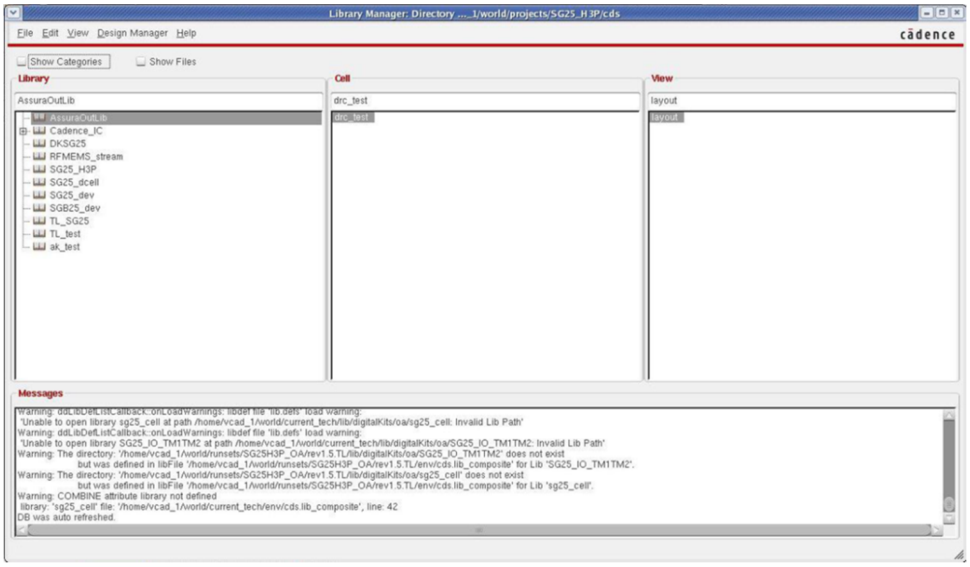

Figure A-6: Library created automatically included the layout with fillers.

Figure A-7 shows the Cadence layout screenshot whit some notes about Assura.

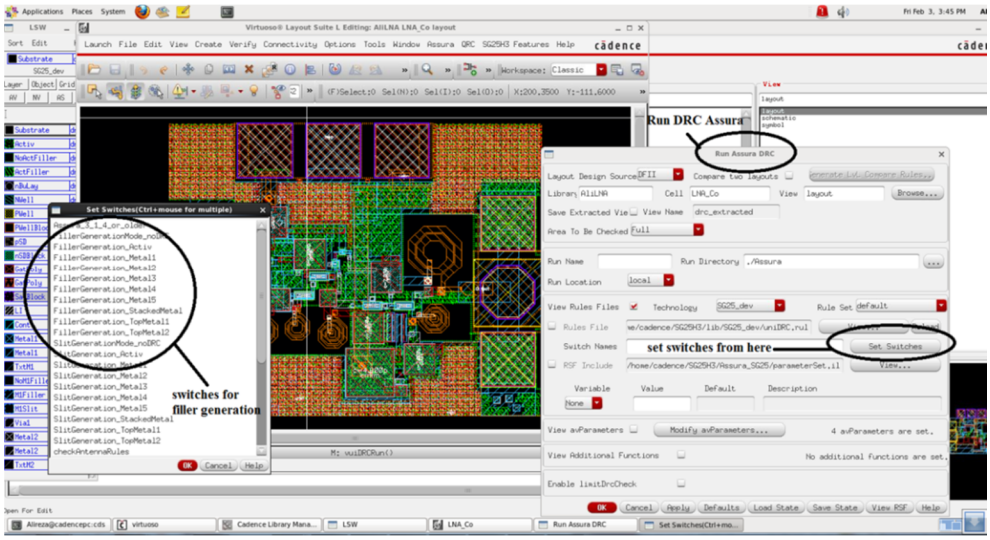

Figure A-7: Cadence layout screenshot with Assura.

After filler generation the design rule must be checked using the Assura DRC check, as shown in figure A-8. To DRC check, the following switches must be set as listed below:

- CheckFillerRules
- DontCheckTies
- NoOffGrid
- NoRecommendedRules
- CheckDensityRules
- CheckGlobalDensityRules

Figure A-7: DRC check switches in Assura.

Then DRC errors can be checked and corrected until the layout becomes DRC clean as shown in figure A-9. Each error in the DRC can be located in the layout and hopefully emended. The final layout of LNA with fillers is shown in figure A-10.

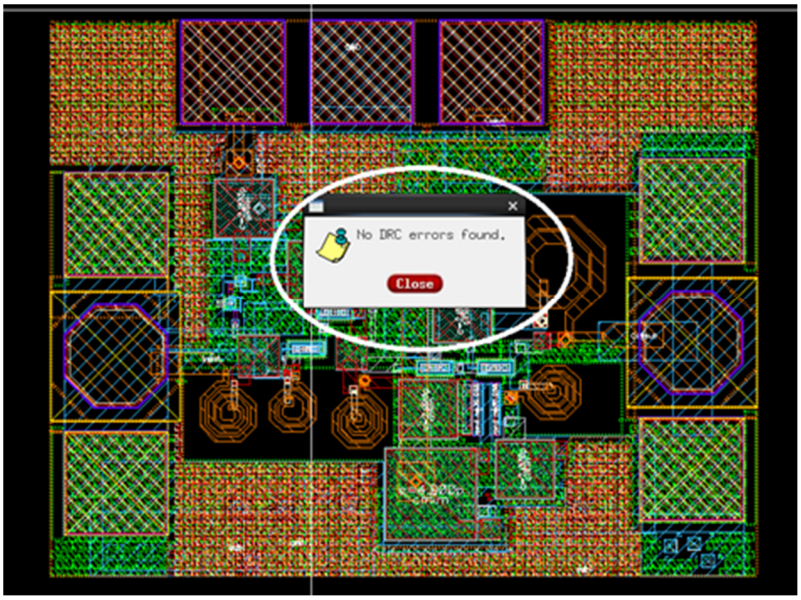

Figure A-9: DRC checked without any error

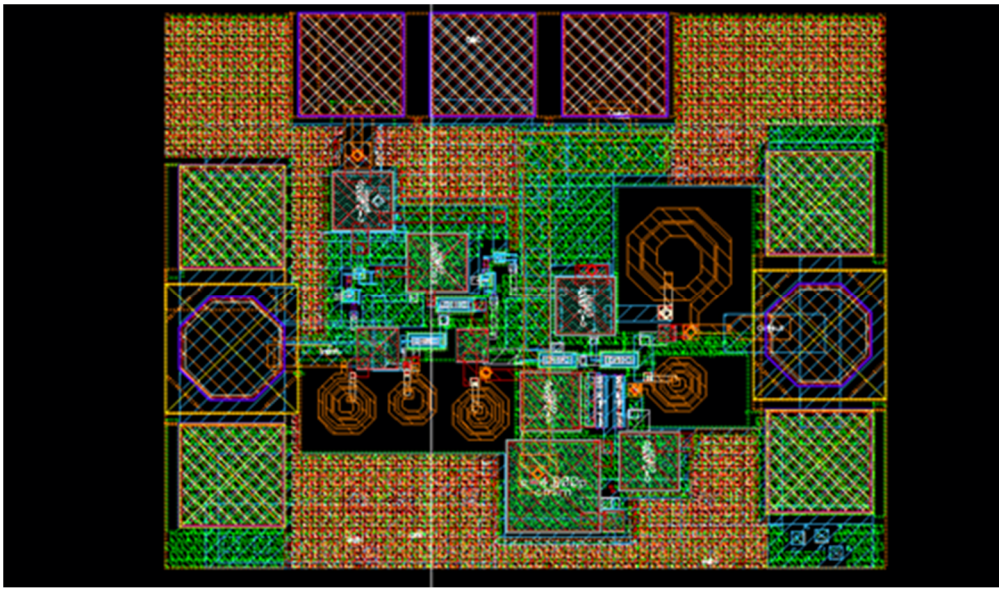

Figure A-10: Final layout of the LNA with fillers that is ready to export as GDS file.

Once completed, the layout is ready to be exported using the GDS file format. To export the GDS file from main window, the following path must be selected as shown in figure A-11:

File>Export>Stream>Stream file (Location of GDS file)>Translate

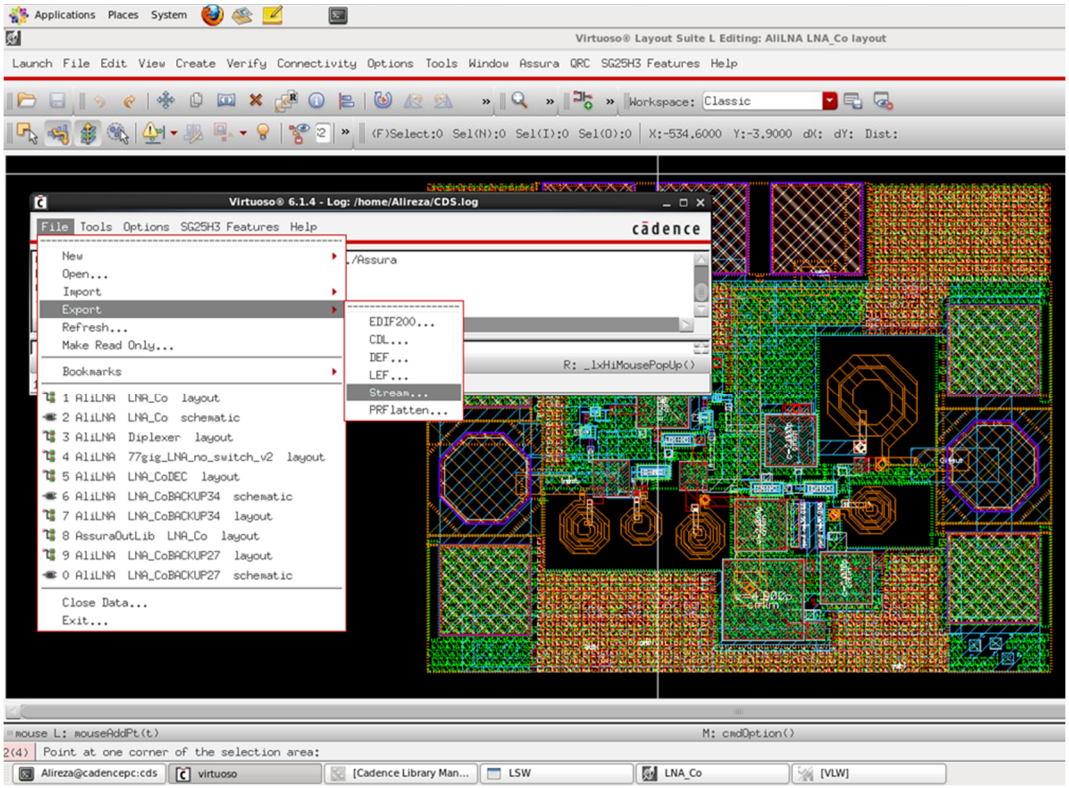

Figure A-11: Screenshot of the GDS exporting process in Cadence.

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